An ASIC Control Circuit for Thermal Actuated Large Optical Packet Switch Array

Jian-Chiun Liou[1], and Fan-Gang Tseng[1, 2, 3]

Abstract—**In this article we propose the employment of an ASIC integrated control circuit to compensate the fabrication error and tuning the wavelength response in a thermally actuated ring type optical switch. Additional functionalities can also be added in this circuit by tailoring externally the roundtrip loss or coupling constants of the ring. The design concept can be easily scaled up for large array format optical switch system without much change in the terminal numbers thanks to the three dimensional hierarchy of control circuit design, which effectively reduces the terminal numbers into the cubic root of the total control unit numbers. The integrated circuit has been designed, simulated, as well as fabricated, and demonstrated a decent performance with Free Spectral Range (FSR) equal to 1.5nm at a wavelength of 1534nm and center wavelength shift of the ring up to 0.3nm for thermal actuated ring type optical switch.**

***Index Terms*—Optical switch, tuning wavelength, electrical control, actuated, modulation frequency.**

I. Introduction

Advances in communication technology and growth of Internet traffic have continuously driven the rapid evolution of networks. Compared to the traditional optoelectronic switches, all-optical switches provides high throughput, rich routing functionalities, and excellent flexibility for rapid signal exchange in fiber optical network systems. Among various all-optical switches, thermally actuated ring-type switches provide the advantages of high accuracy, easy actuation, and reasonable switching speed.

The planar-lightwave-circuit switch (PLC-SW), which employs the thermo-optic effect of silica glass, is very promising because of its many advantages such as its low insertion loss, high extinction ratio, long-term stability, and high reliability[1-4]. However, when scale up, thermal ring switch may encounter issues related to fabrication error, non-accurate wavelength response, and large terminal numbers in the control circuit. Traditional 2D architecture of driving circuits can not meet the requirement for high scanning speed and low data accessing points when switch numbers greater than 1000.

This paper proposes a novel application-specific integrated circuit (ASIC) architecture of high-selection-speed three-dimensional data registration for optical networks applications. With the configuration of three-dimensional data registration, the number of data accessing points as well as the scanning lines can be greatly reduced for large array optical packet switching chip with switch number more than 1000. All the sub-circuits, including power control, digital I/O, analog-to-digital converter, power drivers were integrated into a single device. This circuit has been designed, fabricated, and characterized. It demonstrated not only the functionality in the optical packet switching chip but also the consistency between simulation and experiment results. We have already developed a simple and practical phase-trimming technology to correct permanently the phase-error in each ring and to enable us to avoid the need for electrical biasing. The phase-trimming technique employs a local heating method with a thin-film heater. In another hand, enhancement of the number and array density of switch within an optical packet switching chip is one of the keys to raise the throughput.

Manuscript received March 20, 2008. (Write the date on which you submitted your paper for review.) This work was supported in part by the Chip Implementation Center (CIC),TSMC,Taiwan, for organizing the chip fabrication..

Jian-Chiun Liou is with the Nano Engineering and Micro Systems Inst., National Tsing Hua University, Taiwan, ROC. His research interest is in the ASIC design, MEMS technology and integration of optical switch array processes . (corresponding author to provide phone:886-3-5715131; fax:886-3-5745454; e-mail: d939201@ oz.nthu.edu.tw).

Fan-Gang Tseng is with 1:Nano Engineering and Micro Systems Inst., 2:Engineering and System Science Dept.National Tsing Hua University, Taiwan, ROC. 3:Division of Mechanics, Research Center for Applied Sciences, Academia Sinica, Taiwan, ROC. (e-mail: fangang@ess.nthu.edu.tw)

II. Design concept

This ASIC architecture involves three-dimensional multiplexing with the provision of a gating transistor for each optical-switch resistor, where optical-switch resistors are triggered only by the selection of their associated gating transistors. Three signals: selection (S), address (A), and power supply (P), are employed together to activate a switch for changing optical wavelength phase. The smart optical packet switching chip controller has been designed by a 0.35 μm CMOS process with a total circuit area, 2500×2500 μm^2, which is 80% of the circuit area by 2D configuration for 1000 switches. Experiment results demonstrate the functionality of the fabricated IC in operation, signal transmission and a potential to control more than 1000 switches with only 31 data access points and reduced 30% scanning time. One of the major goals for advanced optical packet switching chip design is to optimize high throughput while minimize cost and thermal tuning speed optimization of thermo-optic devices. To achieve this, first, the most commonly employed architecture of driving IC for commercial optical packet switching chip nowadays is carried out by two-dimensional arrayed-switches. The data accessing points will be N (Pads) $=2\times\sqrt[2]{Y}+1$ (Y~ Switches), which is equal to 21 if the switch number is 100. However, if the switch number increases to thousands in a large array optical packet switching chip, not

only the data accessing points will be easily increased to hundreds, but also the scanning time will significantly rise, which deteriorates the performance of network. In this study, a three dimensional data registration scheme to reduce the number of data accessing points as well as scanning lines for large array optical packet switching chip with switch number more than 1000 is proposed. The total numbers of data accessing points will be $N=3\times\sqrt[3]{Y}+1$, which is 31 for 1000 switches by the 3D novel design, the scanning time is reduced up to 30% (The scanning speed is also increased by 3 times) thanks to the great reduction of lines for 3D scanning, in stead of 2D scanning. The property comparison among 1D, 2D, and 3D architectures is listed in Table 1. As the optical switch number increases, a higher order circuit can effectively reduce the pad number. Secondly, the shape and amplitude of the driving signal can be optimized to increase the speed of the response with low driving powers. In this research the focus is on optimizing the driving signal, since the materials choice and geometry are in most cases optimized or a compromise was made with other design issues. The amplitude and the shape of the driving current determine the speed and the magnitude of the heating. The application of a larger current will enhance the generated heat and therefore the increase in temperature, but this will also take more time. Furthermore, the final resulting modulation will not be perfectly linear with the power, because the resonance series pulse that is used for the modulation can only be locally approximated by a linear function. Note that this also depends on the modulation frequency, i.e. the pulse width of the current. The shape of the driving signal is also of great importance.

An filter PLC based on microrings(MRs) [5] with radii in the order of tens of micrometers, however, allows for extremely small-area devices. Due to the highly selective MR filter characteristic, a minimum component implementation of a four-channel filter PLC controller can already be realized with four MRs while additional switching functionality is easily implemented [6].

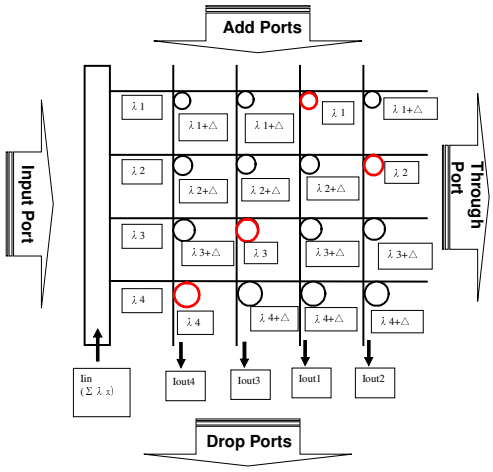

Figure 1 Schematic of a four-channel filter PLC

The first column of Figure 1 shows such an implementation where each MR drops an incoming channel λx to one of the outputs Ioutx when its resonance frequency corresponds to that of the incoming channel. In this paper, the design, fabrication, and measurements performed on a four-channel thermally tunable MR-based filter PLC controller are presented.

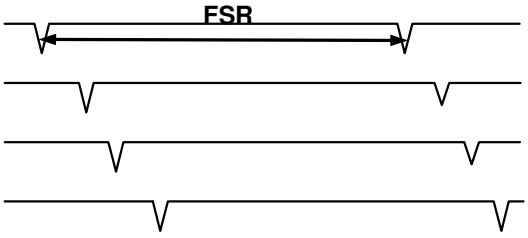

Figure 2 Principle of tuning wavelength

By thermal optic effect processes the effective index can be varied resulting in a shift of the resonance wavelengths, by an amount of △λ. This shift can be used in filter applications to tune the passband to the desired wavelength. Also statistical errors in the radius during fabrication can be cancelled by post deposition trimming. The principle of tuning is shown in Figure 2. The same phenomenon can lead to an additional function when operating at constant wavelength λsource. By a small change in effective index around the steep flank of the MR response a modulation at λsource with a high extinction ratio can be obtained. A relationship between the radius of the ring R, the effective group index n_g, and the FSR is given by the formula: $FSR = \frac{\lambda^2}{2\pi R n_g}$, where λ is wavelength[7-9].

III. Design of Controller Chip

This is the largest number of integrated switches yet achieved in a waveguide-type switch. We have already designed and made a 16×28 matrix switch controller modules. The Y×Y matrix switch module requires Y^2 electrical terminals to feed switching power to each cross-point individually. 448 terminals will be needed in the 16×28 matrix switch controller module. Since such a large number of terminals makes the module structure complicated, we developed 16×28 matrix switch controller module with a driving circuit that has a serial/parallel control signal conversion function, as shown in Figure 3. As a result, we were able to reduce the number of electrical terminals to 5 control terminals and 1 power supply terminals.

The general strategy that we employ is to integrate all relatively small-signal electronic functions into one ASIC to minimize the total number of the components. Three lines are employed to control the heating of one microring, including voltage, shift register, and data line, the relationship of waveform is shown in Figure 4. Each heater resistor requires a voltage line for the driving current flow and shares the same ground with the other resistors. The resistors are individually addressable to provide unconstraint signal permutations by a serial data stream fed from the controller. The shift register is employed to shift a token bit from one group to another through AND gates to power the switch of a microring group. The selection of a ring is thus a combination selection of the shift register for the group and the data for the specific ring.

Such an arrangement allows encoding one data line from the controller to provide data to all of the ring s, permitting high-speed printing by shortening the ring selection path and low IC fabrication cost from the greater reduction of circuit component numbers.

Table 1 Performance comparison among 1D, 2D, and 3D driving schemes.

X :Pads 、Y :Switches	X~Y+1	X=2× $\sqrt[2]{Y}$ + 1	X=3× $\sqrt[3]{Y}$ +1 (X : Connection lines ,Y :Switches)
Switches	1000	1024	1000
Ring resistors	1000	1024	1000
Interconnect Pad	1001	65	31

In the proposed novel 3D design, different from the 2D one, as shown in Figure 3, the digital driver includes a clock-control circuit, a serial/parallel-conversion circuit, a latch circuit, a level shifter, a D/A converter comprised of a decoder, and an output buffer comprised of an operation amplifier . The D/A converter receives a gray-scale reference voltage from an external source. The clock-control circuit receives control signals from an external control circuit. Based on the received control signals, the clock-control circuit attends to control of the latch circuit, the D/A converter, and the output buffer by using a latch-control signal. The received optical data information needs to be converted into data at an optimal transfer rate (frequency) in order to conform to the ring characteristics. To this end, the clock-control circuit divides the 8-bit optical packet switching signals supplied to the data driver, as shown in Figure 4, with an aim of lowing the operation frequency. The serial/parallel-conversion circuit converts serial signals of a plurality of channels into parallel signals, and supplies the parallel signals to the latch circuit. The latch circuit temporarily stores therein the received parallel signals, and supplies same to the level shifter and the D/A converter at predetermined timings. The level shifter converts a logic level ranging approximately from 3.5 V to 5 V into a thin-film heater voltage level that ranges from 7.5V to 8.5V for various heater resistors as a result of variation processing conditions.

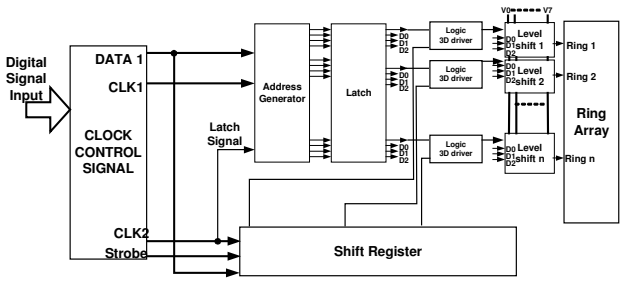

Figure 3 A microing switch controller module block diagram

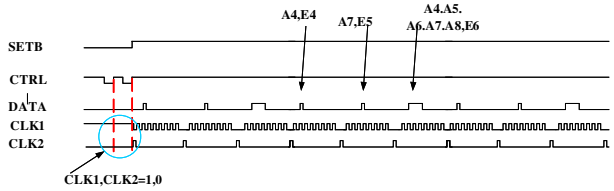

Figure 4 Input waveform of controller

In the signal flow design, optical switches are usually scanned over one by one without jumping on un-activity switches. As a result, for the optical packet switching chip with 450 optical switches, a 1, 2 or 3 dimensional circuit architect will needs 450, 36, and 5 unit times for scanning over all of the switches. Therefore, the scanning time of the 3D multiplexing circuit from the first address line to the 16th, as an example, takes only 5 units of clock time from the simulation result, much faster than that of the 2D configuration with 16 units of clock time. Thus the maximum scanning time for the 3D circuit will be reduced to 30% of that in the 2D case.

To simultaneously write signals into the driving circuit, multiplexing data latches and shift registers are employed by the application of commercial available CMOS ICs. Small numbers of shift registers, control logics, and driving circuits can be electrically connected and integrated with optical packet switching chip using standard CMOS processes. Figure 5 Driving circuit of three-dimensional architect. The desired signal for S selections and A selections can be pre-registered and latched in the circuit for one time writing.

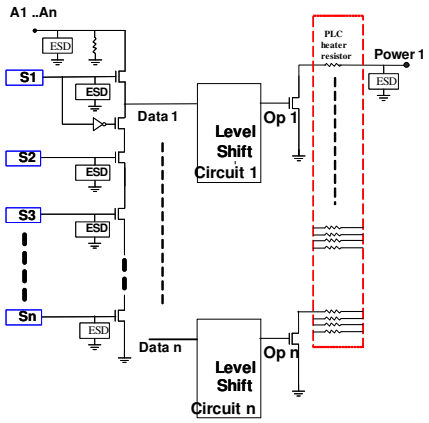

Figure 5 Driving circuit of three-dimensional architect.

By applying an widen the heating pulse width can be made faster. This means that at the start of the driving pulse, a higher current than is needed for the desired steady-state temperature is shortly applied. Just before the desired temperature is reached, the current is changed to a level that results in the desired temperature. So far, only the possibility of speeding up the heating of the material is discussed. Optimize driving signal frequency modulation is shown in Figure 6, according to shift the mount of the shift in center wavelength of the ring λc. A modulating signal was applied to the heater. We designed the driving signal frequency modulation waveform for one ring OP52, this output ring OP52 signal is from A4(Addressing line) AND E4(Enable line). Different waveform sharp applied to thin-film heater

change temperature. By thermal optic effect processes the effective index can be varied resulting in a shift of the resonance wavelengths, by an amount of △λ. The waveform in Figure 6 is optimized because the output signal OP52 will be adjusted by CFD Simulated frequency modulation to attain steady state temperature of variation within 0.1°C.

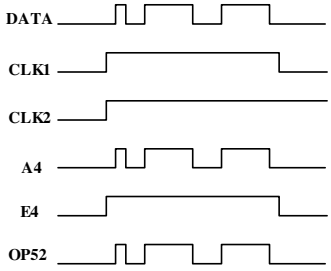

Figure 6 Driving signal frequency modulation

IV. Experimental and Results

By using a Commercial Finite Difference Solver for thermo-optical problems the temperature profile of the used layer stack can be simulated and also the change in refractive index of the layers induced by the temperature rise. Figure 7 shows such a temperature profile of the layer stack mentioned before. Not only design the ASIC 3D multiplexing controller chip of the resistors are individually addressable to provide unconstraint signal permutations by a serial data stream fed from the controller but also according to the Commercial Finite Difference Solver simulation result, optimize driving signal frequency modulation as shown in Figure 8.

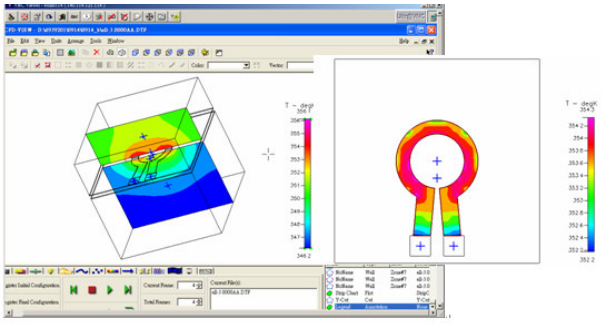

Figure 7 Simulated temperature profile of a cross section with 5μm heater ring width and 2μm cladding

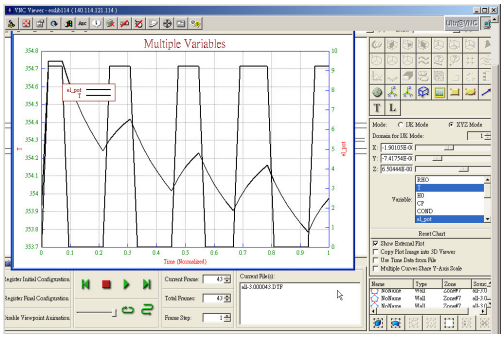

Figure 8 Driving signal frequency modulation for heat

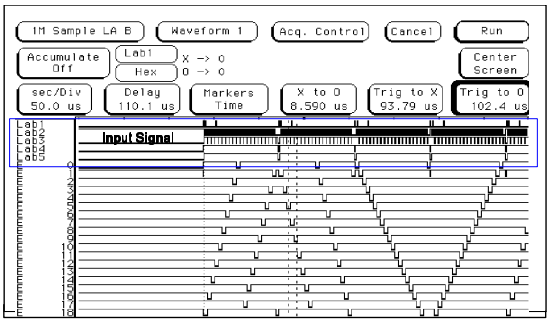

Figure 9 FPGA verify result

In the Logic Analysis, the relationship between the ASIC input and output is shown in figure 9. The input signals include DATA (signal for selected switch action), CLK1(signal to scan DATA signal), CLK2(signal to latch DATA signal), CTRL(signal to select enable type), as well as SETB(the time sequence to set up CTRL), and the output signals match the designed ASIC signals very well.

The testing result of the IC demonstrated the scanning of 125 switches takes 60.5 μs for 2D circuit architect while 20.5 μs for the 3D one, representing a time saving of 40μs or a 67% time reduction. This result is very close to the simulation one of the IC. In the Logic Analysis equipment, we observe the ASIC input and output relationship. The input signal include "DATA、CLK1、CLK2、CTRL、SETB" and output signal is match ASIC design waveform. The ASIC design and logic analysis result is matched. From the verify measurement, Investigations of the logic signal process in the chip show that addressing the heating element exactly and starts heating. The measured results verify the scan speed by the 3D architecture is 34.4 μs faster than that by the 2D architecture with similar switch number. The settling time of 0.35μsec is also faster in the 3D case than that of 0.5μsec in the 2D architecture.

The SPICE simulation result on the relationship of input and output signal at 5μs clock time. Figure 10 demonstrates that not only the switch speed is higher by the level shift device than that of one without level shift circuit, but also the voltage has been enhanced to 5V. An adjustable voltage pulse from 7.98V to 8.02V is applied to the various heater resistors thanks to the processing condition.

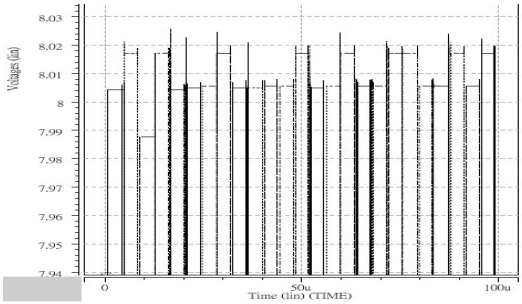

Figure 10 Transient simulation of the input and output signals of the level shift device

The cooling down of the structure is equally important, though. Enhancing the speed of the cooling down process might be done by active cooling, but this would require major adaptations to the device and the low cost low power principle would not hold anymore. A much easier way to do this is biasing. In biasing, a DC-current is applied, that will result in

a relatively small change in temperature, refractive index and therefore resonance wavelength. To heat the device, the wide pulse width signal or high level voltage is applied, to cool it down, a narrow pulse width signal or low level voltage is applied. See Figure 10 for the simulated behavior of high and low bias driving. The maximum current that can be applied is limited, due to the destruction of the heaters at high powers. The use of a bias will therefore cause a smaller modulation depth, but the modulation will be faster, since the time needed for cooling down is reduced.

Figure 11 is a chip photograph of a fabricated 16×28 matrix switch controller module. In this module, the chip area is 2.5 ×2.5 mm and was fabricated by a two-poly four-metal (2P4M) 0.35μm twin-well CMOS technology (TSMC, Taiwan Semiconductor Manufacturing Company Ltd). Each transistor is surrounded by full guard ring for preventing electrostatic shock. The testing result of the IC showing in Fig.14 demonstrated the scanning of 450 ring switches takes 60.5 μs for 2D circuit architect while 20.5 μs for the 3D one, representing a time saving of 40 μs or a 67% time reduction.

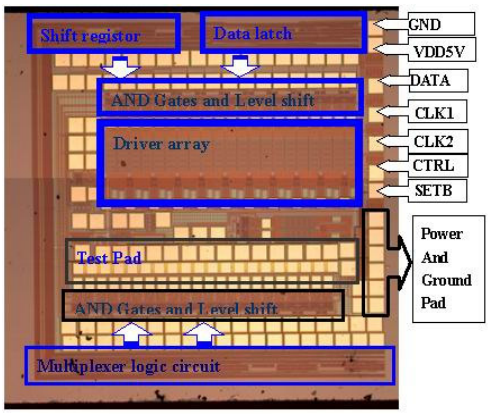

Figure 11 Chip photograph

From Figure 2 shows the tuning characteristics of the single ring resonator. The injection current of ring was changed from 0 to several mA, the injection current and switching time will be consider. Single driver module performance is shown in figure 12 and figure 13, fast and stable switching was observed by the current injection. The switching time was 2.5 ns. While the driver gate of 2V, we obtain the injection current is 40mA, and threshold voltage is 1.0V.

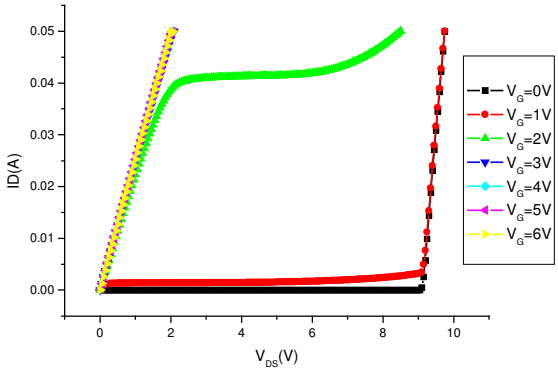

Figure 12 I-V Curve for the CMOS driver.

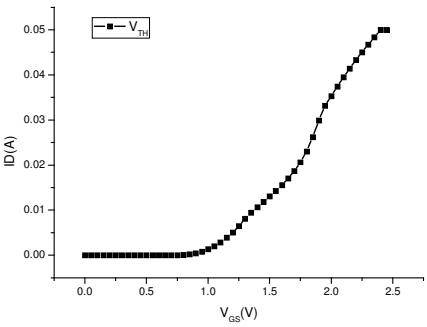

Figure 13 Gate threshold voltage

The measurement shown in Figure 14. Shows the result that we have demonstrated a high-speed tunable optical filter using semiconductor ring resonator controller. The device shows total FSR of 1.5 nm. The switching time of the device is 2.5 ns. This is the first time a high-speed tunable optical filter has been fabricated using a semiconductor ring resonator controller.

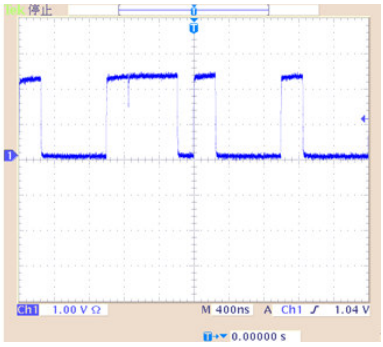

Figure 14 Measure result of output terminal OPn

The measurement result of the use of a bias in the driving signal. Now an overshoot has been applied on the falling slope as well. It can be seen that not only the rising slope is steeper than the normal response, but the falling slope as well. The modulation depth in this measurement is somewhat reduced, since the steady-state values for high and low were chosen the same, to investigate only the effect of the overshoot and bias on the slope behavior. By using the optimized driving signals, modulation frequencies up to 10 kHz were measured, resulting in thermal switching speeds in the order of 0.1 ms.

It should also be pointed out that we have realized an attenuation function. This is because we designed this module so that we can supply an arbitrary switching power independently to each switching unit. The attenuation function makes it possible for us to flatten the optical output power level even if the optical input power level fluctuates.

It should also be noted here that the control signals are used to determine the switching unit and the timing of the ON or OFF switching, not to determine the power applied to the switching unit. The heater power that should be applied to each switching unit for complete switching or attenuation must be measured and stored in advance.

Figure 15 is shown the measurement of shifted in center wavelength of the ring function block, include light source, 1-to-8 core measurement PLC chip platform, optical switch, optical power meters, and Acousto-optic Spectrum Analyzer. We obtained the shift in center wavelength of the ring λc with optic Spectrum Analyzer.

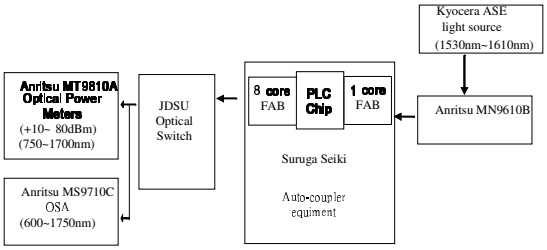

Figure 15 Measurement of shifted in center wavelength of the ring function block

Figure 16 shows a photograph of the pigtailed and PLC based on Microrings. The PLC device is butt-coupled to standard single-mode fibers. Since the optical mode of this fiber does not match the mode of the channel waveguide, losses will be considered. The change in effective refractive index induced by the heater depends largely on the materials used and the distance between the heater and ring.

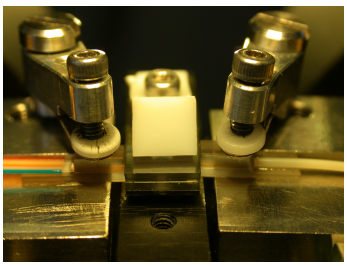

Figure 16 Picture of pigtailed and PLC based on Microrings

Although being most likely the simplest to be implemented, the thermal optic effect suffers from being slow with a response in the order of hundreds of microseconds. For switching applications this can be sufficient but for modulation other effects must be used. The thermo-optic effect can be used by applying a thin film heater on top of the ring. The heater must be placed as close as possible to the ring to minimize the driving power. On the other hand a minimum distance has to be preserved in order to avoid large additional losses inside the ring due to the presence of the absorbing heater metal. The shift in center wavelength of the ring λc is a function of the difference in effective index induced by heating the device, according to:

$$\delta\lambda c = \frac{\lambda \Delta Neff}{Neff}$$

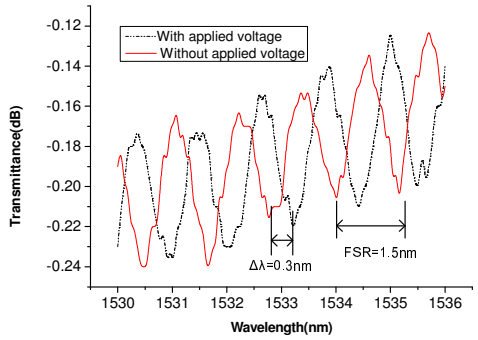

Figure 17 Transmission spectrum of rings resonator

The resonant spectrum was shown in Figure 17. In this case the center of the rings filter are slightly shifted with respect to the signal wavelength. We measured value of FSR=1.5nm, and a wavelength of λ=1534nm, the shift in center wavelength of the ring λc=0.3nm.

V. Conclusion

The next generation of optical networking requires optical parts with complex functionality that are smaller and cheaper than ever before. We successfully fabricated a silica-based 16× 28 PLC-SW controller module in which we incorporated a switch chip based on PLC technology and new driving circuits with a serial-to-parallel control signal conversion function. The new driving circuits significantly reduced the number of control terminals, and enabled us to realize a simple module structure suitable for use as a large-scale switch. The module exhibited excellent levels of performance, about enhancement of the number and array density of switch within an optical packet switching chip is one of the keys to raise the throughput. A signal was applied to the thin-film heater. The wavelength of the incoming light source is chosen such that it is placed on the slope of the resonator response. In biasing, a DC-current is applied, that will result in a relatively small change in temperature, refractive index and therefore resonance wavelength. To heat the device, the modulating signal is applied, the simulated behavior of modulating signal driving. We also obtained the value of FSR=1.5nm, and a wavelength of λ=1534nm, the shift in center wavelength of the ring λc=0.3nm. Since standard technologies are used and mass-production is feasible also here the multi microrings structure have a great potential. Although the need for very complex, density integrated functions, might be a little too complicated and unnecessary for this application in the near future.

Acknowledgment

Authors would like to thank the Chip Implementation Center (CIC), TSMC, Taiwan, for organizing the chip fabrication.

References

[1] C. A. Brackett, et. al., “A Scalable Multiwavelength Multihop Optical Network: A Proposal for Research on All-Optical Networks”, J.Lightwave Technol., vol. 11, 736-753, 1993.

[2] K. Okamoto, K. Takiguchi and Y. Ohmori, “16-channel optical add/drop multiplexer using silica-based arrayed-waveguide gratings”, Electron. Lett., vol. 31, pp. 723-724, 1995.

[3] H. Li, C. Lee, W. Lin, L.S. Didde, Y. J. Chen and D. Stone, “8-wavelength photonics integrated 2x2 WDM cross-connect switch using 2xN phased-array waveguide grating (PAWG) multi/demultiplexers”, Electron. Lett., vol. 33, pp. 592-594, 1997.

[4] C. R. Doerr, et. al., “40-wavelength add-drop filter”, IEEE photon. Technol. Lett., vol. 11, pp. 1437-1439, 1999.

[5] J.E. Ford, V. Aksyun, D. Bishop and J. Walker, “Wavelength add-dropswitching using tilting mirrors”, J. Lightwave Technol., vol. 17, pp. 904-911, May 1999.

[6] C. Pu, L. Lin, E. Goldstein and R. Tkach, “Client-configurable eight channel optical add/drop multiplexer using micromachining technology”, IEEE photon. Technol. Lett., vol. 12, pp. 1665-1667, Dec.2000.

[7] N. A. Riza and S. Yuan, “Reconfigurable wavelength add-drop filtering based on a Banyan network topology and ferroelectric liquid crystal fiber-optic switches”, J. Lightwave Technol., vol. 17, pp. 1575-1584, Sept. 1999.

[8] Wenhua Lin, Haifeng Li, Y. J. Chen, M Dagenais and D. Stone, “Novel Dual-Channel-Spacing WDM Multi/Demultiplexers Based on Phased-Array Waveguide Grating”, Photonics Tech. Lett. 8, 1501 (1996)

[9] B. E. Little, S. T. Chu, W. Pan, and Y. Kokubun. Microring resonator arrays for VLSI photonics. IEEE Photonics Technol. Lett., 12:323–325, 2000.