A Simple Digital VHDL QPSK Modulator Designed Using CPLD/FPGAs for Biomedical Devices Applications

Gihad Elamary, Graeme Chester, Jeffrey Neasham

Abstract— we proposed a new simple design for a Quadrature Phase shift Keying (QPSK) modulator applied for implantable telemetry applications as demonstrated. VHDL programming code is used to generate QPSK digital signal. The input test signals data and carrier are interfaced to the CPLD and FPGAs board from Agilent function generator (E8408A). We used the local clock oscillator for test, which is operating at 25.175 MHz and used 12.5MHz for the carrier and 2Mbps reduced for data source. The modeled Modulator has been designed and simulated and performance was evaluated by measurements. The design has low power consumption and size for biomedical applications. Furthermore, the advantages of this modulator are it can be reconfigured and upgraded to enhance the data rate.

Index Terms—VHDL Modulator (QPSK); Biodevices,Passive filter, CPLD/FPGA.

I. INTRODUCTION

Biomedical implant telemetry devices are increasingly applied today in various areas in medical applications, such as telemedicine, biotelemetry, and health medical care treatments for chronic diseases epilepsy and blindness patients; which are using wireless infrastructure environment [1]. The biodevices are one of these technologies applied with transcutaneous wireless implant telemetry (TWIT).Wireless inductive coupling link is common way for transfer the RF power and data to communicate between readers and a battery-less implant [2, 3]. Demand for higher data rate for the acquisition data returned from the body are increasing, and require an efficient modulator to achieve high transfer rate and low power consumption. In such applications QPSK modulation has advantages over other schemes, and double symbol rate with respect to the BPSK over the same spectrum band. Contrast to analogue modulators for generating QPSK signals, where the circuit complexity and power dissipation

Manuscript received March 23, 2009; (revised April 28, 2009). This work was supported in part by School of Electrical, Electronic and Computer Engineering (EECE). Newcastle University /UK.

The authors are with Department of EECE, Newcastle University (e-mail: <u>gihad.elamaryl@ncl.ac.uk;</u> <u>Graeme.chster@ncl.ac.uk</u> ; <u>j.a.neasham@ncl.ac.uk</u>). School of EECE- Merz Court, Newcastle upon Tyne – Newcastle University-NE1 7RU are unsuitable for medical purposes, this type of modulator provides digital synthesis and the flexibility to reconfigure and upgrade with two most often languages used VHDL-and-Verilog (IEEE standard) based as hardware structures language described [6, 7, 14, 15].

II. METHOD MODULATOR DESIGN

All analogue or hybrid analogue/digital QPSK modulators work with phase shift carrier angle (φ), as a key of modulation [4, 16]. The phase signal is most important part in the modulator to acquire two discrete signals (Sine and Cosine) [21]. Practically, it use Direct Digital Synthesizer (DDS) or Numerical Control Oscillator (NCO) for perform the carrier transitions [11, 12, 17]. However, the NRZ format is essential for mapping *I* and *Q*. The analogue QPSK signal can be represented mathematically as in Equation (1) and I/Q are defined in Equations (2, 3):

$$QPSK(t) = I(t)\cos(2\pi f_c t) - Q(t)\sin(2\pi f_c t)$$
(1)

$$I = \sqrt{\frac{2E}{T}} \cos[(2i-1)^{\frac{\pi}{4}}]$$
(2)

$$Q = \sqrt{\frac{2E}{T}} \sin[(2i-1)\frac{\pi}{4}]$$
(3)

These types of technique are not suitable for medical applications, which essential work with the input data in NRZ signal form at conventional modulators. The proposed QPSK VHDL modulator is programmed generate a carrier phase which acquires four discrete states (0, 90,180,270). Two separate streams in-phase 'I', and quadrature phase Q for mapping the data for controlling the four phase different carriers interfaced to multiplexer. The output is selected by multiplexer to provide a digital QPSK signal, which passes via a passive filter before a transmission (TX) to eliminate the high frequencies [9, 13]. Fig.1 demonstrates the proposed VHDL modulator comparing to analogue modulator. The digital QPSK signal of the multiplexer output can be represented in Equation (4):

$$Mux_{out} = I Q \cdot C_0 + I Q \cdot C_{90} + I Q \cdot I C_{180} + I Q \cdot C_{270}$$
(4)



Figure 1. The block diagram for the proposed QPSK Modulator

III. FILTER DESIGN AND SIMULATION

In wireless transmission we cannot transmit the digital signal directly without harmonics separation. The output of the multiplier is producing a QPSK digital signal "square signal" form. It is essential to use a filter to complete the process for the modulator "off-chip". We designed an analogue passive filter for this purpose as it has zero power consumption. Two types of filters were investigated Low pass Filter (LPF) and Band Pass Filter (BPF) [5, 10,18], as appropriate for medical purpose the Butterworth LPF was given enhanced performance than other types of LP-filters, to eliminates the harmonics from the QPSK digital signal. While the second choice was the Chebyshev II Filter BPF this was observed to give better performance then other types of BP-filters. As demonstrated in Fig.2 and Equation (5).



Figure 2. The filters types used for harmonics eliminates

$$H(jw) = \frac{S_{QPSK}(jw)}{Mux_{out}(jw)}$$
(5)

A. Butterworth LPF design and simulation

Our prototype analogue filter selected is a Butterworth 4th order to filter the input QPSK digital signal. The transfer function of LC filter can be represented in Equation (6). The simulation is presented in Fig. 3; with MATLAB/Simulink

clearly it demonstrates the response of filter comparing to the Butterworth and Chebyshev I. Practically, a simple BW-LPF is designed to omit the harmonies and DC component. The size is implant where the filter is implanted with the modulator in biomedical devices.



Figure 3. The LPF simulation with MATLAB/Simulink

$$H(s) = \frac{1}{S^{2}LC_{2} + SRC_{2} + \frac{C_{2}}{C_{1}} + 1}$$
(6)

B. Chebyshev II HPF design and simulation

The second prototype choice filter is Chebyshev II analogue passive LC filter 5th order. The multiplexer output signal is fed into the designed filter. The simulation result with MATLAB/Simulink FFT is presented in Fig. 4. Which compares the Chebyshev I, Chebyshev II and Elliptic for performances type and characteristics. Obviously it gives a high separation, over 50dB.



Figure 4. The BPF simulation with MATLAB/Simulink

The simulation performances for other types of filters are presented in Table I as: (A) best performance (B) is less performance and (C) weak performance, and (NP) is Not Perfect performance.

TABLE I. Influence of the investigation filters simulation

| | Filter Types | | | | |
|-----|--------------|---------|----------|----------|--------|
| | Butterworth | Cheby I | Cheby II | Elliptic | Bessel |
| LPF | А | В | NP | С | NP |
| BPF | NP | NP | А | С | В |

IV. LE SIMULATION

A.MATLAB/Simulink simulation

The QPSK modulator was designed and simulated with MATLAB/Simulink to verify and validate the modulator specifications [19]. The modulator is consists of carrier source to produce a periodic pulse signal ($_{f_{\it carrier}}\,$), fed to a carrier phase shifter; which shift the input carrier into four different phase signals (0°, 90°, 180°, 270°) interfaced to multiplexer. While the data source was generated with PN_sugance, fed to data mapping to generate I and Q signals to influence the four phase different carries. The output is selected by multiplexer which provides digital QPSK signal, this signal filtered with analogue filter before transmitted to pass fundamental frequency ($f_o \pm data$) and eliminates the higher frequencies associated with the square signal. The architecture block diagram of Tx_Mod is shown in Fig .6. The simulated random data signal (Data_in) which is generated by a PN sequence can be represented by Fourier series analysis as in Equation (6).

$$PN(t) = \sum_{n=-\infty}^{\infty} c_n p(t - nT_c)$$
(6)

Where the input carrier signal is a periodic pulse train signal and mathematically expressed by the Fourier series as in Equation (7).

Carrier
$$(t) = \frac{4}{\pi} \sum_{n=1}^{\infty} \frac{\sin((2n-1)w_c t)}{(2n-1)}$$
 (7)

The Tx and the Rx signals are presented in Fig. 5 shows the spectrum of the transmitted RF signal (CH1) and the received RF signal (CH2) in the presence of noise (AWGN).







Figure 6. The propoused Modulator with Mathlab /simulink daigram



Figure 7. The propoused Modulator with Mathlab /simulink daigra

B. VHDL programming code simulation

The proposed modulator was built by the Altera UP2 development kit board [8], Programmed with the VHDL language for modeling, design and analysis of the proposed QPSK modulator. The simulated result of this modulator is presented in Fig.7. This demonstrates the output signals waveforms indicating the transitions (180°, 270°) of the carrier signal influence by input data signal. The carrier frequency 12.5 MHz was generated from the local clock signal on the board, which operates at 25.175 MHz. The data signal was reduced to 2 MHz by a frequency divider then fed into a random PN_sequence generator (behavioral described).The modulator was implemented and comparing two different designs structural and behavior descriptions; for efficient performance. The generated VHDL "Behavioral" block diagram of the QPSK modulator is illustrated in Fig. 8

V. Experimental results and discussion

In this part of paper, we provide the measurements which were conducted using the Altera UP2 Development kit board, for testing the VHDL code modulator and comparing the performance with the simulated QPSK modulation. The Agilent digital demodulator (E8408A VXI) is used to receive the filtered RF QPSK signal, and analyzed the parameters of the transmitted QPSK signal (Tx) as demonstrated in Fig. 9 [22]. The desired carrier signal was generated from the master clock on the circuit board that operates at 25.175 MHz, using 12.5 MHz as carrier. The carrier phase acquires four discrete states $(0, \pi/2, \pi, 3\pi/2)$ This corresponds to mapping I and Q data source generated with VHDL code inside the CPLD/FPGAs at 2Mbps. The signal passes as digital QPSK through the passive LPF for harmonics separation.



Figure 8. The porporsed VHDL modulator

Figure 9. Illustrated the setup Lab measurement withUK2 Alter

We investigated two prototypes of filters in this paper, LPF and BPF. The BPF has a better performance characteristic then LPF. However, the measurement result was illustrated in Fig. 10 as; (a) PN_code signal generated by VHDL code, (b) the QPSK digital signal, (c) the filtered signal output. While the spectrum of Tx signal was captured with signal analyzer in Agilent (8408A) at center frequency 12.58MHz as demonstrated in Fig 11. The demodulator is also constructed using the Matlab/Simulink tools to examine the performance of the proposed modulator. The performance has measured using Agilent Education version to demodulate the received signal "QPSK Demodulator" to demodulate the information data, which was transmitted with VHDL modulator. The measurement results are given respectively in Fig .12, the constellation diagram for QPSK Rx signal, and Fig.13 illustrating the spectrum and the demodulated data at 2Mbps. Ultimately, the whole bench test system is illustrated in Fig .14



Figure 10. Measured QPSK digital siganl (a); PN-code ;(b)Digital signal (c) filter signal throgh LPF



Figure 11. The Tx Spectrum of the QPSK transmitted signal at carrier 12.5MH



Figure 12. Constellation diagram of QPSK demoulator received from proposed QPSK modulator



Figure 13. Spectrum of the QPSK deomulator recivced signal from proposed QPSK mod at carrier (12.58Mhz), data (2Mbps)



Figure 14. Illustrates the test bench Lab measurement for transmit data over wireless inductive link using Agilent demodulator

VI. CONCLUSION

We implemented a new simple direct QPSK digital modulator model in MATLAB/Simulink environment. It has been successfully designed with VHDL programming code by Altera development kit. The modulator generate QPSK signal directly from binary digital data. For test purpose it was generated with VHDL code inside the CPLD/FPGA, mapped for I/Q to control the carrier signal using VHDL multiplexer code. The output producing modulated digital signal, filtered to transmit through designed filters (LPF/BPF). Experimentally measurements were presented at carrier frequency 12.50 MHz; and data rate 2Mbps. Which presents better performance with high data rate and carrier suppression about ~ 40dB. The filter is main key in the design, eventually we designed and simulated for optimum passive filter for implant part, and comparing to the better filter performances. However, the simulation results given the better performance if we selected the BPF Chebyshev I & II types, comparing to others. On other hand the Butterworth LPF type gave optimum performance. The disadvantage of digital filter is it needs higher sampling frequencies which increase the consumption power and size. These are not considering in this work. Furthermore, additional work was done to test the proposed modulator over wireless inductive coupling, which gave better received data wirelessly up to 3Mbps over distance about 9.5cm. Eventually this technique can offer high transfer rate for biomedical devices requiring a high demand rate, such as electrodes information measured in real time, where the acquisitions data from electrodes are increasing form the neural system. Ultimately, in future work, it is also an intention to up-convert the signal into an ISM unlicensed frequency in UHF band (402~ 405 MHz). For biomedical telemetry applications, increasing the data rate with low noise and size reduced.

REFERENCES

- K.Wise, D.Anderson, J.Hetke, R.Kipke, K.Najafi "Wireless implantable Microsystems High density Electronics interfaces to the nervous system"IEEE, Proceeding, Vol.92, pp. 76-97, 2004.
- [2] Ghazi Ben Hmida, Mhommed Dhieb, Hamadi Gharinai, Mounir Samet "Transcutaneous Power and High Data Rata Transmission For Biomedical Implants" 2006 IEEE.
- [3] S.Atluri, M.Ghovanloo "Digital of wideband power efficiency inductive wireless link for implantable biomedical using multiple carriers" Internal conference EMBS on neural engineering. IEEE, 2005
- [4] A. M. El-Gabaly, B. R. Jackson and C. E. Saavedra, "An L-Band Direct-Digital QPSK Modulator in CMOS," IEEE International Symposium on Signals, Systems and Electronics, Montreal, Quebec, Canada, April 2007.
- [5] B.Williams and Fred.J.Taylor, "Electronic Filter Design Handbook," by the McGarw-Hill companies, vol. III, G. T. Rado and H. Suhl, Eds. USA: 2006, pp. 89–137,pp.165-239.
- [6] G.C.Cardarilli, R. A.Del Re.RE, L.Simone Nicol, "Otimized QPSK Modulaator for DVB-S Applications," ISCAS 2006 IEEE.
- [7] Douglas.L.Perry "VHDL Programming by Example" Mc.Grawh. USA: Academic 2002, pp. 842- 868
- [8] <u>www.altera.com/literature/univ/upds.pdf</u>.(UP2 edicational board datasheet).
- [9] Roger.Lipsett,Carl.Schaefer, Cary.Ussery "VHDL Hardware Description and design" pp842-868
- [10] H.Bochnick, W.Anheier "FIR filter design using Verilog and VHDL". Italy April. 16-26.1993

- [11] He.Jin,He.Song.Ben "Design and Realization on NCO of modulator based on FPGA "IEEE, communication Circuit and system ICCCAS 11-13.july .2007, pp 831-833.
- [12] J.Goncalves, J.R.Fernandes, M.MSilva "A Reconfigurable Quadrature Oscillator Based on a Dirct Digital Synthesis System" DCIS, 2006
- [13] M.Kovac, J.kolouch "BPSK, QPSK MODULATOR SIMULATION MODUEL"2004
- [14] E.Normark,Lei.Yang,C.Wakayama,P.Nikitin,R,Shi "VHDL –AMS Beahvioral Modeling and simulation of api/4DQPSK transceiver system"
- [15] <u>http://ieeexplore.ieee.org/iel5/7180/19335/00893288.pdf</u>("IEEE standred VHDL Language Reference Manual"
- [16] <u>http://www.complextoreal.com/chapters/mod1.pdf</u>, (Intuititive giude to the principles communication)
- [17] I.Janiszwski, B.H.Meuth "Numerically controlled oscillators with Hybrid function generators "IEEE transction on ultrasonics, Vol, 49, No.7, July 2002
- [18] T.J.Kazmierski,F.A.Hamid "Architectural and parametric optimization of low-pass RF anloge Filter in VHDL – AMS based high level synthsis "BMAS2004,San Jose,20-22 oct2004-2.
- [19] http://www.mathworks.co.uk/support/. (Matlab / Simulink sources)
- [20] <u>www.analog.com/.../archives/38-08/dds.html</u> (Data sheet of Direct Digital Synthesiser form analog devices)
- [21] <u>http://www.home.agilent.com/agilent/product</u>. (Digital modulator / demodualtor Agilent E8408A VXI)