Evidence of Dot-size Variation in Nanowire Silicon Transistor

Yue-Min Wan, Kuo-Dong Huang, Shu-Fen Hu and Chin Lung Sun

Abstract—We report measurements of electrical transport in a nanowire transistor over a broad temperature range. The results suggest that quantum dot can varies its size and it will follow a simple scaling law. As demonstrated in the specific experiment of using polycrystalline nanowire transistor at T=180K, the dot size is $(8nm)^3$ and the principle gap ΔE is n=2 state, it is then increase to ~ $(16nm)^3$ at 60 K. The derivation is based on ΔE which is originally ~ 7 meV and then reduces to ~ 1.5 meV for a bigger volume. At 4.2 K, electron trapping becomes evident to make tunnel irreversible in current-voltage (*I-V*) characteristics.

Index Terms-Nanowire, transistor, dot-size variation.

I. INTRODUCTION

Quantum dot (QD) single-electron transistors (RTSET) [1-4] have recently become an important topic in high temperature applications for next generation electronics. The idea is to arrange a side gate near an electrical island to regulate its energy levels [5-7] and its resulting current-voltage (I-V) characteristics. Previous studies [8-9] have found that resonance tunnel is an essential character in deciding how much energy is required in order to add an electron into the central dot. And when that electron is discharged from the dot, the resonance is therefore creating a current peak. Quantitatively, such dynamics involves a charging energy of $Ec = e^2/2C$ (C is dot capacitance) plus a subband gap ΔE near the Ec that is known to be the resonance state En, as denoted by an integer number n. Experimentally, decision of Ec is easy cab be fairly robust by measuring the distance between two neighboring peaks. In contrast, the ΔE is a lot more difficult to decide because it involves the interactions between electron and phonon [10], and between electron and electron [11]. As such, delicate measurements are required in order to distinguishing them. To be explained in this article, we will demonstrate that for a nanowire

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Fig. 1(a) A schematic structure of nanowire transistor. It is made on a p-type silicon wafer. The gate oxide thickness is very thin at ~ 6 nm. Fig. 1(b) shows a scanning electron microscope picture of the device.

granular transistor that has a dot 8 nm³, Ec= 30meV at 180K, the most favorable states is n=2 and the ΔE is 7meV. At a lower temperature of 40K, the ΔE will reduce to 1.5me for a bigger dot of 16 nm³ thus suggestions [12-17] a governing law in the highly disorder system.

II. DEVICE FABRICATION

The nanowire transistor, as illustrated in Fig. 1(a), was fabricated on a p-type (100) silicon wafer [3]. First, a thin layer ~ 25 nm of polysilicon was deposited onto the substrate in a low pressure chemical vapor (LPCVD) of mixed gas using SiH₄. The sheet resistance was determined to ~ $30 \Omega/\Box$ and the PH₃ concentration was at ~ 1×10^{16} cm⁻³. With the technique of electron-beam lithography, granular wires of silicon were made. The typical size in grain was 4 ~ 8 nm as examined by transmission electron microscope (TEM) [4]. Point-contact junctions were then defined by the technique of proximity exposure and their size were controlled down to ~ $40 \times 25 \text{ nm}^2$. An oxide layer was coated on top by the method of rapid thermal annealing (RTA) at ~ 925 °C for 150 sec. The resulting thickness was at about 6 nm as checked by an ellipsometer in order to provide a good gate-dot coupling. In

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Fig. 2(a) First conductance maximum G_{max}/G_o and minimum G_{min}/G_o as a function of reduced temperature KT/Ec. Solid lines are the best fit. Figure 2(b) shows the drain current I_d as a function of the side gate bias V_g at $V_d = 10$ mV. Temperatures from top to bottom are 110, 100, 90, 80, 70, and 60 K in step of 10 K. Inset is the data from 50 to 10 K.

the end, polycrystalline silicon top gate (50 nm thick & ~ 300 nm wide) was then made to finish the device as shown in Fig. 1(b). Devices were loaded on a probe station in 100 mtorr. Their temperature was regulated in a helium bath and was also monitored by a carbon-glass thermometer that had an accuracy of 0.5 K. Transport measurements were carried out by Keithley 4200, which had 1μ V and 10 fA resolutions.

III. DATA ANALYSIS AND DISCUSSIONS

Fig. 2(a) plots the conductance of the first tunnel peak; G_{max} (scaled to $G_o = e^2/h$. represents the maximum value, G_{min} the minimal value and both are coming from the *I*-*V* in Fig. 2(b). Clearly the $G_{max}(T)$ displays three distinctive characters; first, at $T \ge 150$ K, it is dominated by a power law; second, in the middle range of 60 K $\le T \le 150$ K, it becomes 1/T to reach a peak. And, at T < 60 K, another power takes over, making it dropping to zero. According to the famous theory of linear-response for conductance [12], the 1/T peak indicates that there is a ΔE . Judging from the peak position, i.e, K_BT , it is ~ 7 meV.

$$E(n_x, n_y, n_z) = \frac{\pi^2 \hbar^2}{2m} \left(\frac{n_x^2}{W^2} + \frac{n_y^2}{H^2} + \frac{n_z^2}{L^2}\right)$$
(1)



Fig. 3 I_d versus V_d at V_g = 0 V for temperatures of 4.2, 10, 15, 30, 50, and 70 K, respectively. The arrow marks the Coulomb blockade threshold at 4.2 K. Inset shows the threshold $\pm V_c(T)$ and an exponential fit Ae^{-KT/\DeltaE} with A = 50 mV and $\Delta E = 1.5$ meV.

Since electron tunnel is a result of quantum excitation, therefore, it can be used to derive the dot size. Suppose the quantization is occurring in an isotropic box WxHxL as described by Equation (1), then a scaling law, i.e, $En \propto 1/L^2$, would follow in nature. In the following text, we will prove such projection is correct. As we recall from our earlier study [3] that in 60 K \leq T \leq 250 K, the dot has a volume of ~ 8³ nm³ [3] and down to the temperature of 40 K, it increase to $\sim 16^3$ nm³ [20], thus showing as the first evidence that L is changeable. In that regard, the ΔE also has to change. In Fig. 3, we find evidence. Here, nonlinearity clearly dominates each curve showing that Coulomb blockade does exist and the $\pm V_c$ (see arrows) are used to mark such effect. When all the V_c are collected and best fitted by the formula exp $(-K_{\rm B}T/\Delta E)$ [21,22] as shown in the inset, the 40K ΔE is determined at ~ 1.5 meV. Notice that this value is about one-quarter of the old ΔE to support the law.

Another evidence is also discovered to support such principle. The size-increase obviously will modify the coupling scheme of the granular dots. As a consequence, charging is expected to be different. Assuming the resonance



Fig. 4 Spreading of charge carriers in the n = 2 state and the associated first energy gap. (a) illustrates the state in the smaller dot of ~ (8 nm)³ of ~ 180 K. (b) shows the expended state in a larger dot of ~ (16 nm)³ at T = 40 K. (c) to (d) shows the reduction of the gap.

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Fig. 5 I_d as a function of V_g at V_d = ± 16 mV, ± 12 mV and ± 8 mV, respectively. Peak splitting and irreversibility are evident in the positive and negative sweeps, suggesting that the nanowire is of highly disorder.

remains at the same $n_z = 2$, the charges will distribute a wider region, i.e, from 4(a) to 4(b). In fact, that is observed in helium temperature.

In Fig. 5, the data was taken at several Vd and it is evident that the peaks are different from Fig. 2(b). Namely, a major peak will split in several fine peaks (2 to 4) and shows that the coupling picture is correct [23]. Notice that, the peak's half-width is at about ~ 10meV which agrees the ΔE and also indicates extra grain is aligned to the gate direction by merging into the central dot for creating different conductance path. When the bias is reversed, the *I-V* shows a different path that is also known as the stochastic effect in granular material [24].

In the end, we estimate the tunnel rate of electron through the nanowire. At the peak of G_{max} the conductance is ~ 0.07G_o. This value also equals $e^2\rho\Gamma^l\Gamma^r/2(\Gamma^l+\Gamma^r)$ [12], where $\Gamma^l(\Gamma^r)$ is the tunneling rate through the left(right) barrier, ρ is the density of state at the junction $\infty \sim n^{2D}A$, A is area and n^{2D} equals $(n^e)^{2/3}$. Given $n^e \sim 10^{16}/cm^3$, $A=10^{-12}$ cm², $\Gamma^l=\Gamma^r$, and $I_d = n^e\Gamma \sim 10^{-9}$ A, the Γ calculated at the peak is 10^{-4} G_o/sec. By contrast, the rate at the G_{min} is found to be ~ 1x10⁻² G_o/sec.

$$G_{\min} = \frac{2e^2}{K_B T} \frac{\Gamma^{l} \Gamma^{r}}{\Gamma^{l} + \Gamma^{r}} \exp(-\frac{E_{act}}{KT})[1 + f(E^{-})]$$
(2)

This is obtained from equation (2), $f(E^{-})=1/2$ the Fermi function at the lower level E⁻ of the lifted degeneracy, and E_{act} = $\Delta E/2$ + Ec the thermal activation energy. As presented in Fig. 2(a), the best fit suggests that electron tunnel takes more time at G_{min} via diffusion [25].

IV. CONCLUSION

In conclusion, we have studied electron transport in polycrystalline nanowire transistor over a broad temperature range 4.2 K \leq T \leq 250. A major gap is identified to associate with the central dot. Size variation is demonstrated to be a governing principle in the disorder system. At 4.2 K, this rule leads to the effects of stochastic charging and irreversibility in current-voltage characteristics.

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