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Digital Control for Dynamic Performance Enhancement of DC-DC Switching Converters

Yan-Fei Liu

Abstract— **In this paper, an overview of recent advances in digital control of low- to medium-power dc-dc switching converters is presented. Traditionally, analog electronics methods have dominated in controlling such dc-dc converters. However, with the steadily decreasing cost of ICs, the feasibility of digitally controlled dc-dc switching converters has increased significantly. This paper outlines a sample of digital solutions for dc-dc switching converters to enhance the dynamic performance of dc-dc switching converters. Furthermore, latest research activities pertaining to applications for dynamic performance improvement, such as controller auto-tuning, capacitor charge balance control, are discussed. These applications demonstrate the significant advantages and potentials of digital control.**

Index Terms— **Digital control technologies, Dc-dc switching converter, Capacitor charge balance control, Auto-tuning**

I. INTRODUCTION

Over the past decade, digital control has emerged as a viable candidate for low- to medium-power dc-dc switching converters. With the steadily decreasing cost of digital ICs, the cost-prohibitive attribute of digital control technology has begun to fade. Therefore, over the past few years, research focus has shifted toward the unique advantages that digital control can offer to dc-dc switching power converters.

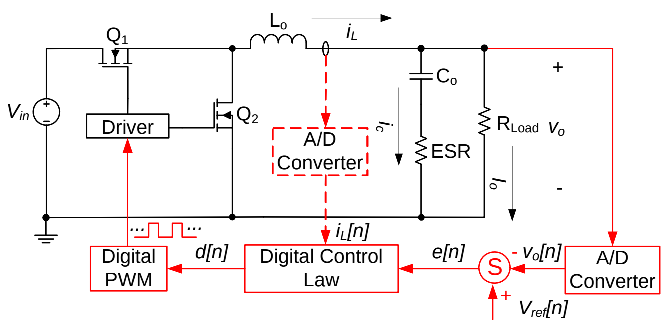

Fig. 1 Digitally controlled synchronous buck converter

Fig. 1 illustrates the implementation of a digitally controlled synchronous buck converter. The controller consists of at least one analog-to-digital converter (ADC) for feedback, a programmable digital control law, and a digital pulse width modulator (DPWM) in order to convert the control output to a modulated pulse waveform with duty cycle *d[n]*.

It is well known that digital control offers advantages over analog control such as programmability, better noise immunity, and low sensitivities to ageing and environmental factors.

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However, from the customer's point of view, the adoption of a new technology that tended to be more expensive and typically did not function as well as present-day technology (in terms of steady-state accuracy and dynamic response performance). From the designer's point of view, digital control compensation development tends to be less intuitive than the tried-and-true analog design methodologies. Furthermore, early digital designs required much larger areas of silicon and consumed more power than analog controllers, effectively prohibiting their adoption into low-power dc-dc power converters. Nevertheless, with the cost and size of digital circuits exponentially shrinking, and researcher's imaginations being sparked by the true power and capabilities of digital control, the opinion that digital control may eventually replace analog controllers is beginning to resurface. This paper discusses the digital control technologies that improve the dynamic performance of DC-DC switching converters.

This paper is organized as follows. In Section II, the digital auto tuning technologies presented. In Section III, the charge balance control is presented. Section IV is conclusion.

II. AUTO-TUNING TECHNOLOGIES

By auto-tuning, it means that the parameters of the power circuits can be determined automatically and the control parameters can then be calculated automatically by digital circuits. The advantage is that the loop is always stable under large parameter value variation.

By use of digital control, it is possible to predict the converter parameters *L*, *C*, ESR, etc., and automatically calculate the compensation coefficients based on bandwidth and phase margin requirements. This is accomplished in [1] – [5] by injecting a specified frequency into the control loop or by adding/amplifying a nonlinearity that causes the output voltage to appear limit cycle oscillation. In [1], the DPWM resolution is intentionally degraded for a short period such that the coarse DPWM resolution will lead to controlled (limit cycle oscillation) LCO. In order to amplify the LCO effect, the digital compensator is temporarily replaced with a PI configuration. By measuring the frequency of the resultant LCO, information related to the converter resonant frequency and output capacitance can be calculated. By measuring the amplitude of the resultant LCO, it is also possible to estimate the Q-factor of the converter (and thus, the load resistance/current). The information is used to design a proper PID by extracting appropriate parameters from LUTs (provided that the load current remains relatively constant).

In [6] and [7], auto tuning is accomplished by introducing a nonlinear relay into the control loop, as shown in Fig. 2. The relay essentially acts as a 1-bit quantizer, causing LCO at the output. When $G_c(z)$ is adjusted to an integrator

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(causing a 90° phase lag in the loop), the output voltage will oscillate at the resonant frequency of the converter. This frequency is measured and stored. This allows for the proper placement of the first zero of a PID compensator. The new PID controller is passed through a low-pass filter to force the desired phase margin at the desired crossover frequency. The second zero is then iteratively placed until the output oscillates at the crossover frequency. After the two zeroes are placed, the compensator gain is set by using the desired bandwidth, zero placement, and an asymptotic Bode plot estimation. The relay function is disabled after the tuning process is completed, allowing for normal loop operation. The advantage of the aforementioned method is that only the frequency of the output voltage oscillation is required to be measured; the amplitude is not required, allowing for more robust operation.

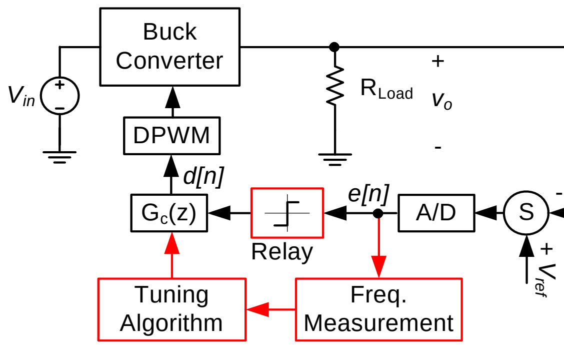

Fig. 2 Nonlinear relay to induce LCOs

On the other hand, the above-mentioned auto tuning algorithms [1] - [4] induce a relatively large voltage oscillation at the output of the converter for a short period of time in order to tune the controller. However, the auto tuning algorithm presented in [11] follows a different approach, as illustrated in Fig. 3. A relatively low-bandwidth multi-input–multi-output (MIMO) controller continuously adjusts the controller's coefficients in an attempt to minimize the f_{c_err} and φ_{m_err}. The system operates by continuously injecting a varying frequency square wave V_z into the DPWM input signal V_x. The DPWM input signal and the digital compensator output signal V_y are passed though a bandpass filter (bandpass equal to the injected frequency) and measured by the digital stability monitor. The injected frequency is adjusted until the magnitude of the two measured filtered signals are equal (indicating the crossover frequency f_c). By comparing the zero-crossover points of the two signals V_y and V_x, the phase margin φ_m of the system can also be calculated. The measured crossover frequency and phase margin are subtracted from the desired crossover frequency and phase margin to produce crossover frequency and phase margin errors (f_{c_err} and φ_{m_err}, respectively).

It is noted that with auto-tuning technology, the control circuit design is significantly simplified and dynamic performance is guaranteed.

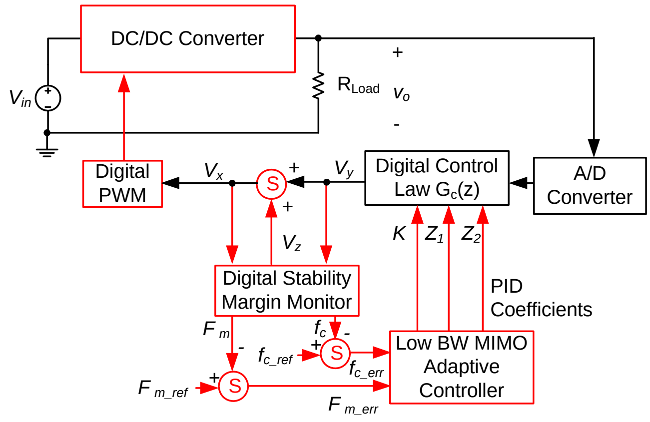

Fig. 3 Auto tuning based on continuous phase margin measurement

III. Charge Balance Control (CBC)

A major application of dc-dc Buck converter is for powering modern processors in the computing industry. Due to the increasing load step/slew value and the stringent requirements of the regulated output voltage, the bandwidth barrier of the conventional linear mode controller needs to be broken through. Although multiphase dc-dc buck converter with conventional controller solution is provided in the market, the incremental transferred cost on the output capacitors apparently limits the applicability of this solution for the future. Under such demands, many advanced control methods are proposed to minimize the concerns or modifications on the hardware design, but achieving optimal or suboptimal response, for example, V^2 control, sliding mode control and capacitor charge balance control.

Charge balance control (CBC, also known as time-optimal control) involves attempting to drive a converter to steady state in the theoretically minimum time and was introduced in [12] for load transient and [17] for input voltage transient. Charge balance controllers typically behave as a linear controller when the converter experiences steady-state conditions and as a nonlinear controller following a transient event. For example, as illustrated in Fig. 4, for a buck converter undergoing a load step transient, it involves a single switching transition at a precise moment. Due to the complex derivation involved, initially, this is well-suited for digital control and has received considerable research attention [8] - [17] and [18] - [21]. The concept involves determining the capacitor current zero-crossover point to estimate the output voltage peak/valley point [19] at t_1. Another key time point is to decide when the switching state of the main switch should be changed, as shown in Fig. 4, at t_2. Finally, the linear mode of controller will take over the regulation task after t_3.

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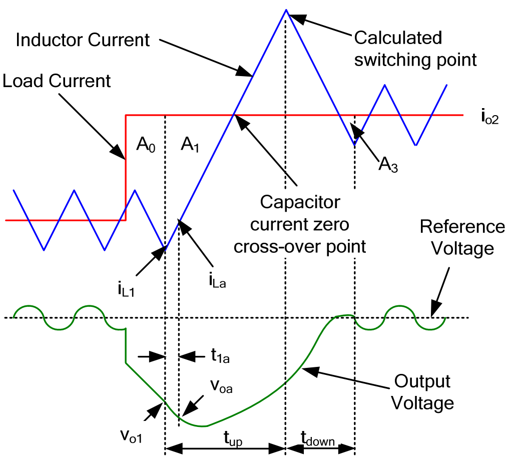

Fig. 4 CBC response under load step transient

In [17], shown in Fig. 5, a new optimal two-switching cycle compensation algorithm is proposed to achieve optimal transient performance for DC-DC converters under an input voltage change. Using the principle of capacitor charge balance, the proposed algorithm predicts the optimized two-switching cycle duty cycle series to drive the output voltage back to the steady state when the input voltage changes. But the algorithm will lose capabilities for regulation ultrafast and large input voltage transient cases.

The controller proposed in [14] employs a asynchronous ADC to capture the time point t_1 based on the voltage valley/peak and uses this information to calculate the optimal switching time instants/intervals, while in [15] and [16], the information is used to calculate the correspondingly mapped output voltage at which the controller should alter its output (ON/OFF) state. An advantage of the controller presented in [15] and [16] is that the inductor and capacitor values are not required; however, it is assumed that the ESR of the capacitor is negligible. If not, the capacitor and ESR values would be required in order to compensate the lead time caused by ESR. From practical design point of view, a current limiting scheme is also concerned in [20], while, fast dynamic response performance can be achieved with proper modifications on original CBC algorithm.

A digital implementation of CBC concept is discussed in [19] based on its analog counterpart [18]. In [19], a current estimation algorithm is presented for predicting capacitor current zero-crossover at t_1. And a double accumulator is employed using FPGA to emulate the double integrator in analog domain [18] and enhance the previous controller performance for AVP extension. With the help of double accumulator/integrator, the algorithm dependence on inductance can be removed, however, for AVP applications the capacitance is still required to be known accurately for determining t_2 in the algorithm.

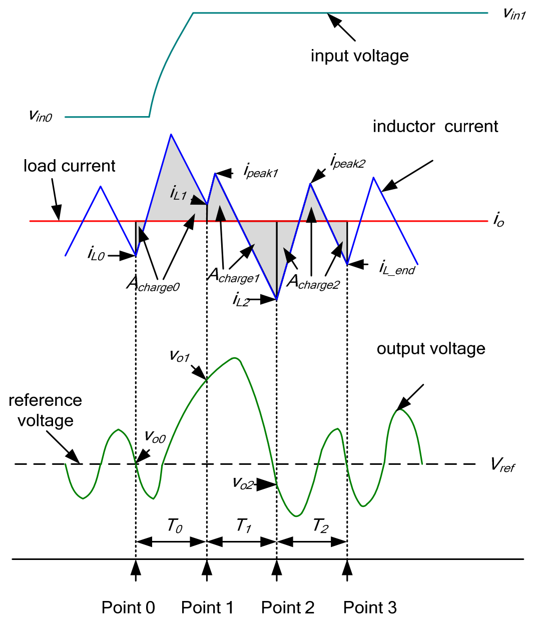

Fig. 5 Charge balance controller response to an input voltage transient

The above nonlinear controllers can be extended to multiphase operation [21] and [22]. In [21], rather than minimum recovery time, it compromises the aim only at achieving the minimum voltage deviations. Further, a smooth controller transition is realized by inserting specified ON/OFF sequences right after the capacitor current undergoes zero-crossover, shown in Fig. 6. However, under a negative load step transient, the improvement is minor because the conventional linear mode compensator is still well-suited for regulating the low output ratio converters with sub-optimal voltage overshoot.

In [22], a current mode digital CBC controller is presented for multiphase Buck converters, which takes advantage of peak current control on the phase inductors to achieve minimum recovery time. During transients shown in Fig. 7, new steady-state current information can be collected at the voltage valley/peak point and the digital peak current reference can be calculated and set based on CBC principles. However, both of the methods [21] and [22] are still limited for low ESR Buck converters and sensitive for passive components' value. Also, the controllers will not work as well for example, if a negative load step occurs before the valley point resulted from a previous positive load step is approached.

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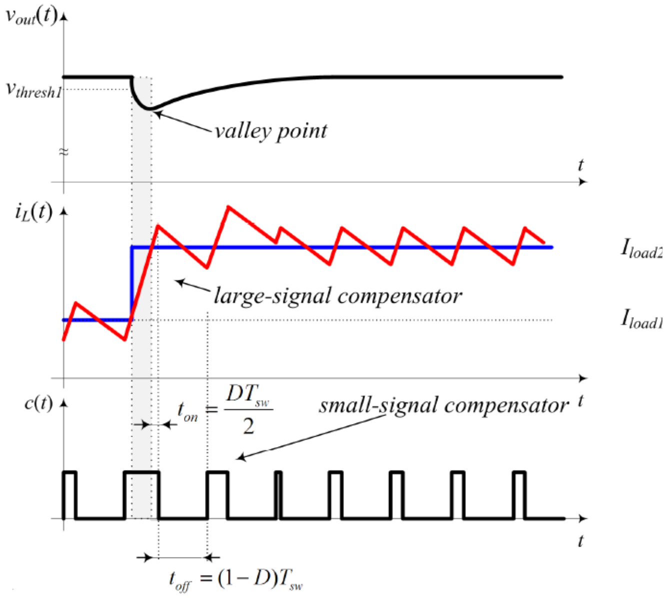

Fig. 6 Principle of operation of the “large-small” signal compensator during light-to-heavy with inserted control sequence

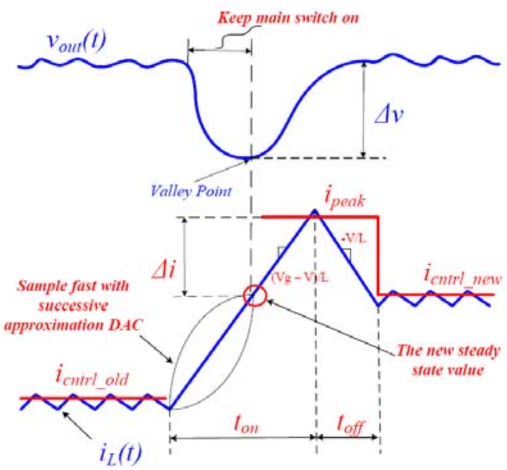

Fig. 7The key waveforms of a single-phase power stage during a light-to heavy load transient. Top: output voltage; Bottom: the inductor current.

It is demonstrated in [18] shown in Fig. 8 that for low-duty-cycle conversion applications (e.g., 12 $V_{dc} \rightarrow 1.5\ V_{dc}$), the voltage overshoot caused by a step-down load current transient may be more than five times as large as the corresponding voltage undershoot caused by a positive current step of equal magnitude.

This is illustrated in Fig. 8. Therefore, to adhere to voltage specifications, capacitor selection must be based on the larger voltage overshoot condition. Numerous topology modifications to Buck and synchronous Buck converters have been proposed to address the aforementioned problem. Ideally, the steady-state duty cycle would be close to 50% in order to achieve a symmetrical transient response to positive and negative load current changes. One solution is to use two synchronous Buck converters in series in order to increase the duty cycle of the second stage. For example, the first stage could convert the voltages 12 $V_{dc} \rightarrow 5\ V_{dc}$ and the second stage could convert the voltages 5 $V_{dc} \rightarrow 1.5\ V_{dc}$. Therefore, the second stage’s steady-state duty cycle would be increased from 12.5% to 30%, yielding a much more symmetric transient response. This allows the use of a smaller inductor for a fixed inductor current ripple value. This concept is studied extensively in [23] and [24].

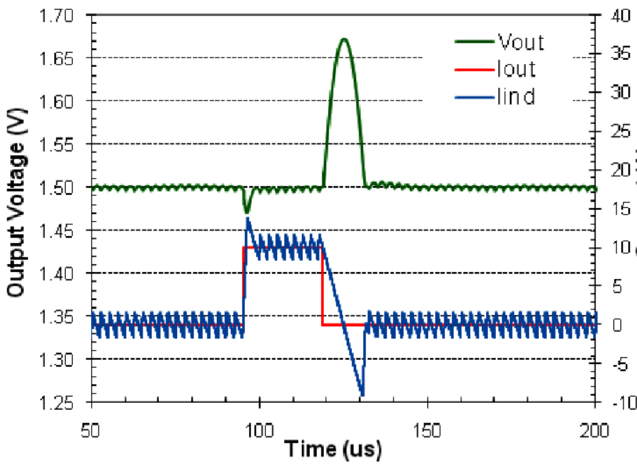

Fig. 8 Asymmetrical transient response to positive and negative load current step change

Three obvious drawbacks of this method are an increase in cost, an increase in physical size, and a decrease in efficiency. However, it is argued in [24] that if a low-enough switching frequency was used in the first stage, then the overall efficiency would not suffer.

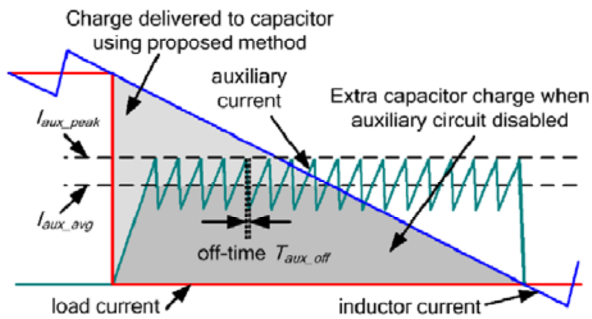

Fig. 9 Peak current mode, constant off-time operation of the proposed controller in [25]

In [25], a controlled auxiliary circuit (CAC) is presented to improve the transient response of a Buck converte, as shown in Fig. 9. It is well established that for converter applications with a large input/ output voltage ratio, voltage overshoots (due to step-down load transients) are much larger than corresponding voltage undershoots (due to step-up load transients). Therefore, the goal of the proposed method is to reduce the overshoot. The control method only activates the auxiliary circuit during step-down load transients and operates by rapidly transferring excess load current from the output inductor of a Buck converter to the converter’s input. The proposed method behaves as a controlled current source shown in Fig. 9 to remove a constant regulated current from the output of the Buck converter. The duration of activation of the auxiliary circuit is also regulated. The proposed circuit has the following advantages:

1) predictable behavior allowing for simplified design;
2) inherent over-current protection;
3) low peak current to average current ratio allowing for use of smaller components.

In addition, the proposed auxiliary controller estimates the magnitude of the unloading transient and sets the auxiliary current proportional to the transient magnitude. This allows for greater design flexibility and increases the auxiliary circuit efficiency for unloading transients of lesser magnitude. In this paper, it is shown through analysis,

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simulation, and experimental results that a large reduction of voltage overshoot and output capacitor requirements can be realized through the addition of a small MOSFET, diode, and inductor.

Capacitor charge balance control is a concept that has generated numerous digital controllers and subsequent analog designs [8] - [25]. The end result is a very fast reaction to transient events with minimal/reduced settling time. The main drawbacks of the existing CBC implementation methods are as follows:

(1) precise information of converter parameter information such as *L* and *C* is required;

(2) fast and accurate ADC for sensing is needed to detect the voltage peal/valley;

(3) complex computation is embedded in CBC algorithm formulas (i.e. division or square root)

(4) the ESR of the output capacitor is assumed to be negligible.

IV. Conclusions

This paper provided a brief review of the latest development of digital control technologies to improve the dynamic performance of DC-DC switching converters. It demonstrates that with auto-tuning and charge balance control technologies, the dynamic performance of DC-DC converters can be significantly improved.

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