Fuzzy-Logic-Based Approach to Accurate Modeling of Double Gate MOSFET for Nanoelectronic Circuit Design

F. Djeffal , A. Ferdi, D. Arar, M.A. Abdi and M. Chahdi

***Abstract*— The Double Gate silicon (DG) MOSFET with extremely short-channel length has the appropriate features to constitute the devices for nanoscale circuit design. To develop a physical model for extremely scaled DG MOSFETs, the drain current in the channel must be accurately determined under the application of drain and gate voltages. However, the modeling of the transport mechanism for the nanoscale structures requires the use of overkill methods and models in terms of complexity and computation time (self-consistent, quantum computations,…). Therefore, new methods and techniques are required to overcome these constraints. In this paper, a new approach based on the fuzzy logic computation is proposed to investigate the nanoscale DG MOSFETs. The proposed approach has been implemented into device simulator to show the impact of the proposed approach on the nanoelectronic circuit design. The approach is general and thus is suitable for any type of nanoscale structure investigation problems in nanotechnology industry.**

***Index Terms*—nanoscale circuit, DG MOSFET, fuzzy modeling, computational cost, circuit design.**

I. Introduction

As transistor feature size moves into nanoscale region for realising the better device performance and higher package density, the characteristic of conventional MOSFET degrades due to the hot-carrier and short channel effects (SCEs). Recently, the importance of multi-gate MOSFETs, particularly Double Gate (DG) MOSFETs, is rising in nanoscale CMOS circuit design. This is mainly due to the superior control of short channel effects (SCEs) because of the reduced influence of the drain voltage on the channel charge. The advantages advocated for DG MOSFET, shown in Figure 1 include: ideal subthreshold slope; light doping of the channel reducing the mobility degradation due to the elimination of impurity scattering; good control of short channel effects; ideal subthreshold swing due to the elimination of substrate doping; etc [1–3]. Although the operation of DG MOSFET is similar to the conventional MOSFET, the physics of this type of MOSFET is more complicated.

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Moreover, physical phenomena, such as the quantum mechanical and short channel effects, have to be considered. Therefore, simulation tools which can be explored to design nanoscale CMOS circuits require new theories and modeling techniques that capture the physics of quantum transport accurately to guide the design for nanoelectronic circuits.

The aggressive scaling scenarios set by the ITRS (International Technology Roadmap for Semiconductors) [4] make the accurate simulation of nanoscale transistors a challenging objective of modeling activities. Previous works which studied the DG MOSFETs include the numerical and analytical modeling [1–3], [5-10]. The accurate modeling of the nanoscale DG MOSFET requires the solution of Schrödinger and Poisson equations based on the non-equilibrium Green's function (NEGF) formalism, assuming quantum effects are to be fully accounted [10]. But from the nanoscale CMOS circuit design point of view even 2-D solution of numerical NEGF is an overkill approach in term of both complexity and computational cost [10]. Moreover, the nanoscale DG MOSFET introduces challenges to analytical compact modeling associated with the enhanced coupling between the electrodes (source, drain, and gates), quantum confinement, ballistic transport, gate tunnelling current, etc. [5-7,9]. However, in these compact models, the quantum confinements for a very thin silicon channel (less than 5 nm) have not been taken into account. Therefore, models are obtained by a simplification of the full physical model (quantum effects, short-channel-effects, etc.). Accurate analytical models are required to be utilized in nanoscale circuit simulators and circuit design tools. In this context, in order to achieve the required accuracy and model simplicity, in this work we present the applicability of Fuzzy Logic (FL) computation approach to develop an analytical drain current model using the well known SPICE level 3 model [11,12], which has been widely used to simulate the conventional bulk MOSFETs, for the nanoscale CMOS circuit design. Finally, the FL-based model of the DG MOSFET was used as a subcircuit in the SIMULINK software for the modeling and simulation of the nanoscale circuits.

II. Modeling Methodology

The basic structure of the DG MOSFET investigated in this study is shown in Fig.1. As MOSFET feature size moves into nanoscale regime, canonical carrier transport theories are no longer capable of describing carrier transport accurately. The canonical theories are basically derived from the Boltzmann transport equation (BTE), with more or fewer approximations

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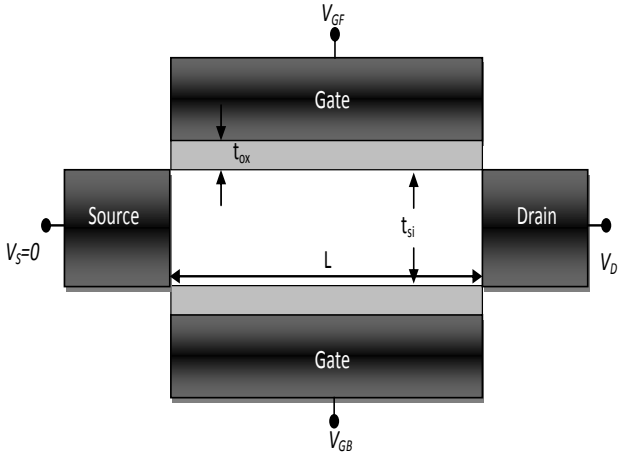

Fig. 1. Schematic sketch of symmetrical DG MOSFET (V_{GF} = V_{GB}) structure investigated in this study with channel doping N_A=10^{16} cm^{-3}.

being made [13]. These models focus on scattering-dominant transport, which typically occurs in long channel devices. However, transistors operate in ballistic or quasi-ballistic transport regime. Simulations using conventional models may either under predict or over predict the electrical device behavior [10, 13, 14].

To simulate nanoscale transistors, the non-equilibrium Green's Function formalism (NEGF) provides one of the best frameworks available [10]. Under ballistic conditions, the Green's Function method is mathematically equivalent to solving, numerically, the Schrpödinger equation with open boundary conditions [10]. Based on the efficiency proven by NEGF for the modeling of nanoscale DG MOSFETs and the difficulty imposed at the moment by the constraints of the nanotechnology to form an experimental database, we have used the NEGF formalism to form the database which will be used to optimize the SPICE Level 3 model using a FL-based computation approach that have several advantages over conventional computing methods.

A. Fuzzy-logic computation

Among control technique Schematics, one that is especially easy to use is the one based on verbal rules that control the behavior of the system, which is called fuzzy control [15]. It is based on the theory of fuzzy sets and Fuzzy Logic [15]. References [15-17] offer extensive introductions to the fundamentals of FL and its wide range of applications. The input–output behavior of a fuzzy system is programmable using linguistic information in the form of IF (preconditions) THEN (postconditions) rules, describing an approximate or qualitative knowledge of an observed process. FL is a superset of conventional Boolean logic that has been extended to include the concept of partial truth-truth-values between 'completely true' and 'completely false'. Due to its simple mechanism and high performance for behavior modeling, FL can be applied to study the nanoscale devices.

The first step of our approach consists of the compact SPICE Level 3 model for conventional bulk MOSFETs. This model is similar to the Power-lane model [11] that introduces

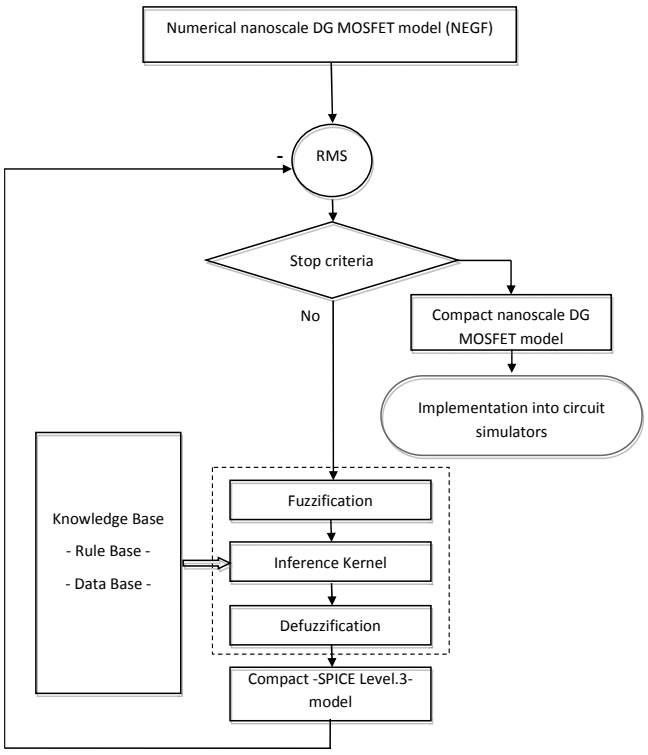

Fig. 1. Flowchart of our Fuzzy-based computation approach.

smoothing functions for the various transition regions. This allows the use of the following single equation to model the drain current for all operation regions.

$$I_{DSF}=\frac{\beta}{1+\theta(V_{GS}-V_T)}\left((V_{GS}-V_T)V_{DS}-\frac{\alpha}{2}V_{DS}^2\right)\left(1+\lambda(V_{DS}-V_{DSsat})\right) \quad (1)$$

where V_{GS} and V_{DS} represent the applied gate and drain voltages, respectively. V_{DSsat} is the saturation drain voltage given as

$$V_{DSsat}=\frac{V_{GS}-V_T}{\alpha} \quad (2)$$

The model parameters are: V_T (threshold voltage), β (gain factor), α (saturation factor), θ (mobility reduction factor), and λ (channel length modulation factor).

To extend the above equation to subthreshold and saturation regions, the gate and drain bias are replaced with two modified expressions, V_{GSX} and V_{DSX} :

$$V_{GSX}=F(V_{GS},V_T,\delta_1) \quad (3a)$$

where $F(V_{GS},V_T,\delta_1)$ is smoothing function [11] given by

$$F_0(x,y,\delta)=\frac{1}{2}\left(x-y+\delta-\sqrt{(x-y+\delta)^2+4\delta x}\right) \quad (3b)$$

The parameter δ is an empirical smoothing parameter used to describe the rate at which V_{GSX} goes to V_{GS} or zero.

The expression for V_{DSX} is similar:

$$V_{DSX}=V_{DSsat}-F(V_{DS},V_T,\delta_2) \quad (3c)$$

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Parameter V_{DSsat} in (1) is also replaced by V_{DSX} to remove the channel length modulation term in the triode region.
With these changes the drain current expression becomes

$$I_{DSF} = \frac{\beta}{1+\theta V_{GSX}}\left(V_{GSX}V_{DSX} - \frac{\alpha}{2}V_{DSX}^2\right)\left(1+\lambda\left(V_{DS}-V_{DSX}\right)\right) \quad (4)$$

This is a very simple expression that is useful for our purposes in order to develop a compact model to study the nanoscale MOSFETs using a FL- based computation. The flowchart of our proposed approach is detailed in Fig.2. The main elements of the FL-based controller are a fuzzification unit, an inference engine, a knowledge database, and the defuzzification unit.

To define the fuzzy associative memory, we need some knowledge about the how each of these parameters affects the behavior of the $I-V$ curves:

- V_T shifts the whole $I_{DS}-V_{GS}$ curve.
- θ describes the curvature of $I_{DS}-V_{DS}$ as V_{GS} increases.
- β provides a scale factor.
- α establishes the relation between V_{GS} and V_{DSsat}.
- λ controls the slope of the $I_{DS}-V_{DS}$ characteristic in saturation.

Based on the effect of each parameter on the $I-V$ characteristics, we can define the following rules in order to develop our knowledge Base (Fig.2) for each design parameter:

- If the calculated curve $I_{DS}-V_{GS}$ is to the right of the numerical data, then decrement V_T, and vice versa.
- If the calculated curve $I_{DS}-V_{GS}$ is more curved than the numerical data, then decrease θ, and vice versa.
- If the calculated curve $I_{DS}-V_{GS}$ is over the numerical data, then decrease β and vice versa.
- If the $I_{DS}-V_{DS}$ calculated curve saturates too soon, decrease α, and vice versa.
- If the slope of the calculated $I_{DS}-V_{DS}$ curve is too small, then increase λ, and vice versa.

In order to implement the above rules, we have used the triangular fuzzy sets, while defuzzification is done through the method of centre of area (COA). The input and output parameters are normalized by using the numerical curves as reference. The linguistic variables chosen for this FL-based controller are the principal and secondary errors (Er_P and Er_S) for each parameter of the compact SPICE Level 3 model (Eq.4). These errors can be calculated, for each parameter, from:

$$Er\_P = \frac{I_{DS-N}(V_{GS} \approx V_T)}{Max(I_{DS-N})} - \frac{I_{DS-F}(V_{GS} \approx V_T)}{Max(I_{DS-F})} \quad (5a)$$

$$Er\_S = \frac{I_{DS-N}(V_{GS} = V_M)}{Max(I_{DS-N})} - \frac{I_{DS-F}(V_{GS} = V_M)}{Max(I_{DS-F})} \quad (5b)$$

where I_{DS-N} and I_{DS-F} represent the 2D numerical drain current simulation and FL-based drain current model, respectively. V_M is the medium voltage given by $V_M = \frac{V_T + V_{DD}}{2}$ with V_{DD} represents the supply voltage.

The both errors are the input linguistic variables and drain current is the finale output linguistic variable. In this work, the principal error of each parameter represents the drain current deviation affected, only, by the main parameter, and the secondary one is the drain current deviation affected by a combination of several parameters (mutual effect). Each of the input and output fuzzy variables is assigned seven linguistic fuzzy subsets varying from negative large (NL) to positive big (PL). Each subset is associated with a triangular membership function to form a set of seven membership functions for each fuzzy variable. The fuzzy controller diagram and the membership functions for each linguistic variable, in the case of fuzzy V_T controller, are given in Figs. 3a and 3b. The linguistic terms chosen for this controller are seven. They are negative large (NL), negative medium (NM), negative small (NS), zero (Z), positive small (PS), positive medium (PM) and positive large (PL). After assigning the input, output ranges to define fuzzy sets, mapping each of the possible five input fuzzy values of principal error(Er_P), three input fuzzy values of secondary error (Er_S) to the seven output fuzzy values is done through a rule base. Therefore, the fuzzy associative memory (FAM), for fuzzy V_T controller, comes into picture. The rules are framed keeping in mind the nature of the system performance and the common sense. Table.1 shows the fuzzy associate memory table of the fuzzy V_T controller.

It is to note that the development of the fuzzy controller for each parameter is carried out by following the same steps, which have been used to develop the fuzzy V_T controller

TABLE II
OPTIMIZED FUZZY ASSOCIATE MEMORY TABLE (FAM) FOR THE FUZZY V_T CONTROLLER

		Er_P (Principal error)				
		NL	*NM*	*Z*	*PM*	*PL*
Er_S Secondary error	*N*	*NL*	*NM*	*NS*	*PS*	*PM*
	Z	*NM*	*NM*	*Z*	*PM*	*PM*
	P	*NM*	*NS*	*PS*	*PM*	*PL*

III. RESULTS AND DISCUSSION

Once all the parameters have been estimated, the method will then iterate from an initial point (a set of parameters) until a stopping condition is found (Fig.2). In each iteration, new values for the parameters will be calculated by the fuzzy controller. The global RMS (Root Mean Square) error between the numerical and the calculated curves, considering all points on the curve, will be updated. In our case, we have used a stopping condition of global RMS error less than a 5%.

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Fig. 3 shows good agreement between numerical and predicted results for the nanoscale DG MOSFETs. Our simulations were carried out for a wide range of nanoscale channel lengths, where we found that the RMS errors are within 5%. This last observation shows the applicability of FL-based approach to study the nanoscale DG MOSFETs. The obtained results can be explained by the fact that the FL-based model is characterized as a computational model based on parallel distributed processing of data. Hence, the FL-based model provides a practical insight into the nanoscale devices modeling without the uncertain accuracy or meticulous tuning effort that face more rigorous nanoscale DG MOSFET models. The FL-based modeling is a step towards a new generation of simulation tools that will allow device and material engineers to explore new classes of electronic devices.

A. Impact on nanoscale circuit design

In order to show the impact of our approach on nanoscale circuit design, we propose the simulation of the digital NAND gate (Fig. 4), which is considered as the most basic elements of digital VLSI circuits [22]. This circuit consists of several nanoscale DG MOSFETs.

The I-V characteristics of each transistor were predicted using the ABM (Analog Behavioural Modeling) FL-based DG MOSFET model. The parameters used for simulation are as follows: $L = 10nm$, $t_{ox} = 1nm$ and $t_{si} = 3nm$. The proposed circuit has been implemented in a standard electronic simulator (SIMSCAPE-SIMULINK). In order to prove the effectiveness of the proposed approach for nanoscale low power and high frequency applications, the supply voltage is fixed at $1V$ and the input voltage frequency is fixed at $1GHz$ for the digital gate circuit. The purpose of this simulation is to study the electrical behavior, time computation and evolution of output voltages for the circuit.

Fig.5 shows the input and output voltages for the investigated circuit. From this figure, it is clearly shown the digital operation (NAND) carried out by this circuit. It is important to note that our FL-based DG MOSFET model can be realistically extended to study other complex practical nanoelectronic circuits like: nanoprocessors and memory cells.

TABLE II
COMPUTATIONAL COST FOR THE ANALYSED CIRCUIT

Model / Circuit	FL-based model	NEGF-based model [10]
Digital NAND gate	5.1 seconds	Several hours

The forgoing simulation results show that the FL-based DG MOSFET model makes it feasible to include quantum effects accurately and generally in nanoelectronic circuit simulation. In this part, we go further to show that the proposed FL-based DG MOSFET model is in fact quite efficient in accomplishing this. In particular, we calculate the computational cost of the FL-based DG MOSFET circuits for the simulations carried out in this section. For the purpose of simulation of circuits shown in Fig. 5, routines and programs for FL computation were developed using MATLAB 7.7 and all simulations are carried out on a computer with a 2.5 GHz CORE (TM) I3 CPU and 4 GB RAM.

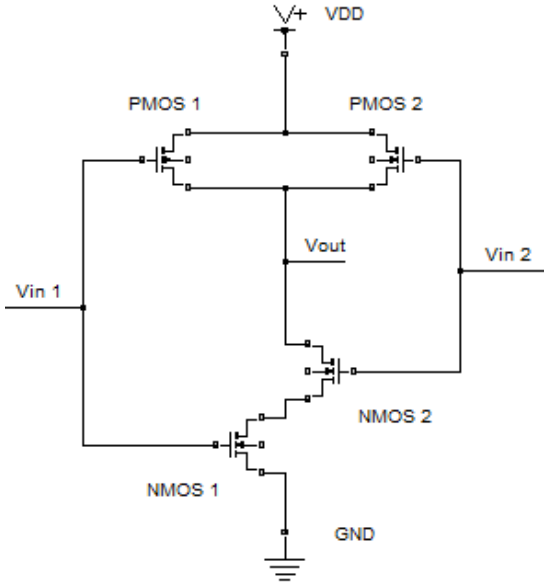
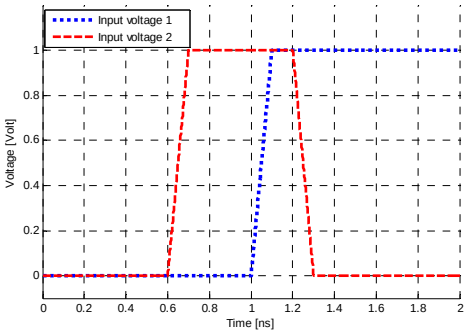


Fig. 4. Digital circuit: NAND gate.

Table 2 gives a comparison of the CPU (central processing unit) time requirements for simulating FL-based DG MOSFET circuits with numerical NEGF-based approach. Obtained results can be explained by the fact that the FL is characterized as computational model based on behavioral and parallel distributed processing of data.

Since the FL-based model is only moderately more computationally demanding than the associated numerical models, it can even be feasibly for to study other structures more complex than DG MOSFET. Therefore, the FL-based modeling provides practical insight into quantum effects in nanoscale electronic devices without the uncertain accuracy or meticulous tuning effort that face more rigorous numerical quantum models



(a) **input signal**

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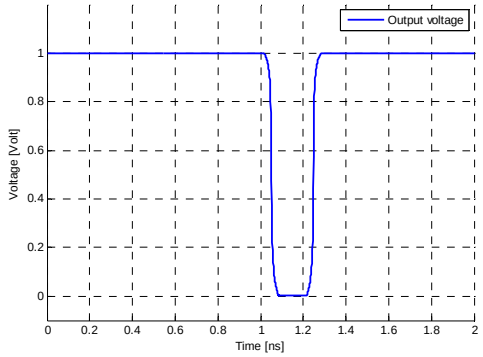

(b) **Output signal**

Fig. 5. SPICE input and output signals of our FL-based NAND gate.

IV. Conclusion

In this paper, we showed the applicability of the FL approach to the nanoscale CMOS circuit simulation problem. The use of 2D NEGF-based numerical simulations enabled us to build the required knowledge database in order to evaluate and optimize our nanoscale DG MOSFET compact model. The behavior modeling process was completed in a relatively short time, with no need for user intervention during the computation. The proposed approach was tested in two different circuits: in a low power voltage amplifier and in nanoscale NAND gate. It is to note that the proposed approach can be extended to include other complex phenomena in nanoscale regime like: hot-carriers, aging phenomena and length modulation in nanoscale domain, which cannot be modeled using conventional analytical approaches. The obtained results have indicated that the developed FL-based approach is particularly suitable to be incorporated in electronic device simulators to study the nanoscale CMOS circuits.

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