Multi-Objective Genetic Algorithms Based Approach to Optimize the Small Signal Parameters of Gate Stack Double Gate MOSFET

T. Bendib, F. Djeffal, T. Bentrcia, D. Arar and N. Lakhdar

***Abstract*— In this paper, the small signal parameters behavior of Gate Stack Double Gate (GSDG) MOSFET are studied and optimized using multi-objective genetic algorithms (MOGAs) for deep submicron CMOS analog circuits' applications. The transconductance and the OFF-current are the small signal parameters which have been determined by the proposed analytical explicit expressions in saturation and subthreshold regions. According to the proposed analytical models, the objectives functions which are the pre-requisite of genetic algorithm are formulated to search for optimal small signal parameters to obtain the best electrical performances of the devices for analog applications. Thus, the encouraging obtained results may be of interest to practical applications.**

***Index Terms*— dosimeter, RADFET, traps, irradiation, sensitivity**

I. Introduction

DOUBLE-GATE (DG) MOSFETs have become very attractive for scaling CMOS devices down to deep submicron sizes because of a number of advantages such excellent short-channel-effects immunity, as ideal sub-threshold slope and unique mobility enhancement [1-3]. This structure utilizes a very thin body to eliminate sub-surface leakage paths between the source and drain. The use of an undoped body is desirable for immunity against dopant fluctuation effects which give rise to threshold-voltage roll-off, and also for reduced drain-to-body capacitance and higher carrier mobility which provide for improved circuit performance. The studied device presented in Fig. 1 is considered as symmetrical structure, with a double-layer gate stack, oxide and high-*k* layers, with no overlap with the source extensions. $N_{D/S}$ represents the doping level of the drain/source region respectively.

There small-signal and subthreshold parameters particularly the transconductance (g_m) and the OFF-current are required basically for analog circuits design [2,4]. These parameters can easily be derived from the device drain current models. To improve the device performances for analog circuits' applications, a new design approaches are required to enhance the reliability performances of the devices for analog applications (voltage amplifiers, Current conveyor,…). One preferable approach is the evolutionary-based model, which could provide practical solutions for a nanoscale CMOS circuits design. We called this the "intelligent simulator" approach [5].

The key idea of this approach is to find the best dimensions, electrical and biasing conditions of the transistor to facilitate the circuits design strategy. In order to facilitate a device design and improve electrical behavior for high-performances analog circuits, the proposed approach suggests two objective functions, which are the transconductance (which describes the transistor behavior in saturation regime) and the OFF-current (which gives the power dissipation of the device), that simplifies the optimization procedure.

In this work, we present the applicability of multi-objective genetic algorithm optimization (MOGA) approach to optimize the small signal parameters of GSDG MOSFET for deep submicron CMOS analog applications. Design optimization, adopted in this work, is the process of finding the maximum/minimum of the device parameters called the objective functions and must also satisfy a certain set of specified requirements within constraints [6, 7]. In multi-objective optimization problems, all objective functions should be optimized simultaneously [6, 7].

II. MOGAs Computation Methodology

Multi-objective optimization has been defined as finding a vector of decision variables satisfying constraints to give acceptable values to all objective functions [6-8]. It has recently been introduced to study the complex and nonlinear systems and has found useful applications in engineering fields [6-9]. An ideal multi-objective optimization procedure constitutes of two steps. The first is to find some optimal solutions corresponding to multiple objectives considered in research space. The next step is to choose the most suitable solution by using higher level information. Due to the simple mechanism and high performance provided by MOGAs for multi-objective global optimization, MOGA can be applied to study the nanoscale GSDG MOSFETs.

In the present study, Pareto approach should be a suitable choice. Pareto approach searches non-dominant solutions called Pareto optimal solutions in the objective space. The number of Pareto optimal solutions is always not single [7,9]. The objective in the design of optimal GSDG MOSFET for analog and digital CMOS-based devices is to find the better design of the transistor that satisfies the high working performances in subthreshold regime.

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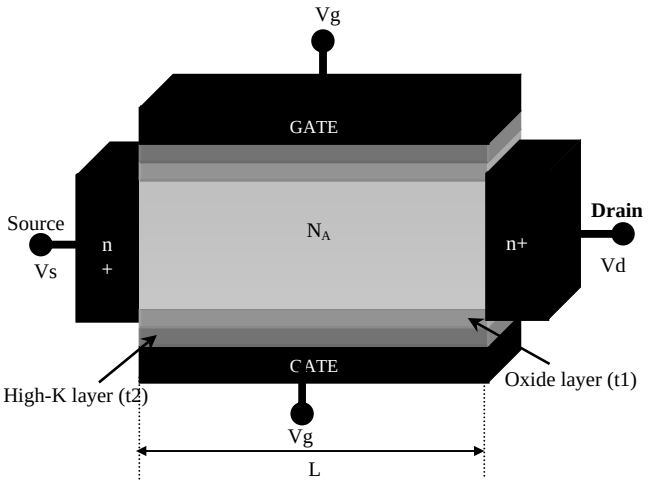

Figure 1. Illustration of the symmetric GSDG MOSFET

The first step of our approach consists of compact models of transconductance and OFF-current parameters for GSDG MOSFETs proposed in [10]. Using the SILVACO software [11], it was observed that the formulated parameters models can be used as objective functions, which are given as function of input design variables.

In the saturation region the drain current can be given as,

$$I_{ds} = \mu_{eff} C_{oxeff} \frac{W}{L}\left[\left(V_g - V_0\right)^2 - \frac{8rk^2T^2}{q^2} e^{q\left(V_g - V_0 - V_{ds}\right)/kT}\right] \quad (1)$$

where μ_{eff} is the effective mobility, C_{oxeff} is the effective capacitance oxide, $r = \varepsilon_{si} t_{oxeff} / \varepsilon_{ox} t_{si}$ is a structural parameters, $t_{oxeff} = t_1 + \frac{\varepsilon_1}{\varepsilon_2} t_2$ is the effective thickness oxide, t_1 is the thickness of the SiO_2 ($\varepsilon_{ox} = \varepsilon_1$) layer and t_2 is the thickness of the high-k layer (ε_2)

V_0 is a weak function of silicon thickness and is close to the threshold voltage of DG MOSFETs. V_0 is given by: $V_0 = \frac{2kT}{q} \ln\left[\frac{2}{t_{si}} \sqrt{\frac{2\varepsilon_{si} kT}{q^2 n_i}}\right]$

In the subthreshold region, the drain current can be given as,

$$I_{ds} = \mu_{eff} \frac{W}{L} kTn_i t_{si} e^{q(Vg)/kT}\left(1 - e^{-qV_{ds}/kT}\right) \quad (2)$$

where t_{si} is the silicon thickness

Note that the subthreshold current is proportional to the silicon thickness t_{si}, but independent of t_{oxeff}. In contrast, the current in saturation region, (1), is proportional to C_{ox}, but independent of silicon film thickness t_{si}. So, our optimized problem can considered as deep non linear coupled objective functions.

According to the drain current expression in the saturation region (1) and the subthreshold region (2), the transconductance and the OFF-state current can be calculated by:

$$g_m(x) = \left.\frac{\partial I_{ds}}{\partial V_g}\right|_{Vds} = \mu_{eff} C_{oxeff} \frac{W}{L}\left[2 \times \left(V_g - V_0\right) - \frac{8rkT}{q} e^{q\left(V_g - V_0 - V_{ds}\right)/kT}\right] \quad (3)$$

$$I_{OFF}(x) = I_{sub}\big|_{V_{gs}=0} = \mu_{eff} \frac{W}{L} kTn_i t_{si}\left(1 - e^{-qV_{ds}/kT}\right) \quad (4)$$

III. Results and Discussion

In what follows, first, we will consider the problem of electrical and geometrical synthesis to improve the electrical behavior of the transistor for both regimes of working, which are the subthreshold and saturation regimes. The obtained design can provide the best subthreshold and saturation parameters by satisfying of the following objective functions:

- Maximization of the transconductance function:
- Minimization of the OFF-current state:

where x represents the input variables vector which is given as, $x = (t_{si}, t_1, t_2, \varepsilon_2, L, V_g, V_{ds})$.

Finally, the global optimization approach is adopted. This approach is a multi-objective function optimization where several objective functions are considered simultaneously.

Genetic algorithms have been shown to solve non-linear problems by exploring all regions of state space and exponentially exploiting promising areas through selection, crossover and mutation applied to individuals in populations [7].

TABLE I
Optimized GSDG MOSFET Design Parameters

Optimized parameters		
Symbol	Quantity	Values
Vds	Drain source voltage	4.8512V
Vg	Gate voltage	4.9999V
t_{si}	Silicon thickness	49.999 nm
t_1	thickness of the SiO_2	0.5046nm
t_2	thickness of the high-k layer	0.5010nm
L	Channel length	144.7187nm
ε_2	Permittivity of the high-k layer	39.9999
I_{OFF}	OFF-state current	9.0044 10^{-14}A/µm
Gm	transconductance	1.7374 10^{-2} S/ µm

The overall objective function is obtained by given weightage based on 'Weighted sum approach method' as follows:

$$F(x) = w_1 . g_m(x) + w_2 . I_{OFF}(x) \quad (5)$$

where w_1 and w_2 are weight functions. If high derived current, ONN-current, and low power dissipation transistor is the device produced by this process, then both transconductance and OFF-state current are equally important. Hence, w_1 and w_2 can be assigned equal values as 0.5. Lower value of OFF-state current is needed to design a transistor with low power dissipation and high transconductance values are

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needed to improve the transistor behavior in saturation regime. It is to note that the optimization of the transconductance and OFF-state current leads to increase of the ON-state current, and therefore an increasing of the ration I_{ON} / I_{OFF} can be obtained by our approach.

Given the clearly defined problem to be solved and a bit-string representation for candidate solutions, the adopted MOGA works as follows [7],

Start with a randomly generated population of 'n' chromosomes (candidate solutions to the problems):

- Calculate the overall objective function of each of the chromosome 'x' in the population.
- Create 'n' offspring from current population using the three MOGA operators namely selection, crossover and mutation.
- Replace the current population with the updated one.
- Repeat the above steps until the termination criteria are reached.

It is to note that at the end of each of evolutionary period, the non-dominated individuals (paretian solutions) are selected from dynamic population and added to elitist one (paretian population). The elitist population is then filtered to yield a non-dominated population. For our MOGA-based approach, the optimum solutions form what is called a 'Pareto Front' . These solutions correspond to the non-dominated individuals which present the best solution of the objective functions simultaneously.

The MOGA parameters were varied and the associated optimization error was recorded. For this configuration, the fitness function, global objective function, was *28.877* and almost 99 % of the submitted cases were learnt correctly. This resulted in *10 000* parameter set evaluations, and took about *20s* to complete using Windows XP with Pentium IV (1.5 GHz).

Figure. 2 shows the variation of global overall fitness function, optimized transconductance and optimized OFF-state current with generation for a maximum iteration of 500.

The steady decrease in both transconductance and optimized OFF-state current of the best solution in each generation until it reaches a best possible value can be attributed to the selection procedure used namely tournament wheel selection. Final optimized (GSDG) MOSFET parameters are summarized in Table. 1.

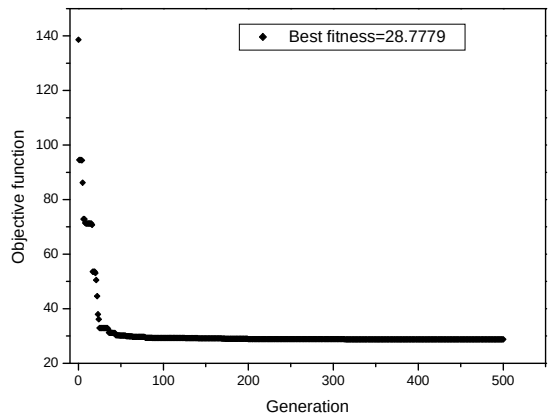

Figure 2. Variation of normalized overall objective function .

IV. Conclusion

In this work, MOGA- based approach is proposed to improve the subthreshold performances and saturation behavior of (GSDG) MOSFET for deep submicron CMOS digital applications. A global optimization problem was then formulated where all the parameters of the (GSDG) MOSFET were considered simultaneously, and the problem is presented as a multi-objective optimization one where the geometry and the electrical parameters were considered simultaneously. Such multi-objective optimization led to discovering of important relationships and useful optimal design principals in electrical behavior optimization of deep sub micron devices both in the space of objective functions and device parameters. The proposed approach has successfully searched the best possible transistor performances and the input design parameters that can yield those specific performances. It can be concluded that the proposed MOGA-based approach is efficient and gives the promising results for circuits design and optimization problems.

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