Mixed Mode Analysis of Raised Buried Oxide Tunnel FET

B. Bhowmick and S. Baishya

***Abstract*—: In this paper, a mixed mode signal analysis of Raised Buried Oxide structure (RBO) Tunnel FET is done considering digital logic inverter circuit. The simulation is done using Synopsys TCAD tools. The transient analysis of output voltage, and digital circuit parameters like transconductance, output conductance etc. are measured and compared with conventional Silicon TFET. Here a p channel TFET and n channel TFET is simulated and device DC characteristics are also plotted. This paper provides the estimation of the switching speed characterized by power delay product (PDP). Furthermore, it is also reported that the switching delay in case of Si Tunnel FET can be overcome by the Raised Buried Oxide Tunnel FET, and overshoot and undershoots in case of Si Tunnel FET can also be minimized in RBO TFET.**

***Index Terms*—Band-to-band tunneling, PDP, quantum capacitance, raised buried oxide.**

I. Introduction

Aggressive supply voltage scaling is an approach towards reducing the static and dynamic energy consumption since it reduces the dynamic power quadratically and the leakage power linearly and also to maintain transistor performance off state leakage current should be reduced and the on state current should be increased [1]. Supply voltage scaling limits the ON current and the $I_{ON} - I_{OFF}$ ratio [2]. The fundamental limit for threshold voltage scaling arises from MOSFETs 60 mV/decade subthreshold swing at room temperature [3]. But in case of Tunnel FET this fundamental limit can be overcome [4]-[5]. Tunnel FET is a quantum mechanical device and it has reduced short channel effects compare to MOSFET [6].Recently, due to the band-to-band tunneling mechanism, Tunnel FET has become a promising candidate to replace CMOS [6]-[7]. The current in the tunnel FET based on tunneling probability which is an exponential function of energy band gap and effective mass of the material [8]. But the on current in large band gap silicon is less. Therefore, a modified device structure is used. An SOI structure with Raised Buried Oxide feature is simulated [9]. The device can operate in n-channel mode and p-channel modes.

The detail understanding of the Capacitance is very important for circuit level operation of Tunnel FETs. The total gate capacitance (C_{gg}) of TFET include gate-to-source capacitance, gate-to-drain capacitance and quantum capacitance of the channel [10]. The gate to source capacitance $\left(C_{gs}\right)$ for conventional silicon TFET is very low in the ON state and gate to drain capacitance or Miller capacitance $\left(C_{gd}\right)$ is very large due to little potential drop between the channel and drain [11]. In the OFF state, C_{gd} dominates since source to channel barrier resistance is large compare to that of drain to channel [12]. The quantum capacitance originates from filling the channel density of states from source and drain reservoirs [13]-[14]. The quantum capacitance can be determined from Non equilibrium Green's function formalism [15].In order to meet ITRS requirement and reduced Miller capacitance, heterogate oxide and SOI structure with Raised Buried Oxide in drain has been proposed. Heterogate dielectric structure reduces parasitic bipolar current and increases on current [16].

To investigate the circuit-level switching performance of RBO SOI Tunnel FET, an inverter operation is analyzed. Transconductance, output conductance and total gate capacitance are measured. The transient characteristics are also shown and the RBO structure exhibits low voltage overshoot and undershoot due to its reduced miller capacitance and high drive current.

II. Principle of Operation

The device operates on the principle of band-to-band tunneling. An N type Tunnel FET consists of a P+ source, intrinsic (i) channel and a N+ drain and the P type Tunnel FET has N+ source, intrinsic (i) channel and P+ drain regions. The source and drain regions are heavily doped regions and the channel region being intrinsic. The gate work function of N type TFET is modified suitably to obtain a P-channel TFET. TFETs operation takes place by tunneling of carriers from the valence band in the source to the conduction band in the channel [8]. The doping concentration in source, channel, and drain are respectively 10^{21} cm^{-3}, 10^{16} cm^{-3}, $5X10^{19}$ cm^{-3}. In the OFF state (V_{gs} =0V,V_{ds} = 0.7V), the tunneling transmission probability is low due to the thick depletion region associated with the source to intrinsic tunnel junction, which results in very low

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OFF currents. With the application of the gate voltage ($V_{gs} = 1V, V_{ds} = 0.7V$), the depletion region shrinks and the carriers tunnel through the barrier i.e. from valence band of P + source to the conduction band in channel in case of N type TFET. The TFET ON current is limited by the inter-band tunneling compared to thermionic emission over the barrier. The reverse biased leakage current under the OFF state condition yields extremely low OFF current in the order of Pico-amp P type Tunnel and N type Tunnel FET. The device is hetero gate tunnel FET where high-k gate oxide (H_fO_2) is over the tunneling junction and low-k gate oxide (SiO_2) is on the channel. This heterogate oxide provides high gate coupling in the tunnel junction and reduced ambipolar current in the drain side [16]. The device is a SOI device with Raised Buried Oxide feature to achieve high on current, low off current, high on/off current ratio, low subthreshold swing, and reduced Miller capacitance effect [11]. A low band gap material Germanium is used at the tunnel junction to enhance the tunneling probability. Here inverter is designed considering the P and N type RBO tunnel FET. The CMOS inverter is a basic building block for digital circuit design [12]. Due to the smaller effective device area and the smaller static power consumption compared to the standard MOSFET. The integrated substrate/well contact, the source of the TFET is shorted to the substrate/well [12]. Thus, for a single/twin-well bulk process, only devices with the source not connected to the power rails can be realized as RBO TFETs.

The static power dissipation of inverter is practically zero, the inverter can be sized to give equal sourcing and sinking capabilities and the logic switching threshold can be set by changing the size of the device.

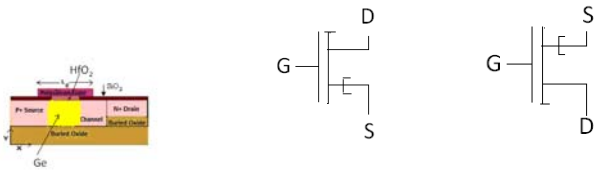

Fig.1 (a) RBO Tunnel FET (b) N FET (RBO) (c) P TFET (RBO)

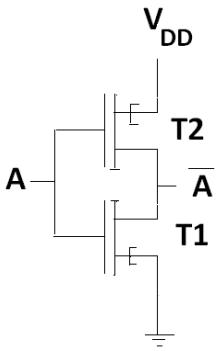

Fig. 2 Basic building block of digital logic inverter

III. Result and Discussion

The simulation is done using Synopsis TCAD tools where non local band-to-band tunneling model is activated. Band gap narrowing is also activated. The mixed mode simulation is done for an inverter consists of N type and P type Raised Buried Oxide Tunnel FETs. Sentaurus Device computes the transient response of the inverter to a voltage signal, which codes a 010 binary sequence. Here capacitor load is used.

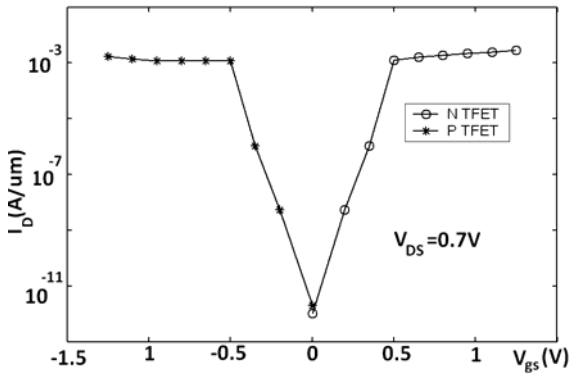

Fig. 3 Log I_D vs. V_{gs} characteristics for N type and P type RBO TFET

The device has mA range on current and Pico ampere range off current. To increase the on current in TFET according to ITRS requirement, we have used SOI structure with Raised Buried Oxide in drain. Here a FD SOI structure is simulated. FD devices have low electric field, and quasi-ideal subthreshold slope characteristics [14]. In case of TFETs, band-to-band tunneling occurs at high electric field near the tunneling junction. Here the silicon film thickness used is 30 nm in channel and source, and in the drain it is 20 nm. In Fig. 2 the digital inverter is shown with the RBO Tunnel FET.

Fig.3 shows the DC characteristics for N type and P type RBO SOI Tunnel FET.

In Fig. 4, the transient response of conventional Silicon Tunnel FET is shown for an [010] input. Output voltage overshoot of 66.7 % and undershoot of 34 % of input voltage are observed due to the large Miller feedthrough capacitance originating from its fundamental device operation coupled with its low drive current. The overshoot and undershoots are improved for an inverter operation with RBO Tunel FET as shown in Fig. 5. In raised buried oxide structure, the gate-to-drain capacitance is reduced and hence, the effective under/overshoots are lowered as compare to conventional Tunnel FET. The gate capacitance is also limited by quantum capacitance limit.

Next, in Fig. 6 the transconductance (g_m) vs. V_{gs} graph is plotted. When the RBO is used, the surface roughness scattering in the source and the channel increases as compared to the drain region. This is due to the fact that peak electron concentration is located at some distance from Raised BOX in the drain, and accordingly, the peak electron concentration occurs at source tunneling junction. Hence the

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overall channel mobility is not degraded and an increased g_m is obtained and channel resistance is less.

Fig. 7 compares the output conductance vs. V_{ds} graph of RBO TFET to the Si TFET.

The increase in gate oxide capacitances (as the device sizes scale down), along with the quantum confined structures, have made the quantum capacitance limit of device operation increasingly relevant; i.e. condition $C_{OX} > C_Q$ where and C_{OX} and C_Q are the gate oxide and quantum capacitance, respectively [17, 18]. C_Q is related to the average density of states (DOS) near the Fermi level [19]. In the case of the TFET even though the conduction band in the channel is well below the source E_F, the channel states are relatively empty. This is due to the presence of the tunneling barrier that hinders carrier injection into the channel from the source reservoir. The DOS of TFET structures can become significantly small [13], thus the aforementioned condition can be easily achieved. In this case the gate capacitance is dominated by C_Q. Fig. 8 shows the normalized Miller capacitance for Si Tunnel FET and RBO Tunnel FET as a function of its input voltage. In case of RBO TFET due to high drive current, Raised Buried Oxide in drain, and the presence of Germanium in the source, the normalized gate capacitance is found to be reduced compared to Si TFET.

The dynamic power dissipation for an inverter is given by

$$P_D = fCV_{DD}^2 \qquad (1)$$

Where f is the frequency at which inverter is switched and C is the total gate capacitance.

The frequency is related with propagation delay, lower the propagation delay , the higher the frequency at which the circuit can be operated and higher the power dissipation in the circuit. A figure of merit or a quality measure of the particular circuit technology is power delay product(PDP).

$$PDP = P_D(t_{PHL} + t_{PLH}) \qquad (2)$$

In TableI, power delay product is estimated at $V_{DD} = 0.3V$. It is observed that the RBO Tunnel FET has less PDP compared with Si TFET.

Fig. 9 shows the dependence of PDP on V_{DD} at $I_{ON/IOFF}$ ratio= 10^9. PDP shows a clear advantage of RBO TFET over Si TFET for low switching power. So, RBO FET might be better suited for low-power applications

TABLE I
COMPARISON OF RBO AND SILICON TFET

Type of FET	% overshoot	PDP	% undershoot	Dynamic power dissipation
Si TFET	66.7	843 eV	34	$0.045X10^{-4}$watt
RBO TFET	20	37.9 eV	8	$0.067X10^{-5}$watt

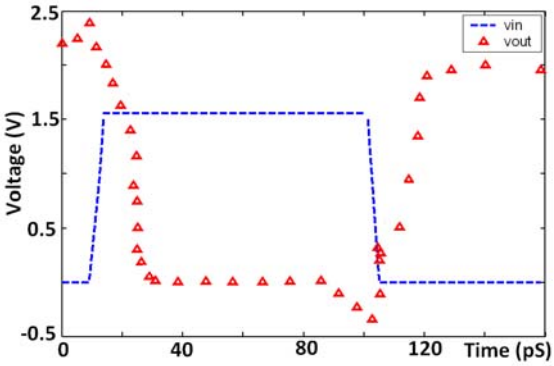

Fig 4. For silicon TFET

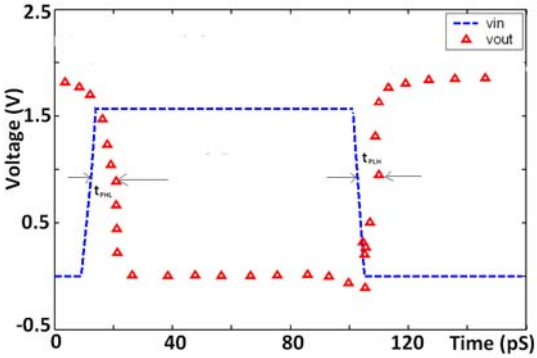

Fig. 5 Transient characteristics for RBO TFET

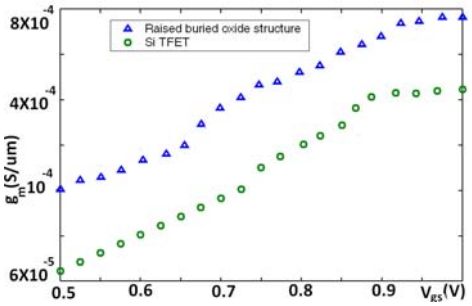

Fig. 6. Transconductance as a function of input voltage.

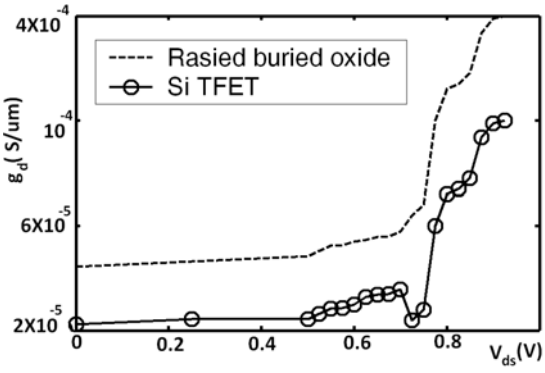

Fig. 7. Output Conductance vs V_{ds}

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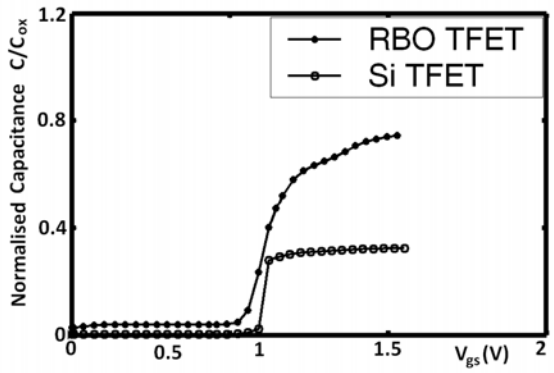

Fig. 8 Capacitance voltage characteristics of RBO and Si TFET.

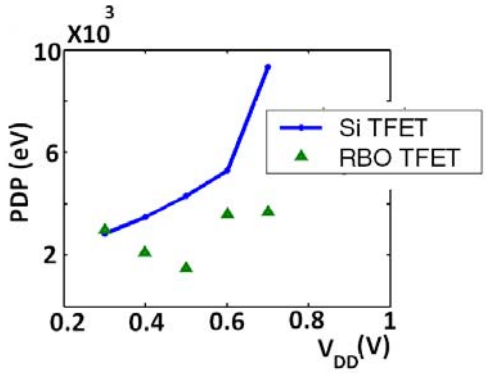

Fig. 9 Comparison of power delay product for Si and RBO TFET at $I_{ON/IOFF}$ ratio= 10^9

IV. Conclusion

The potential of RBO Tunnel FETs was examined by TCAD simulation. We find that fairly large ON-current (> 1mA) , transconductance, output conductance, and dynamic power consumption of $0.067X10^{-5}$watt should be readily achieved at 10^9 $I_{ON/IOFF}$ ratio and significantly improved overshoot and undershoots as compared to Si Tunnel FET. Hence RBO Tunnel FET might be suitable for ultra-low power digital applications.

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