Design of 3-16GHz Ultra-Wideband CMOS LNA Based on Current-Reused Topology

Meng-Ting Hsu #1, Yi-Cheng Chang#2 , Yu-Hwa Lin#3

Abstract—**This paper presents an UWB low noise amplifier (LNA) based on current reused topology to achieve low power on overall circuit in the band of 3~16GHz. Measurement of the input and output reflection coefficient S11, S22 are less than -10 dB, the maximum amplifier gain S21 gives 9.7dB, the minimum of the noise figure is 4.2dB, the measured IIP3 is -8.5dBm at 6GHz. It consumes 11mW power consumption from 1.1-V supply voltage. This chip was implemented by TSMC 0.18μm 1P6M process.**

Index Terms —**Low noise amplifier(LNA), Current-reused, Ultra-wide band(UWB), low power**

I. INTRODUCTION

Two approaches have been proposed to exploit the spectrum of 3.1–10.6-GHz allocated for UWB systems. One uses multiband OFDM modulation with 14 528-MHz sub-bands and a fast frequency-hopping scheme. The other transmits short-duration pulses with position or polarity modulation, which results in signals spreading over several gigahertz of bandwidth[1].

The low noise amplifier (LNA) is mainly designed for UWB system. Many topologies have been presented in LNA designs, such as distributed amplifiers[2], resistive shunt feedback[3], cascade amplifier[4], and current–reused amplifier[5]. The distributed amplifier can improve gain at higher frequency and hence can extend the bandwidth. But it needs more inductors and thus consumes more power. Resistive shunt feedback has numerous advantages for broadband amplification including gain flatness, stability, noise figure, and matching. But feedback also exchange gain for bandwidth. However, saving power is very important for mobile installment. That goal can be reached by providing lower supply voltage.

In this paper, in order to reduce power consumption where current reused circuit is used. And T-match network with source degenerated inductor is used to achieve the input matching in section Ⅱ. The circuit design and description are also addressed in this section.

The Measurement result is shown in sectionⅢ. Finally, the conclusion is given in Ⅳ.
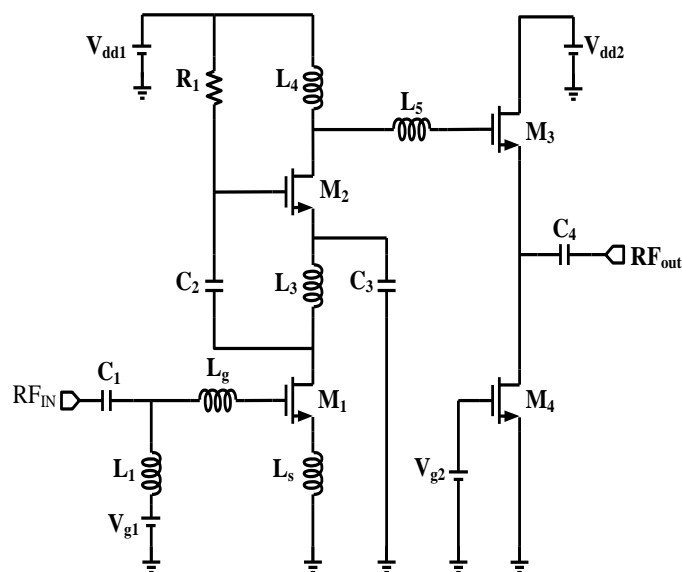
II. CIRCUIT DESIGN

Fig.1   Schematic of the proposed LNA.

A. Input matching network

Fig.1 shows the proposed circuit based on common source topology with current-reused technique. The first stage is used to reduce power consumption with current-reused technique. The second stage is worked for output matching and bandwidth extension. This section, the main circuit is designed to reduce component and the chip area. By using a source degenerated inductor coupled with high-pass filter is worked to form the input matching network. Design of the circuit of the input matching, to avoid using the resistive element as a bias, due to resistor itself will generate lots of noise, cause overall circuit noise rising, so in this paper, we uses inductance to reduce noise. Transistors, inductors, capacitors have their own internal resistance of the composition, so we use their internal parasitic resistance as 50Ω impedance matching, using a T-match network and the parasitic capacitance of the transistor makes imaginary part of the impedance elimination. The total input impedance of low-frequency MOS model is shown in equation(1).

$$Z_{in} = \frac{1}{sC_1} + \left\{ sL_1 \, // \left[sL_g + \left(\frac{1}{sC_{gs1}} + \frac{gmLs}{Cgs} \right) \right] \right\} \qquad (1)$$

B. Current-reused technique

In order to achieve lower power consumption, we adopt the current-reused structure to achieve high gain and avoid increasing the power consumption. The current-reused structure is the most easier topology for the circuit design. The presented LNA adopts two-stage cascade architecture to achieve enough power gain and bandwidth. The first stage is designed to resonate at the lower band, and the second stage is to resonate at the higher band. In order to achieve a flatness power gain, the inter-stage matching network is designed for gain compensation.
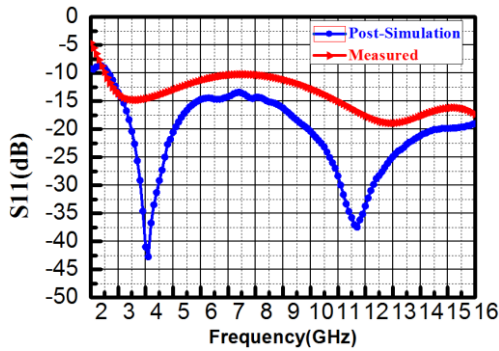
Ⅲ. MEASUREMENTS

Fig 3   Simulated and measured S11
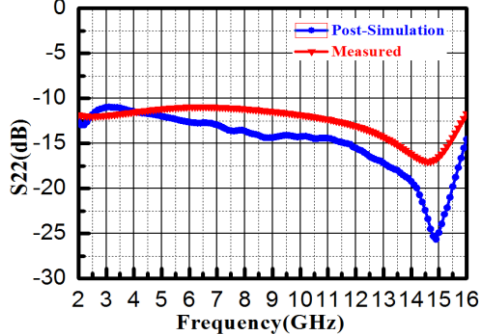

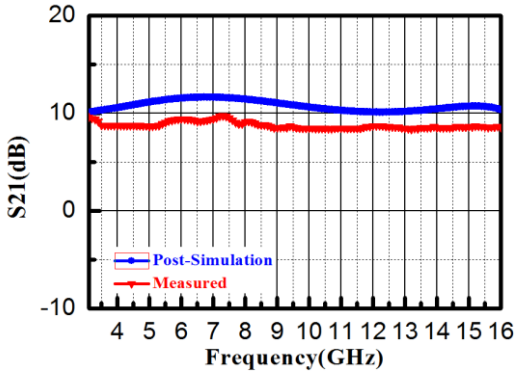Fig 4   Simulated and measured S22

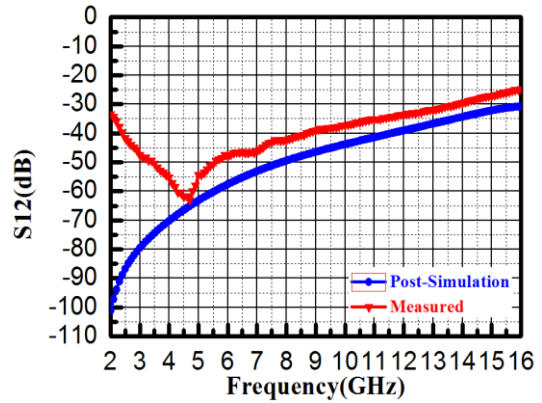Fig 5   Simulated and measured S21
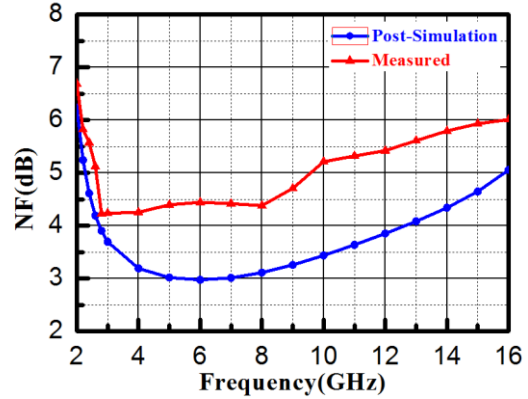

Fig 6   Simulated and measured S12
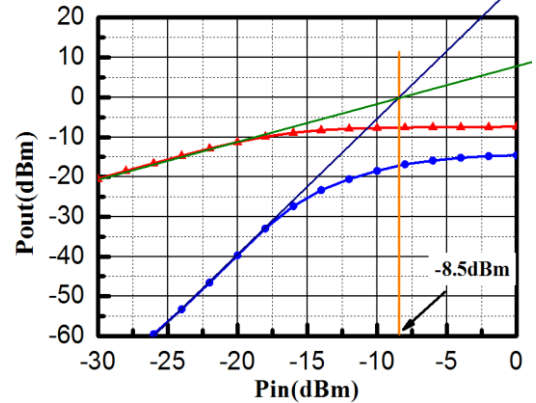

Fig 7   Simulated and measured NF

Fig 8   Measurement of IIP3

Figure.3 shows the measured and simulated input reflection coefficient (S11) results. The measured S11 was lower than -10dB over the entire 3-16 GHz UWB frequency range. The measured and simulated of output reflection coefficients (S22) are shown in Figure.4. The measured S22 was less than -12 dB over a 3-16 GHz range. This proved the effectiveness of the broadband matching. In Figure.5 the measured and simulated forward gains (S21) are reported for the UWB LNA circuit. The maximum S21 was 9.7 dB. Figure.6 indicates the measured and simulated reverse isolation (S12) for the UWB LNA circuit. An excellent S12 was less than -26 dB. The measured and simulated NF is shown in Figure.7. The minimum NF was as low as 4.2 dB. The linearity of input third-order intercept point is -8.5dBm in Fig.8. The power consumption is 11mW at 1.1V supply voltage. The comparison of overall performance LNAs is defined as [6].

$$FOM = \frac{Gain_{max}(dB) * BW(GHz)}{(F-1) * Pd(mW)} \qquad (5)$$

$$FOM_A = \frac{Gain_{max}[dB] \times BW[GHz]}{(F-1) \times P_{DC}[mW] \times Area[mm^2]} \tag{6}$$

Where $Gain_{max}$ is the maximum gain value, BW is the 3dB bandwidth, F is the absolute value of noise figure and P_d is the DC power consumption. Area represents the chip area and its value is related to a typical area of 1 mm^2.

Table I summarizes the measured performance of the LNA and compares with the other reported circuit performance. The proposed circuit shown a good performance with low power, high gain and low noise.

TABLE I COMPARISON OF LNA WITH SIMILAR CURRENT-REUSED STRUCTURE

Reference	[7]	[8]	[9]	[10]	This work
Technology	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS
Frequency (GHz)	3.1-10.6	3.1-12.2	2-11	3.1-10.6	3-16
S11 (dB)	<-9	<-8.7	<-9.9	<-12	<-10
S22 (dB)	N/A	<-10.9	N/A	<-14	<-12
S12 (dB)	N/A	N/A	N/A	N/A	<-12
S21max (dB)	12	13.1	12.1	13	9.7
NFmin (dB)	3.8	2.7	3.6	4	4.2
PDC (mW)	9.8	13.9	14.3	4.6	11
IIP3 (dBm)	N/A	-9	-10	-14	-8.5
Chip Size	N/A	N/A	1.118	0.928	0.925
FOM	6.6	9.97	5.9	14.13	7.165
FOM_A	N/A	N/A	5.28	15.23	7.737

IV CONCLUSION

This paper demonstrates a low power UWB LNA Based on the common source topology. The current-reused technique is used to form a cascoded structure to reduce the power consumption. Measurement results show the power gain with 9.7dB, noise figure with 4.2dB and IIP_3 is -8.5dBm. The proposed circuit consumes 11mW from 1.1V supply voltage.

ACKNOWLEDGMENT

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