Modeling and Software Implementation of PID Controlled Higher Order PLL

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***Abstract*— We propose for modeling and software implementation of proportional-integral-derivative controlled higher order phase-locked loop with low settling time acquisitions applicable to frequency modulated transceiver. The implementation has been done by inserting a proportional-integral-derivative control block into the phase-locked loop during acquisition, where originally the output frequency/phase is controlled by a low pass loop filter. Simulation results show that the method can reduce the settling time up to 94%, 49% and 18% for 2nd, 3rd and 4th order phase-locked loop up to a frequency range of 0.9GHz.**

***Index Terms*— Phase-locked loop, Proportional-integral-derivative controller, Low pass loop filter, settling time.**

I. Introduction

Phase-locked loop (PLL) is essentially a control system that employs feedback to maintain the phase of output signal in step with the phase of a reference signal [1, 2, 3, 4]. When the PLL is in lock, a small phase difference between the two input signals of the phase detector (PD) is observed. This phase difference results in a dc voltage at the detector output which is used to shift the voltage controlled oscillator (VCO) from its free-running frequency and keep the loop in lock.

PLLs are employed in a wide variety of communication systems including frequency synthesizers, modulators and demodulators, motor speed control, signal detection etc [5]. In applications such as wireless local area networks (WLANs) where fast frequency-hopped spread spectrum methods is used, the settling time of the PLL is of great importance [6]. Also, in application, like frequency modulated (FM) transceiver which has multiple frequency channels, needs local oscillation frequency for reception and carrier frequency for transmission with low settling time. Thus, it is essential to improve the settling time without effecting the noise performance and power consumptions of the system. This can be achieved by inserting a proportional-integral-derivative (PID) control block into the PLL during acquisition where originally the output frequency/phase is controlled by a low pass loop filter (LPF). A PID filter is employed in a time recovery PLL for synchronizing and reducing the settling time of the system. The proportional and integral (PI) term of the PID filter decrease the settling time of the PLL by increasing the phase margin and damping factor (DF).

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II. The Model & Theoretical Estimation

A. The model

The basic block diagram of the proposed PID controlled PLL is shown in **Fig.1**. It consists of a phase detector (PD), a PID unit along with optional LPF, a VCO and a frequency divider (FD) network.

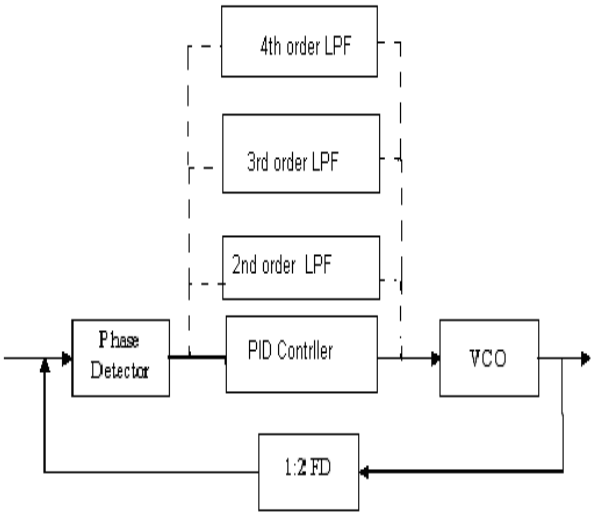

Fig.1: Block diagram of the proposed PID controlled PLL model

B. Theoretical estimation

The transfer function (TF) of the PLL model can be expressed as [7]:

$$H(s) = \frac{K_d F(s)\frac{K_0}{s}}{1 + \frac{K_d F(s) K_0}{Ns}} \quad (1)$$

The TF of the 2nd order LPF introduced in the system can be written as:

$$T_{f2nd} = \frac{CR_2 s + 1}{C(R_1 + R_2)s + 1} \quad (2)$$

Combining equation (1) and equation (2), the TF of the system with 2nd order LPF in the loop become,

$$H(s) = \frac{K_d T_{f2nd}\frac{K_0}{s}}{1 + K_d T_{f2nd}\frac{K_0}{Ns}} \quad (3)$$

The TF of the 3rd order LPF introduced in the present system is given by,

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$$T_{f3rd} = \frac{(C^2R_2R)s^2 + C[2R_2 + R_1 + R]s + 2}{C^2R[R_1 + R_2]s^2 + C[R + R_1 + R_2]s + 1} \quad (4)$$

Combining equation (1) and equation (4), the TF of the system with 3rd order LPF in the loop can be derived as:

$$H(s) = \frac{K_d T_{f3rd} \frac{K_0}{s}}{1 + \frac{k_d T_{f3rd} K_0}{Ns}} \quad (5)$$

In a similar way, the TF of 4th order LPF introduced to the system can be derived as:

$$T_{f4th} = \frac{(CR_2s + 1)[C(R_1 + R_2)s + 1]}{[C(R_1 + R_2)s + 1]^2} \quad (6)$$

Combining equation (1) and equation (6) the TF of the system after introduction of the 4th order LPF in the loop can be derived as:

$$H(s) = \frac{K_d T_{f4th} \frac{K_0}{s}}{1 + \frac{k_d T_{f4th} K_0}{Ns}} \quad (7)$$

The TF of a conventional PID controller can be expressed as:

$$T_{fpid} = K_p[1 + \frac{1}{t_i s}] \quad (8)$$

If we combine equations (1) and equation (8) the overall TF of the system after replacement of the LPF by the PID controller can be derived as:

$$H(s) = \frac{K_d T_{fpid} \frac{K_0}{s}}{1 + \frac{K_d T_{fpid} K_0}{Ns}} \quad (9)$$

Equations (3), (5), (7) and (9) are used for analysis and experimental investigation of model.

((9) (9)

III. The Simulation

The model has been simulated on MatLab platform for a frequency range 0- 0.9GHz. Different parameters used for simulation is given in **Table 1**.

TABLE 1
PARAMETERS USED FOR SIMULATION

Symbol	Description	Value
k_{pd}	Phase Detector Gain	200×10^3
k_{vco}	VCO sensitivity	20×10^6
C_1	Loop Filter Capacitor	0.4261×10^{-9}
C_2	Loop Filter Capacitor	2.61×10^{-9}
R_1	Loop Filter Resistor	8.26×10^3
R_2	Loop Filter Resistor	10^3
$\frac{1}{N}$	Fractional Counter Value	2.22×10^{-4}

The simulated step response for the 2nd order PLL is shown in **Fig.2**. The step response of the 3rd order PLL is shown in **Fig.3**. The **Fig.4** shows the step response of the 4th order PLL. **Fig.5** shows the step response for the system when the LPF is replaced by a PID controller as shown in **Fig.1**. The Bode response of the system is shown in **Fig.6**.

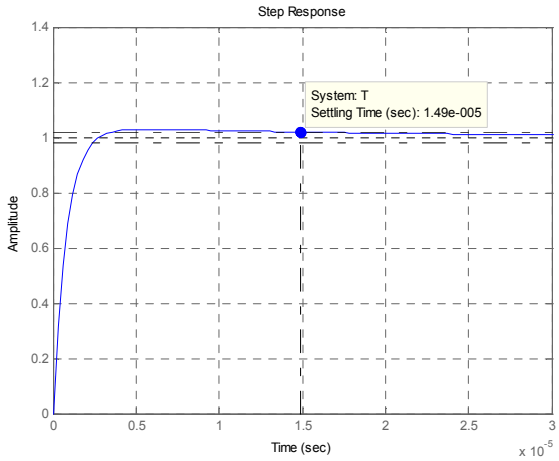

Fig.2: Step response for 2nd order PLL

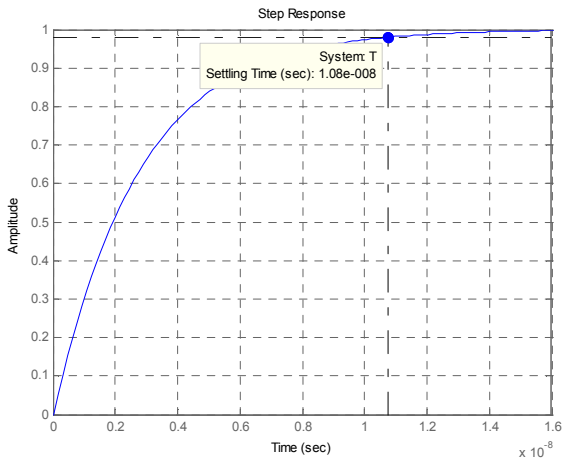

Fig.3: Step response for 3rd order PLL

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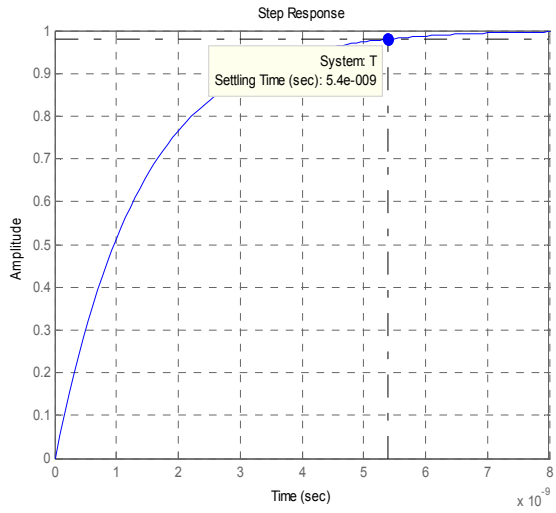

Fig.4: Step response for 4th order PLL

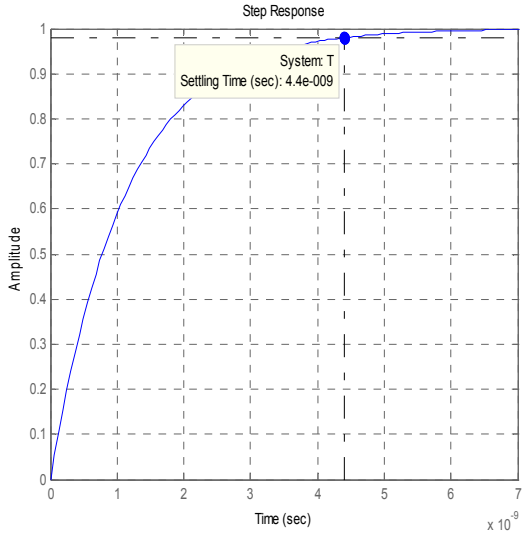

Fig.5: Step response, when LF is replaced by PID

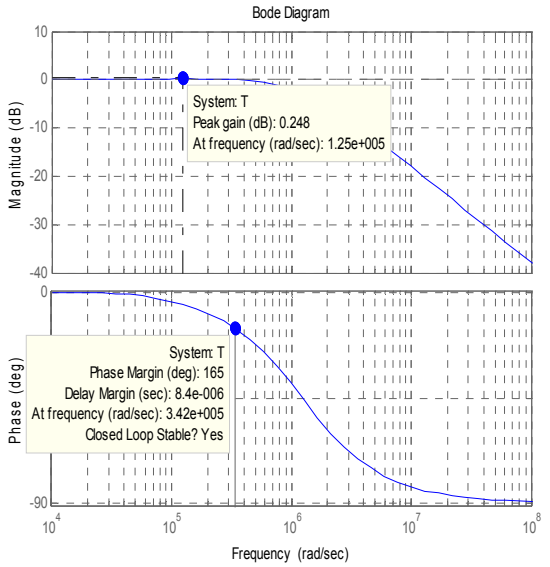

Fig.6: Bode plot of PID controlled PLL

IV. Results and Disscusion

The results of the responses of simulation are summarized in **Table 2.** It is observed that the method enables reducing the settling time up to 94%, 49% and 18% for 2nd, 3rd and 4th order PLL respectively. **Fig.6** shows the Bode diagram of the system while replacing the LPF by the PID controller. The phase margin of the system is 165 degree with a delay of 8.4×10^{-6} sec. It is also observed that the system is highly stable (poles are in the left hand side of the root locus plot). The settling time of the step response of the PID controlled PLL is 0.4528 sec for frequency ~0.9GHz.

TABLE 2
SIMULATION RESULTS

PLL order	Settling time (second)	Settling time with PID (second)	Improvement (in percentage)
2nd order	1.49×10^{-5}	4.4×10^{-9}	94
3rd order	1.08×10^{-8}		49
4th order	5.4×10^{-9}		18

V. Conclusion

The results will certainly provide PLL developers in research and industrial applications to develop their own PID controlled PLL, with an indication of the performance tradeoffs associated with current technologies.

The model developed may be suitable for high frequency FM transceiver due to its better settling time and stability.

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