A Novel High Performance Nanoscaled Dual Oxide Doping Less Tunnel Field Effect Transistor

Sajad A Loan*, *Member, IAENG,* Faisal Bashir, M. Rafat, M. Nizamuddin, Asim. M. Murshid, Abdul Rahman M. Alamoud and Shuja A. Abbasi

***Abstract*—In this paper, we propose a new structure of double gate dual oxide doping less tunnel field effect transistor (DG-DO-DL-TFET). The concept of charge plasma is used to realize source and drain regions in the proposed device. A 2D simulation study of the proposed device has been performed and the performance has been compared with a conventional double gate dopingless TFET (DG-DL-TFET). The simulation study has shown a significant improvement in *ON* current, I_{ON}/I_{OFF} ratio and in average subthreshold slope (SS_{av}). It has been observed that ~185% increase in I_{ON}/I_{OFF} ratio and 6.14 times enhancement in I_{ON} has been achieved in the proposed DG-DO-DL-TFET device in comparison to conventional DG-DL-TFET device. Further, a 30% improvement in SS_{av} is achieved in the proposed device in comparison to conventional device. The small signal ac analysis has shown that the cutoff frequency of proposed device (42.5GHz) has increased by 5.3 times in comparison to conventional device (≈8 GHz). Furthermore, since source and drain regions are not realized by conventional ways of ion implantation or diffusion, therefore, both the devices are free from random dopant fluctuations and can be processed at low temperature.**

***Index Terms*— Charge plasma, dual oxide, SOI, current gain.**

I. Introduction

The performance enhancement in MOS technology can be attributed to the scaling of the device dimensions. The scaling has significantly enhanced speed, power, functionality, packing density, reduced chip cost etc [1-2]. However, the scaling of dimensions below 32 nm is extremely difficult due to short channel effects (SCE), gate tunneling and other parasitic effects [3-4]. The magnitude of leakage current or static power dissipation has significantly increased in scaled device. Further, the supply voltage V_{DD} need to be scaled down with the scaling in device dimensions, to keep the electric field below its critical value. However, V_{DD} scaling degrades the performance of the device and hence threshold voltage V_{th} is bound to be scaled down to increase the overdrive for high performance. The scaling of V_{th} significantly increases the leakage current and in turn static power. An important approach to reduce leakage power and at the same reduce the operating voltage V_{DD} is to use the tunnel field effect transistors (TFETS). Since in a conventional MOSFET subthreshold slope (S) cannot be less than 60 mV/decade limit, hence it is the need of the hour to go for devices with *S* lower than 60 mV/decade [5-6].

Tunnel FET is a device of interest to researchers nowadays. It has steep subthreshold slope, less than 60mV/dec, possesses very low OFF current, have improved short channel effect performance and are the promising candidates for low power applications. With TFETs supply voltage can be reduced below 0.5V without performance degradation. However, TFETs have a major issue of poor ON-current (I_{ON}) due to large tunnel width. The ambipolar nature of these devices and random doping fluctuations are other issues which increases the leakage current in these devices [7-13].

In this paper, a new tunnel FET is designed and simulated using Atlas [12]. The source and drain regions of the device are realized by using charge plasma mechanism [13-17], where metals of appropriate work functions are used to induce *n* and *p* type charge plasma. Further, the proposed device uses dual oxide, hafnium oxide under source and silicon diode under drain regions. The dual oxide TFET has also been studied in [18-19]. The simulation results have shown that the proposed double gate dual oxide doping less tunnel field effect transistor (DG-DO-DL-TFET) outperform the conventional double gate dopingless TFET (DG-DL-TFET) significantly. The comparative analysis through 2D simulations has revealed that a significant improvement in *ON* current, I_{ON}/I_{OFF} ratio and in average subthreshold slope (SS_{av}) is achieved in the proposed device. It has been observed that ~185% increase in I_{ON}/I_{OFF} ratio and 6.14 times enhancement in I_{ON} has been achieved in the proposed DG-DO-DL-TFET device in comparison to conventional DG-DL-TFET device. Further, a 30% improvement in SS_{av} is achieved in the proposed device in comparison to conventional device. Further, it has been observed from the small signal ac analysis that the cutoff frequency (f_T) of proposed device (42.5GHz) has increased by 5.3 times in comparison to conventional device (≈8 GHz). Furthermore, since source and drain regions are not realized by conventional ways of ion implantation or diffusion, therefore, both the devices are free from random

Manuscript received March 22, 2014; revised April 4, 2014. The authors would like to acknowledge the support from NPST Saudi Arabia (11-NAN-2018-02). Dr. Sajad A Loan is associated with Jamia Millia Islamia (Central University) New Delhi, where he works as a Sr. Assistant Professor. (*Corresponding author: sajadiitk@gmail.com). Faisal Bashir, Humyra Shabir and M. Nizamudin are also associated with Jamia Millia Islamia, where they are pursuing their PhD. Prof. M. Rafat is also associated with Jamia Millia Islamia, New Delhi. Dr. Asim. M. Majeed is associated with Kirkuk University Iraq. Prof. Shuja A. Abbasi and Prof. Abdul Rahman Alamoud are associated with the Electrical Engineering Department, King Saud University.

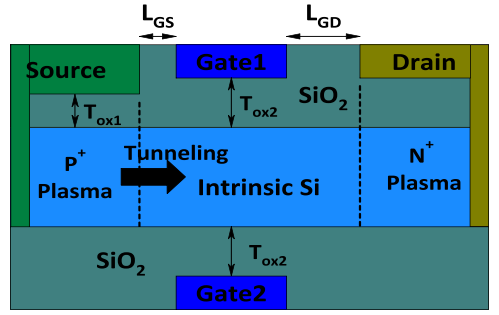
ISBN: 978-988-19252-7-5
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

dopant fluctuations and can be processed at low temperature [20-22].

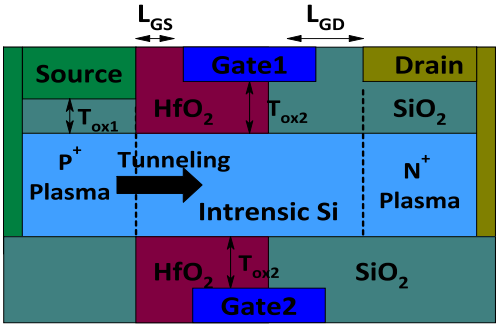
This paper is divided into four sections. Section II discusses various device structures and parameters. The simulation results and discussion have been discussed in section III. The conclusion is given in section IV.

II. DEVICE SCHEMATICS AND PARAMETERS

Figure 1 shows the schematic diagrams of DG-DO-DL-TFET and the conventional DG-DL-TFET devices. The parameters used in simulation study include oxide thicknesses (t_{ox1} = 0.5nm and t_{ox2} = 3nm), channel length (L) = 50 nm, L_{GS} = 3 nm, L_{GD} = 15 nm oxide. The gate work function used is 4.5 eV in all the devices. In order to keep uniform carrier concentration throughout the Si thickness, thickness of undoped Si has to be kept less than the Debye length. For realizing *p*+ source and *n* drain regions, platinum (work function = 5.93 eV) and hafnium (work function = 3.9 eV) is employed as the source metal electrode and a drain metal electrode.



(a)



(b)

Figure 1: Schematic diagrams of (a) Conventional DG-DL-TFET (b) Proposed DG-DO-DL-TFET

The device structures shown in Figure1 have been simulated using Atlas device simulator. Various models that have been used are drift-diffusion current transport model; Lombardi mobility model and concentration dependent SRH recombination model. Non local band to band tunneling (BTBT) model is used to account for the spatial profile of the energy bands.

III. RESULTS AND DISCUSSION

The carrier concentration induced in the proposed device by the charge plasma method is shown in Figure 2, taken along a cross section at a distance of 1nm away from silicon-oxide interface. It shows induced carrier concentration for both equilibrium state (with V_{DS} = 0V and V_{GS} = 0V) and non-equilibrium state (with V_{DS} = 1V and V_{GS} = 1.5V). The

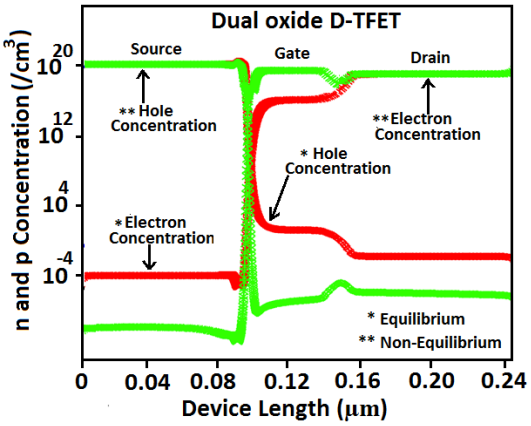
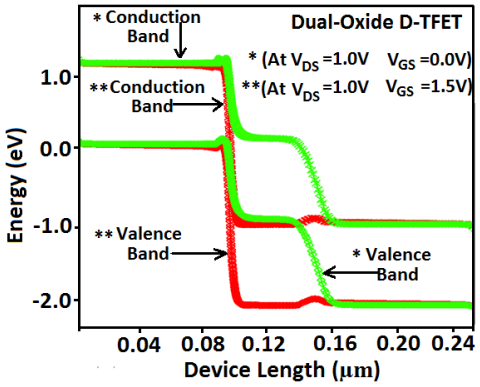
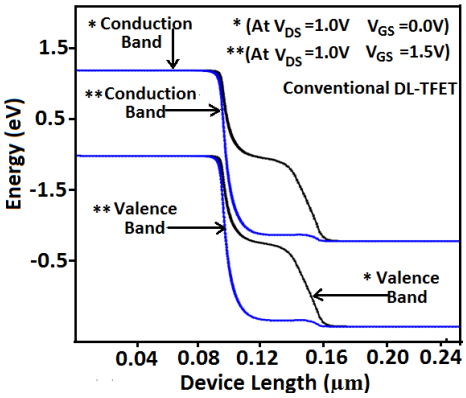


Figure 2: Electron and hole concentrations of the Proposed Dual oxide D-TFET under thermal equilibrium and ON-state conditions



(a)



(b)

Figure 3: Valence and conduction band energy in the OFF-state (V_{GS} = 0V,V_{DS} = 1.0 V) and ON-state (V_{GS} = 1.5V, V_{DS} = 1.0 V) for (a) Proposed Dual oxide D-TFET and (b) conventional D-TFET.

The energy band diagrams of both conventional and the proposed TFETs in the ON-state and OFF-state are shown in Figure 3. In the ON-state, the valence band energy levels of the source side are aligned with the conduction band energy levels of the channel in both the sturctures. This reduces the tunnel width in the ON-state, increasing the tunneling probability and hence increases the ON current. From Figure 3, it is clear that the tunneling width in case of proposed DG-DO-DL-TFET device is smaller as compared to conventional DG-DL-TFET device. The reduction in tunneling width is caused by using high-k dielctric gate oxide on the source side. It has resulted in considerable

ISBN: 978-988-19252-7-5
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

improvement in ON current, I_{on}/I_{off} ratio and *SS* in comparsion to conventional D-TFET. The transfer characteristics of proposed and conventional D-TFET are shown in Figure 4. The threshold voltage used over here is the voltage corresponding to 10^{-7} A/μm for both the devices. It has been observed ON current and I_{on}/I_{off} ratio are significantly higher in the proposed device in comparison to the conventional device. It has been observed that ~185% increase in I_{ON}/I_{OFF} ratio and 6.14 times enhancement in I_{ON} has been achieved in the proposed DG-DO-DL-TFET device in comparison to conventional DG-DL-TFET device. Further, a steep subthreshold slope is achieved in the proposed device. A 30% improvement in SS_{av} is achieved in the proposed device in comparison to conventional device.

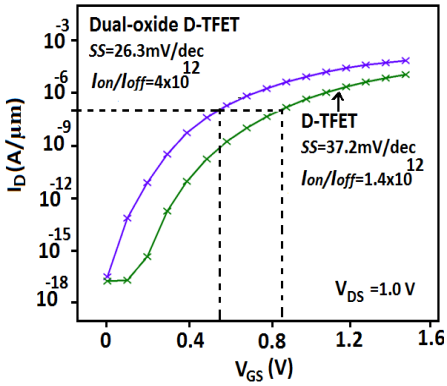


Figure 4: Transfer characteristics of the Proposed DG-DO-DL-TFET device and conventional DG-DL-TFET.

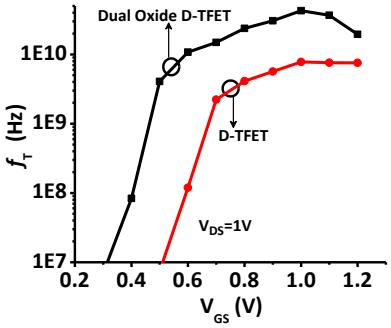
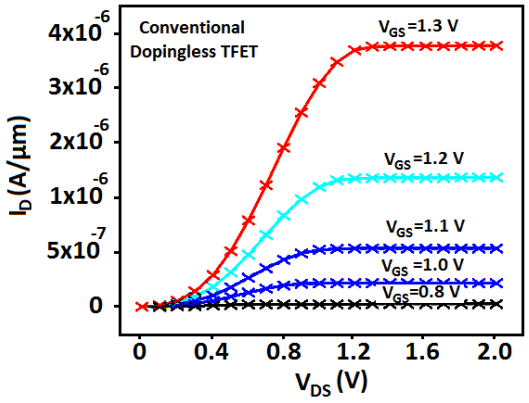
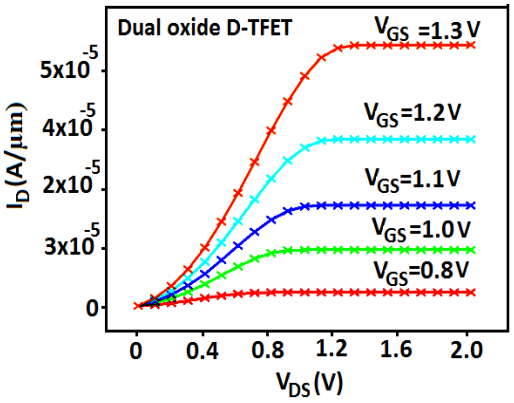


Figure 5: Cutoff frequency (f_T) comparsion of Proposed Dual oxide D-TFET and conventional D-TFET.



(a)



(b)

Figure 6: Output characteristics of conventional (a) D-TFET (b) Proposed Dual oxide D-TFET.

The ac analysis of both the conventional and the propose devices have been performed to see the cutoff frequency (f_T) of the devices. it is clear from Figure 5 that the proposed DG-DO-DL-TFET device has a significantly large f_T in comparison to the conventional DG-DL-TFET device. The large f_T can be attributed to high transconductance and large ON current in the proposed device due to efficient tunneling in the device. The small signal ac analysis has shown that the cutoff frequency of proposed device (42.5GHz) has increased by 5.3 times in comparison to conventional device (≈8 GHz). The output characteristics of both the devices have been performed and are shown in Figure 6. As is clear from Figure 6 both the devices have reasonable large breakdown voltage.

IV. CONCLUSIONS

In this work, a new structure of a tunnel FET is designed and simulated using Atlas simulator. The proposed device is a dual gate dual oxide and uses the concept of charge plasma to realize source and drain regions. A 2D simulation study of the proposed device has been performed and it has been observed that the proposed DG-DO-DL-TFET device has outperformed the conventional DG-DL-TFET device in almost all aspects. The ON current, I_{ON}/I_{OFF} ration and SS_{av} has significantly improved in the proposed device. The cutoff frequency of proposed device (42.5GHz) has increased by 5.3 times in comparison to conventional device (≈8 GHz). Furthermore, the proposed device is free from the doping issues, like the random doping fluctuations, and hence can be processed at low temperature as it is not using ion implantation or diffusion for realizing doped source and drain regions.

REFERENCES

[1] R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. Leblanc, "Design of ion-implanted MOSFETs with very small physical dimensions," *IEEE J. Solid-State Circuits*, vol. SSC-9, no. 5, pp. 256–268, Oct. 1974.

[2] G. Baccarani, M. R. Wordeman, and R. Dennard, "Generalized scaling theory and its application to a 1/4 micrometer MOSFET design," *IEEE Trans. Electron Devices*, vol. ED-31, no. 4, pp. 452–462, Apr. 1984.

[3] F. Ellinger, M. Claus, M. Schroeter, and C. Carta, "Review of advanced and beyond CMOS FET technologies for radio frequency

ISBN: 978-988-19252-7-5
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

circuit design, in *Proc. SBMO/IEEE MTT-S IMOC*, Oct. 2011, pp. 347–351.

[4] T. Skotnicki, "Heading for decananometer CMOS—Is navigation among icebergs still a viable strategy," in *Proc. ESSDERC*, pp. 19–33, 2000.

[5] S. A. Loan, S.Qureshi and S. S. K. Iyer, "A novel partial ground plane based MOSFET on selective buried oxide: 2D simulation study" *IEEE Trans. Electron Devices, no.* 57, pp. 671–80, 2010.

[6] V. Nagavarapu, R. Jhaveri, and Jason C. S. Woo, "The Tunnel Source (PNPN) n-MOSFET: A Novel High Performance Transistor", *IEEE Trans. Electron Devices, no.* 4, vol. 55, pp. 1013-1019, 2008.

[7] A. M. Ionescu and H. Riel, "Tunnel field effect transistors as energy efficient electronic switches, Nature, vol. 479, pp. 329-337, 2011.

[8] S. Banerjee, W. Richardson, J. Coleman and A. Chatterjee, "A new three-terminal tunnel device". *IEEE Electron Device Lett. vol.*8, pp. 347–349, 1987.

[9] E. Takeda, H. Matsuoka, Y. Igura, and S. Asai, "A band to band tunneling MOS device B2T-MOSFET", *Tech. Digest IEEE Int. Electron Devices Meet. pp*. 402–405 (IEEE, 1988).

[10] T. Baba, Proposal for surface tunnel transistors. *Jpn. J. Appl. Phys.* 31, L455–L457, 1992.

[11] A. C. Seabaugh, and Q. Zhang, "Low voltage tunnel transistors for beyond CMOS logic". *Proc. IEEE* 98, 2095–2110, 2010.

[12] *ATLAS Device Simulation Software*, Silvaco Int., Santa Clara, CA, USA, 2012.

[13] B. Rajasekharan, R. J. E. Hueting, C. Salm, *et al.*, "Fabrication and characterization of the charge-plasma diode," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 528–530, Jun. 2010.

[14] R. J. E. Hueting, B. Rajasekharan, C. Salm, *et al.*, "Charge plasma P-N diode," *IEEE Electron Device Lett.*, vol. 29, no. 12, pp. 1367–1368, Dec. 2008.

[15] M. J. Kumar and K. Nadda, "Bipolar charge-plasma transistor: A novel three terminal device," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 962–967, Apr. 2012.

[16] M. J. Kumar and S. Janardhanan, "Doping-less tunnel field effect transistor: Design and investigation," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3285–3290, Oct. 2013

[17] S. A. Loan, F. Bashir, M Rafat, A. R. Alamoud and S. A. Abbasi, "A high performance charge plasma based lateral bipolar transistor on selective buried oxide, Semicond. Sci. Technol. Vol. 29, 2014.

[18] S. Saurabh and M. J. Kumar, "Investigation of the novel attributes of a dual material gate nanoscale tunnel field effect transistor," *IEEE Trans. Electron Devices*, vol. 58, no. 2, pp. 404–410, Feb. 2011

[19] K. Boucart and A. M. Ionescu, "Double gate tunnel FET with high-k gate dielectric," *IEEE Trans. Electron Devices*, vol. 54, no. 7, pp. 1725–1733, Jul. 2007.

[20] M.-H. Chiang, J.-N. Lin, K. Kim, and C.-T. Chuang, "Random dopant fluctuation in limited-width FinFET technologies," *IEEE Trans. Electron Devices*, vol. 54, no. 8, pp. 2055–2060, Aug. 2007

[21] N. Damrongplasit, C. Shin, S. H. Kim, R. A. Vega, and T. J. K. Liu, "Study of random dopant fluctuation effects in germanium-source tunnel FETs," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3541–3548, 2011.

[22] A. Mallik, A. Chattopadhyay, S, Guin and A. Karmakar, "Impact of a Spacer–Drain Overlap on the Characteristics of a Silicon Tunnel Field-Effect Transistor Based on Vertical Tunneling, IEEE Trans Electron Devices, vol. 60, pp. 935-943, 2013

ISBN: 978-988-19252-7-5
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)