Converting Binary Data To NRZ signal for RFID and Biomedical Applications

Gihad. A. Elamary, *Member, IAENG,* E.G. Chester

Abstract— **In this work, we proposed a simple new circuit design to convert binary data into a non return to zero (NRZ) signal. These techniques were applied in analogue modulation schemes for radio frequency identification (RFID) applications, and these may suitable for biomedical purposes. The proposed circuit steps down the input signal below a zero level by the value of ($-V_{EE}$). The negative signal drives the transistor switch. The output of the switch provides a NRZ signal. The circuit has been designed for low power consumption and hand-held applications for biomedical purposes or RFID. Our proposed circuit has been simulated and evaluated by measurements of performance.**

Index Terms— NRZ signal,RFID security system, BPSK Modulator, Biomedical,Medical Health Care,

I. Introduction

RFID and Biomedical systems are widely applied today in wireless technology for communication between tags and readers. Modulated with analogue or digital schemes in the near field, these technologies are rapidly applied, for many applications such as wireless security systems, medical health care and implant sensors [1] [2] [3] [4]. There is a requirement for handheld devices and low cost readers with high data rate. The information data are transmitted and modulated with digital schemes such as BPSK, which has advantages over other schemes such as ASK or FSK [5]. The BPSK modulation has advantages such as having a fixed carrier signal amplitude that provides a stable wireless transfer power and independent data modulation [6]. However, this type of modulation needs a NRZ form signal, thus some technique is essential to convert the binary data into NRZ signal. To achieve a transition of the carrier (0, π), which is controlled by the input data, the BPSK signal can be represented mathematically in an analogue way as expressed in the equation (1). The data signal 'Data-input' *m (t)* has been generated by a PIN sequence and can be represented by Fourier series analysis as in equation (2) [7].

$$S_{BPSK}(t) = m(t)\sqrt{\frac{2E_b}{T_b}}Cos(w_{rf}t + \theta_{rf}) \qquad (1)$$

Manuscript received (March 23, 2013). Gihad. Elamary, The professional institute of electronics/ Dr. Graeme Chester Department of EEE, Newcastle University School of EEE-Newcastle University, UK,-NE1 7RU. Phone: E-mail: (gihad.elamary1@ncl.ac.uk)-(graeme.chester@ncl.ac.uk).

$$PN(t) = \sum_{n=-\infty}^{\infty} c_n\, p(t - nT_c) \qquad (2)$$

$$where \quad m(t) = PN(t)$$

Our purposed circuit has been interfaced to the modulator to provide a BPSK signal as demonstrated in Fig. 1. In practice the binary data *m (t)* is converted to a NRZ signal that maps the logic'0' to -1V (nominal) and the logic '1' to+1V. This data signal has controlled the transition shift $(0, \pi)$ for the carrier frequency signal, as shown in Figure 2.

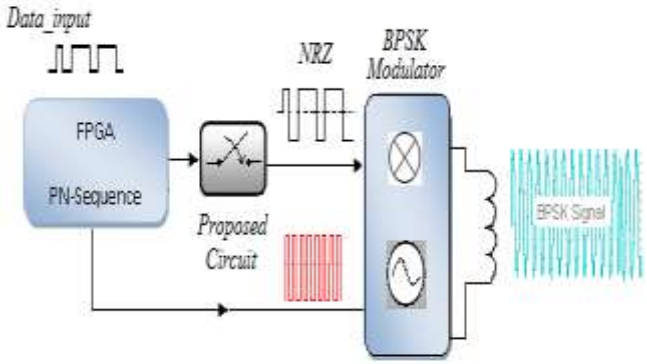

Figure 1: the proposed circuit with BPSK Modulator

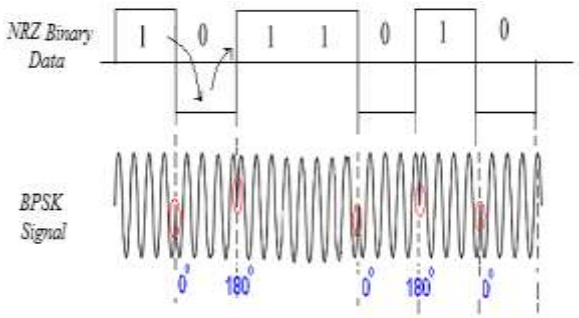

Figure .2 illustrates the BPSK waveform with respect to (NRZ) data state

II. Theory Method of the Circuit

The theory of the proposed circuit has been analysed and the principle of the pulse signal has been demonstrated in the block diagram as shown in Fig. 3. The mathematical analysis can be expressed in the equations for the input and output data signals [8], [9]. The input pulse signal can be expressed in equation (3) with Fourier series analysis, and in the equation (4) is presented the processing by the inverter circuit of the square wave signal output.

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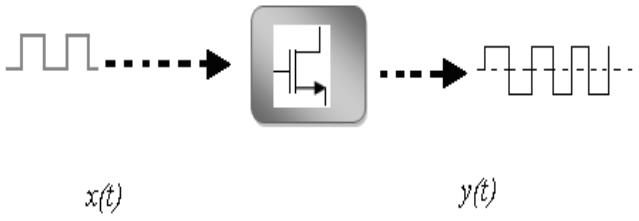

Figure 3: the block diagram of the NRZ convertor

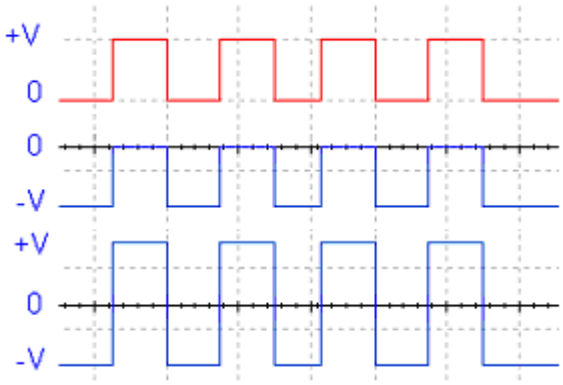

Figure 4: the waveforms of the pulse processing signals

$$z(t) = \frac{2V}{\pi} \sum_{n-1}^{\infty} \sin(2\pi ft) \tag{3}$$

$$y(t) = \frac{4V}{n\pi} \sum_{n=odd}^{\infty} \frac{1}{n} \sin(2\pi ft) \tag{4}$$

The external circuit is used as the input data source which generates a PN sequence, feeding a clock driver circuit as booster for the output pulse signal, then inverted by the Inverter. After that it is stepped down to the negative level by Switched Capacitor Voltage Converter. The signal controls the gate of a MOSFET-Transistor. The transistor is working as a switch element in the circuit which combines the positive and negative pulse signals to produce the squared output signal. This output is applied into the BPSK modulator, then the output is filtered for transmission.

III. Proposed Circuit Description

The proposed circuit has been demonstrated in Fig. 5. Generally it is divided into two parts. The first part is the external data source and clock driver, the second part is the inverter and the switch circuits. The control switch circuit consists of the integrator that is controlled by the negative voltage for step down the level of data signal as illustrated in Fig. 6. The negative pulse is driving the transistor switch for selecting the positive and negative pulses. In addition, the capacitor is used to block the DC bias voltage. The switched capacitor DC-DC voltage converter is capable of converting the positive Dc voltage input (+V) to a corresponding negative DC voltage (-V). The chosen device LMC7660 from National semiconductor [10] is used to work with the range (-1.5V) to (-10V) with low power consumption (200µA) . In practice, additional circuitry has been modified to adjust the DC bias from (-0.5 V to -5V) to drive the integrator RC circuit (C, R3) to the right level.

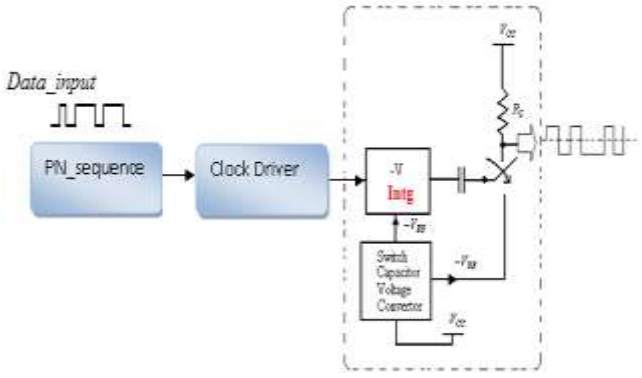

Figure 5: the proposed diagram for the converter binary data in to NRZ signal

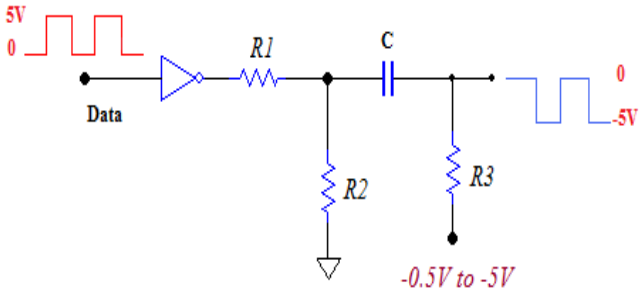

Figure 6: the level shifter circuit for driven the DC bias up to -5V

IV. Simulation Circuit for NRZ

The proposed system design shown in Fig.5 has been simulated and evaluated to produce the NRZ signal; which is generating a bipolar signal as data source. The simulation results for the circuit have provided a square signal from the pulse signal as shown in Fig. 7. On channel CH1 is presented the input data signal at 125Kbps, and on CH2 is presented the negative pulse signal. Finally channel CH3 illustrates the square output signal. The circuit has been simulated with different frequencies to evaluate the performance of the circuit when tested at data rates up to 3Mbps over a carrier frequency of 13.56 MHz. The algorithm of the PN-sequence has been synthesized in VHDL code, and there are many techniques which can be used to generate the code sequence [11]. This simulates the command information which is used as a data source either in the reader part or tag and implant device. The PN generator here has been synthesized by VHDL code using the Altera development kit [12]

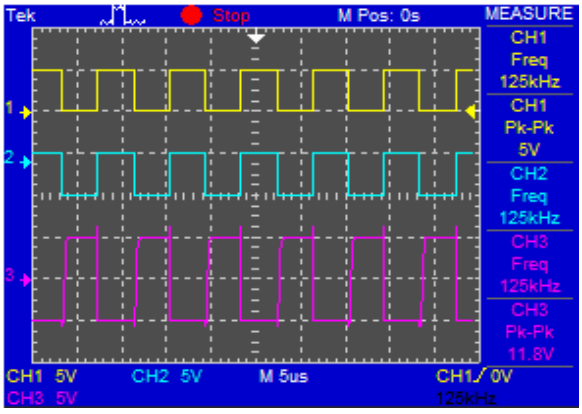

Figure 7: The simulation result of proposed circuit

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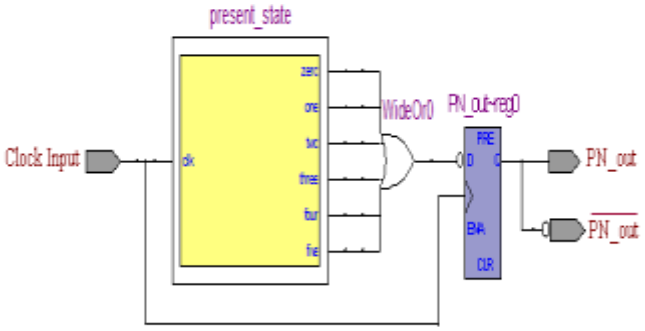

Figure 8: The block diagram of PN sequence generated By VHDL code

V. EXPERIMENTAL RESULTS

The prototype circuit in Fig. 9 has been implemented and evaluated experimentally to generate a square bipolar signal. The data source has been synthesized with different clock frequencies using a PN sequence signal. In this work we generated the PN signal by VHDL code. In addition, the desired carrier at 13.56 MHz has been produced by VHDL code. The lab setup measurements for our proposed circuit have been illustrated in Fig. 9. The first measurement result for the circuit has been performed for stepped down integrator RC as shown in Fig. 10, where at the top CH1 shows the input pulse signal; while channel CH2 shows the stepped down output signal. The second set of measurements has been performed for the proposed circuit, as illustrated in Fig. 11, at data rate of 256 kbps. However, the circuit has been tested at up to 2.5 Mbps.

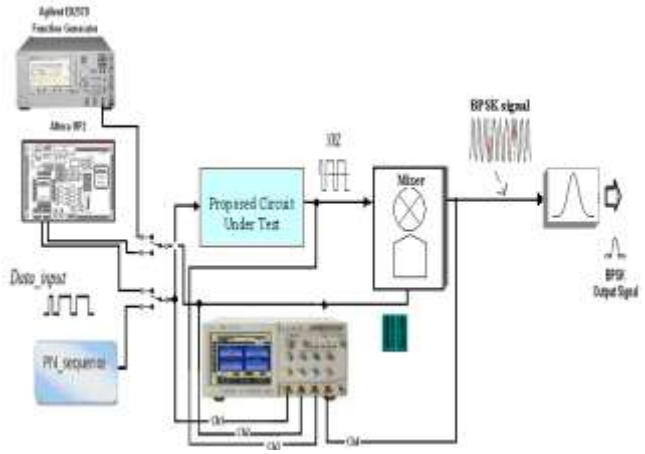

Figure 9: Lab setup test measurements for the proposed circuit

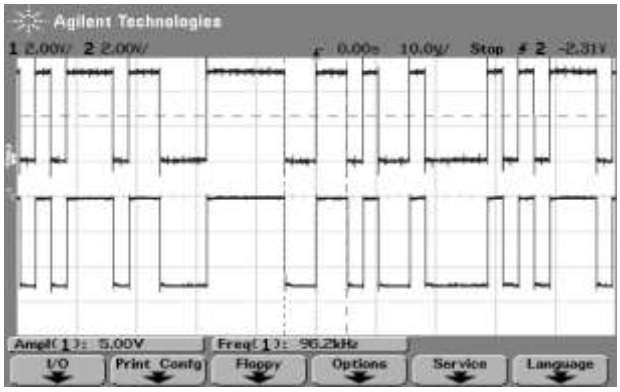

Figure 10: The input pulse signal and stepped down pulse signal

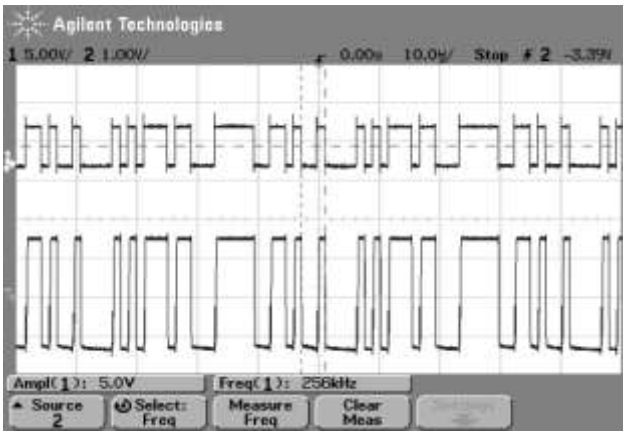

Figure 11: the output measurement results for NRZ signal

VI. CONCLUSION

In this paper, we have demonstrated a new simple circuit design for generating the NRZ signal from binary data. It uses control of the switch transistor (ST) to produce a square signal. The data bits are inverted and followed by a circuit which consists of a passive integrator fed with a negative voltage. The switch transistor is clocked by a negative pulse for selecting between positive and negative voltages. The output of the ST is a square 'Bipolar base band digital signal'. Generally, we focus in this work on designing a simple circuit for hardware implementation and low power consumption , which is able to work from a battery. However, the PN sequence has been produced with VHDL using a CPLD (EPM3064) as a part of the reader unit, to reduce the hardware. Finally the circuit can work with higher carrier frequencies, when used with CMOS full-custom technology.

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