An Innovative Design of ADC and DAC Based Phase Locked Loop

Koushalya Ramakanth, and Lili He, *Member, IAENG*

***Abstract*— The project aims at designing an analog phase locked loop based on digitally controlled feedback loop wherein the digital control loop gathers the locking information in digital blocks. The loop consists of analog components such as phase detector, loop and oscillator and digital components in the feedback loop. Therefore, this architecture facilitates low power digital logic. When on low power mode, the phase locked loop is turned off, the locking information stored in the digital control loop are retained thereby avoiding delay when the loop is relocked when turned on.**

The design is implemented using 45nm CMOS technology. This architecture gives an area advantage to the system as compared to the digital phase locked loop. The design is estimated to function between 2 to 6 Gb/s.

***Index Terms*—phase locked loop, low power digital logic.**

I. Introduction

The Phase locked loop has a lot of applications ranging from communications to electronic circuit for both digital and analog blocks. Phase locked loop has applications in wireless communications wherein the frequency synthesis method of transmitting signals in a communication channel between the transmitter and the receiver is widely in use and has benefitted the communication industry in many ways. The emerging market, demands for a compact, lightweight, movable electronic appliances. The density, size and the complexity of the circuits and their functions continue to hike and hence the design of low power circuits becomes a major scientific challenge in order to make a product/system more flexible and vulnerable in handling more functions into one single part of the circuitry and which would carry out the functions easily with less power and the topic is restricted with CMOS circuits.

Therefore the design of the phase locked loop for low power circuit applications has become important. The phase locked loop circuitry consisting of the oscillators and the passive components in conjunction with the other components of the IC are required to operate on a wide range of frequencies in a communication system and the use of phase locked loop in these applications is proved to be efficient.

Phase locked loop is a circuit which has an oscillator whose voltage is controlled by constantly adjusting to match with the phase of the frequency of the signal input [1]. It has a feedback loop to harmonically match the clock of the circuit with the external clock. Practically the phase locked loop work to match the phase of the signal generated by the voltage controlled oscillator with that of the reference signal [1]. The phase and the frequency error difference signals of the input signal and the divider output signal are preserved as analog voltages at the loop filter output which is then followed by the VCO. This happens in an analog phase locked loop with the limitation that the analog voltages will be lost if any of the other component blocks of the PLL would switch off or become inactive [3].

Hence to avoid the loss of any information of the locking pulses, a DAC and up-down counter loop supplants the filter which performs the function of preserving the lock information of the signals as digital codes. Therefore the loop preserves the digital form of the locking information even when the other components of the PLL are inactive or when working in low power [3]-[4].

II. Review of Phase Locked Loop

A. Analog PLL

Any analog PLL consists of a phase detector and a charge pump. But when there is a significant mismatch in the frequency of the input signal and the VCO generated output, the PLL has a very few frequency range to get locked. Hence to enhance the lock acquiring ability with a broader frequency range of acquisition, phase frequency detector is used in preference of the phase detector [8].

The charge pump is therefore not required as the phase frequency detector provides the up down pulses required by the counter and DAC loop to achieve easy locking. Figure 1 shows a common analog PLL block with a charge pump and loop filter.

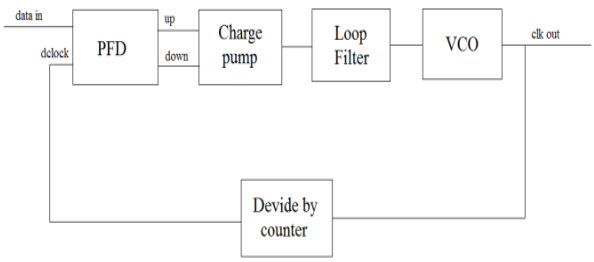

Figure 1. Analog PLL with charge pump and loop filter [8]

B. Digital PLL

An all-digital PLL are designed by substituting all the analog components with digital blocks. Although the digital

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The authors are with San Jose State University, Department of Electrical Engineering, San Jose, CA 95192-0084,USA. (Corresponding author, phone: 408-924-4073; fax: 408-924-3925; e-mail: lili.he@sjsu.edu).

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PLL helps in preserving the lock information as digital codes in the loop, it has certain disadvantage that makes the design not suitable for low power mode [8]. In order to reduce phase noise and jitter, the delay of each block in a digital PLL must be minimized. To keep the clock period stable through the different stages of the block, a number of blocks that contributes smaller delays should be used. This would increase area and power consumption. The module shown in the figure 2 is a typical digital PLL.

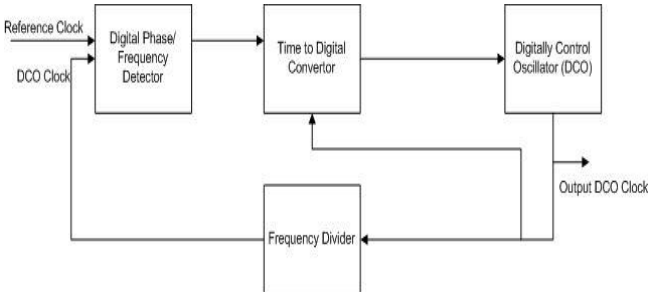

Figure 2. Digital PLL [8]

III. Design and Simulation

A. Architectural Block

The architectural design of the proposed phase locked loop comprises of blocks such as Phase detector, which produces error signals up and down signals, counter which generates outputs that are built using adders and D flip flop based up/down counter, current steering DAC, VCO and divider. The design of analog PLL includes DAC and ADC counter loop that aids in reducing area and power consumption.

1) Phase frequency detector: The phase detector is an important block of PLL which generates difference signal. The difference in the phase between the two input signals of the phase detector are generated as up and down pulses depending upon the phase lagging and phase leading of the reference input signal with that of the divider output signal [1], [8].
2) Up down counter: The up down counter also called the ADC block converts the up down pulse signals from the phase frequency detector to digital bits. The block acts as an ADC and the digital codes of the up down signals are fed to the DAC stage [3]- [4].

3) DAC loop: The DAC in the PLL has decoders which selects the digital inputs and converts it into analog current signal in the current cell block [4]. The analog voltage of the current signal generated from the DAC block is given as a control voltage signal to the VCO.

4) Voltage controlled oscillator: The VCO converts the control voltage of the input signal to frequency signal to latch with the input signal frequency of the phase frequency detector [8].

5) Divider: The frequency divider block makes the oscillator output signals in sync with the frequency of the input reference signal [8].

B. Phase Frequency Detector

The phase detector outputs UP and DOWN signals, wherein the UP signal is high or enabled if the frequency of the reference signal leads the frequency of the oscillator generated signal and the DOWN signal is high if the frequency of the reference signal lags the frequency of the oscillator signal [4].

The UP and DOWN error signals generated by the phase detector, decides the current coming into or going out from the capacitor, with a difference in voltage levels across the capacitor. This voltage affects the oscillator which controls the voltage and converts into frequency.

The UP and the DOWN signals also called the increment and the decrement signals have to be properly aligned and regulated for the appropriate voltages which would proceed to lessen the phase difference between the two signals of the Phase locked loop and would in turn help in locking the signal accurately.

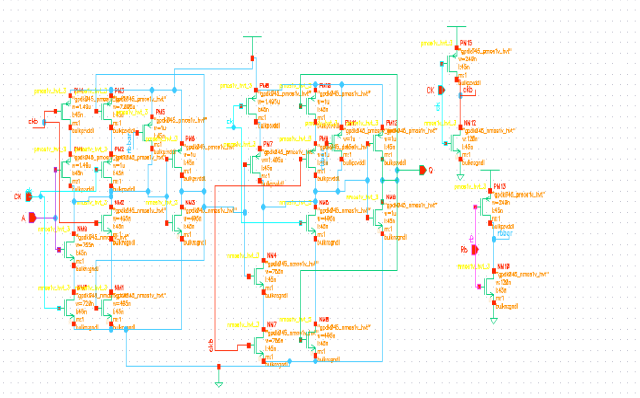

Figure 3. DFF Schematic used in Phase frequency detector

The schematic used in designing a phase frequency detector is a Dff as the circuit shown in figure 3, which is a transistor level schematic of D flip flop used in designing the phase frequency detector. The timing diagram of negative edge triggered D flip flop shown in the schematic is presented in the figure 4.

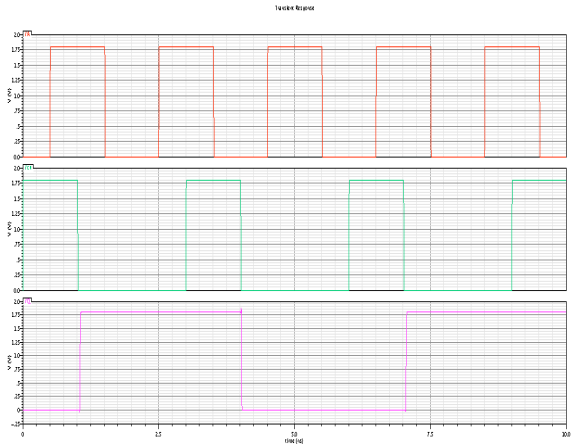

Figure 4. Simulation results of D flip flop

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In figure 4, the The phase frequency detector is built using two D flip flops whose outputs are connected to the input of the AND gate. The AND gate output resets the D flip flop if it's active or high. In figure 4, the x-axis is time in nano-second (ns) , and the y-axis is voltage in volts (V). Figure 5 shows the phase frequency detector block [1].

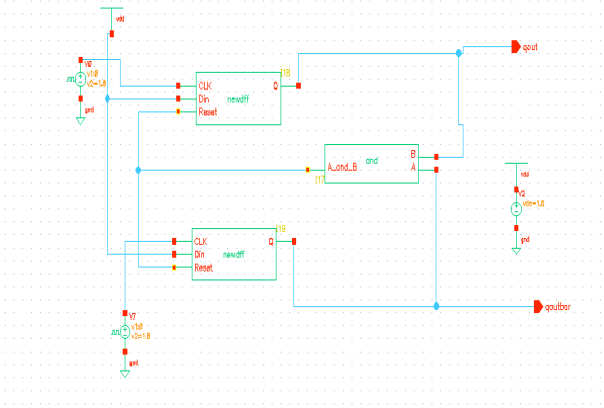

Figure 5. Phase frequency detector (PFD)

The PFD test bench is as shown in the figure 6 . The inputs to the PFD are the reference and the divider output signal and the output is an UP and DOWN signal and the reset signal to check whether the circuit has been reset or set.

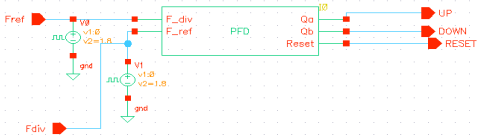

Figure 6. PFD test bench

A more comprehensive and optimized schematic of PFD can be shown in figure 7. As the circuit input of the D flip flop is always high, the circuit is optimized for high speed operation. The Qa and the Qb denotes the UP and DOWN signal respectively.

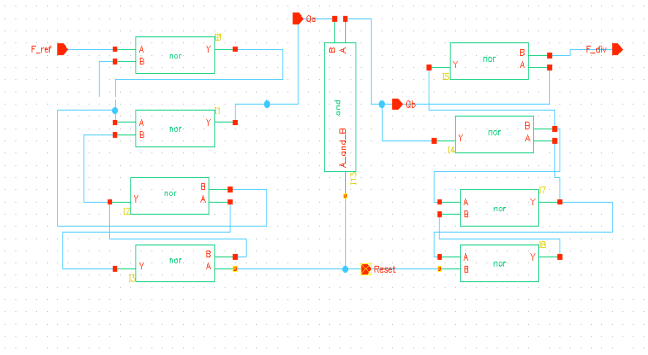

Figure 7. Optimized PFD block

The phase frequency detector can be recognized using the timing diagram. It shows that the UP signal is activated when the divider output signal is lagging the input signal and the DOWN signal is activated when the divider output signal is leading the reference input. The simulation results of the UP and DOWN pulses of the PFD with reset pulse are shown in the figure 8. In figure 8, the x-axis is time in nano-second (ns), and the y-axis is voltage in volts (V).

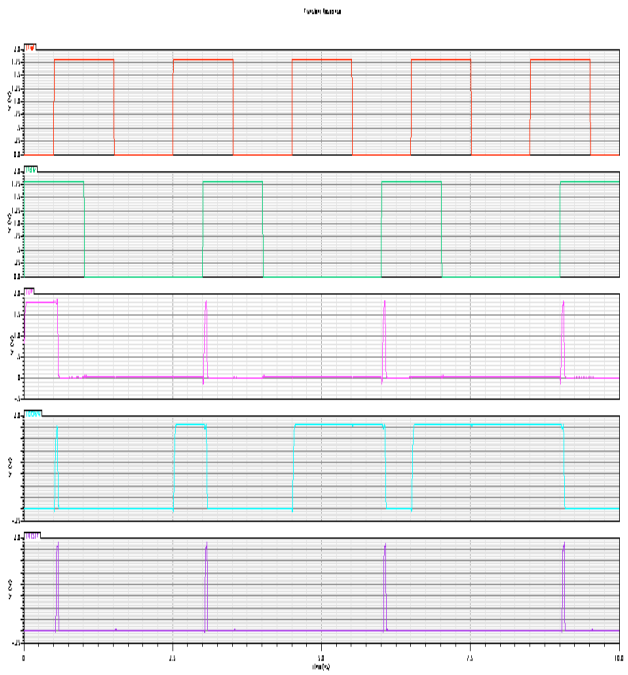

Figure 8. Simulation results of the PFD

C. *UP- DOWN Counter*

The Up-Down counter also called the Increment-Decrement counter takes the UP and DOWN signals as the input and converts the signal to digital codes which is given as inputs to the DAC [3]. The UP or DOWN signals are given to the increment and decrement counter which comprises or a ripple carry adders and D flip flops. The output carry out of the adder is given as input to the next adder and so on. The adder output sum is given to D flip flop which stores the added result and produces digital output. This acts as an ADC block which converts the analog input pulses into digital codes. The ripple carry adder can be shown in the figure 9 which takes the UP and DOWN signals as inputs from the PFD and the outputs are stored in D flip flop which outputs digital codes given to the next DAC block.

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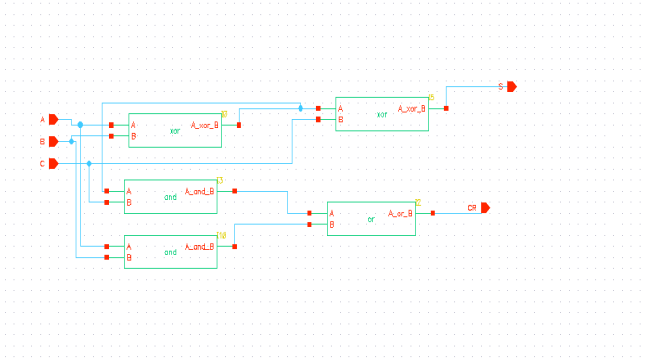

Figure 9. Adder block

The UP DOWN counter in combination with the DAC loop acts as a low pass filter to preserve the locking information. The UP DOWN counter is DFF and adder based counter which outputs digital code which is the input to the DAC. The counter according to the matrix of row and column decoder, counts the error signals the UP and DOWN signals and selects the appropriate signals given out by the phase detector and the adder and DFF block to keep a track of the changing error signals. This generates the appropriate digital code which is captured in the DAC when the other components of the loop are in low power mode or inactive. Hence the digital code is converted to analog signals and given to the oscillator which regulates the voltage of the phase and frequency signals to lock and align the signals of the phase locked loop.

The architectural block of the increment-decrement counter also called the up-down counter is a block of series of adders and D flip flops which have UP and DOWN pulses as inputs with the clock.

D. Digital to Analog Converter

The 10 bit thermometer DAC is used to convert the digital codes and gather the digital information of the signals for proper lock acquisition during power down mode. The DAC loop takes input from the counter and converts it into analog signal which is controlled by the oscillator to tune the frequency to harmonize or align with the reference input signal for the loop to be locked properly [6]. The DAC block consists of the following blocks: Selector and Current cell.

The selector block is a decoder which forms a matrix with the row and the column decoders to select the appropriate digital code. The selected decoder output is given to the current cell block to convert it into analog signal. The current cell has a current reference circuit connected in series. The output of the DAC block is analog current which is fed to the VCO wherein it is converted to frequency and locked to the frequency of the phase detector input signal [3] and [6].

D. Voltage controlled oscillator

The voltage controlled oscillator used in the design is a ring oscillator. The oscillator converts the controls the Figure 11 shows the VCO control input, the reference signal and the divider signal and analog current signal from the DAC. The reference signal and the divider signal are compared at the PFD and the up down signals are given to the counter ADC block to produce digital signals. These digital codes are given to the DAC where the digital codes voltage of the received input analog signal from the DAC and converts to frequency at the output which assists in locking with the frequency of the input signal of reference in the phase locked loop. This generated clock frequency of the oscillator aligns with the reference clock signal. This operation is called clock data recovery.

The ring oscillator is a series of digital inverters connected in a ring manner. The output of the Nth inverter is feedback as input to the first stage of inverter. To generate a constant DC signal inversion, odd numbers of inverters are connected in a loop. Assuming the output of the first inverters '0' , and second inverter output will eventually be '1' and so on the Nth stage output will be '0' with odd number of inverter stages. The Nth inverter output is connected to the input of the first inverter forming a ring and now the output of the first input will be '1' thereby switching again the output of the Nth inverter. This repetitive process results in oscillating voltages at each node of the inverters [7]-[8].

IV. PLL DESIGN

The complete schematic of PLL design is shown in figure 10. The resulti ng waveform of the overall loop is as shown in the figure 11. In figure 11, the x-axis is time in nano-second (ns), and the y-axis is voltage in volts (V).To prevent the loop from being affected by the stability , the output of the DAC is compared with the Up Down pulses from the PFD in the counter loop and the corresponding pulses are decoded and converted to digital codes in the ADC loop.

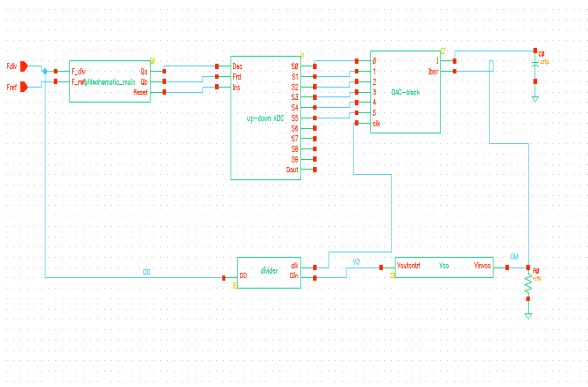

Figure 10. PLL schematic

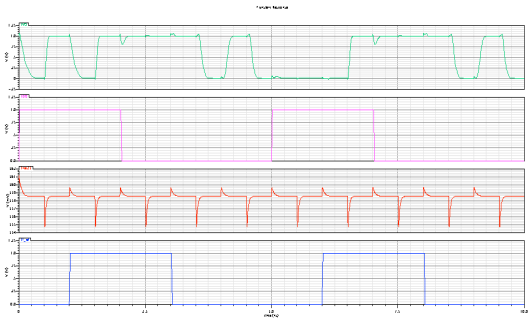

Figure 11. Simulation results of the PLL loop

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are converted to analog signal by the row and column decoders and the current source cell in the DAC block. The outputs of the DAC block are compared with the up down pulses in the ADC counter to align the output pulses again with that of the reference signal differences. The outputs of the DAC are given to voltage control inputs to the VCO and the VCO output is tuned to lock with the frequency of the reference input signal. The divider divides the VCO signal to align with the frequency of the reference input signal.

V.PLL SIMULINK MODEL

The top level module of the design is simulated in Simulink and the module is as shown in the figure 12. The top level module has a phase detector that produces the Up Down pulses which are fed as inputs to the increment decrement counter followed by DAC and VCO to control the voltage and align the frequency with respect to the input reference signal.

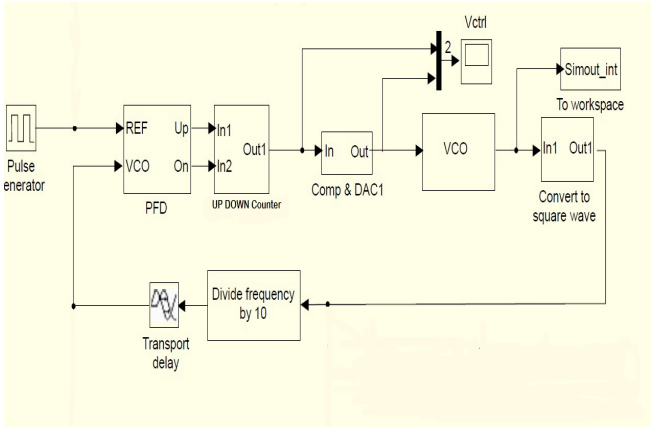

Figure 12. Simulink model of PLL

VI. CONCLUSION

An analog PLL with ADC of 10 bit resolution and a DAC acting as a digital control loop has been designed. The PLL with DAC in the control feedback loop helps in gathering the digital information of the pulse signals to be locked. The ADC and DAC combination aids in reducing area and power by storing digital bits of information when the components of the PLL goes to inactive state.

The PLL design is implemented in 45 nm CMOS technology. The PLL works at a frequency of 2Ghz with an input frequency of 0.3GHz. The PLL lock time is approximately 5us. The VCO wake up time when the system is re-switched back after the low power mode is found to be less than the VCO wake up time for any other analog PLL. The PLL design is evaluated by checking outputs at every stage of the PLL loop.

VII.FUTURE SCOPE

It is realized that the current design can be further enhanced by using higher resolution DAC to reduce jitter and improve output efficiency. The design can be upgraded to reduce area and power and to provide better stability. Higher resolution DAC will provide efficient locking of the loop and will minimize jitter for better performance. To avoid the ADC loop from affecting the stability of the whole system, the loop bandwidth of the ADC loop can be designed to be much wider than the loop bandwidth of the system loop.

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