Design of a Low Jitter PLL for Serializer/Deserializer Transmitter

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***Abstract*— This paper proposes a low jitter PLL using DAC for Serializer/Deserializer (SerDes) transmitter realized using 45nm technology. It aims at having lesser jitter, low power, for high speed applications using capacitive free blocks. The project analyzes and finds the best combination of digital and analog blocks (Digital PLL) that could be used to work at GHz speed. This project uses a bang-bang PD, Incrementer/Decrementer, Digital Filter, current steering thermometer coded DAC and Ring-VCO for achieving the best performance and low Jitter. The modified design of PLL will replace the analog charge pump and low pass filter with asynchronous Incrementer/decrementer, Digital FIR and current steering thermometer coded DAC and analog VCO. Advantages of doing that are some factors like cost, area and power savings.**

***Index Terms*—Digital to Analog Convertor, phase locked loop, low jitter**

I. Introduction

PHASE locked loop (PLL) is a negative feedback system where an oscillator output is phase and frequency matched to the reference/input signal. Due to this characteristic PLL's find widespread use in electronic circuits and communications. PLL's can be used to stabilize a communication channel and to generate high frequency clocks by making the divided down signal corresponding to the clock to be in sync with a low frequency signal.

PLL is considered a reliable source for clock generation. Today's electronic world is focused towards increasing the speed of the integrated chips mainly to the maximum possible level accompanied by compactness housing several billion electronic components in a small area. A phase locked loop has four main sub-blocks which includes phase detector, charge pump, low pass filter and voltage controlled oscillator. Analog parts in the low pass filter and charge pump such as resistors and capacitors play a vital role at high speed. Capacitive components also occupy the majority of area in the PLL.

II. The Proposed PLL Design and Implementation

This project involves modifying the PLL blocks for achieving an optimal performance and reducing the jitter at the transmitter of SerDes. This project would be using a digital PLL and DAC to model the various parameters to achieve the requited performance. In this project, the modified design of PLL will replace the analog charge pump and low pass filter with asynchronous Incrementer /decrementer, Digital FIR and current steering thermometer coded DAC and the analog VCO will be retained, the type of VCO used would be a ring VCO. The design would be done by weighing the advantages and disadvantages of each block in the PLL for this specific application.

The main focus will revolve around reducing jitter, low power and high speed by implementing a PLL which is hybrid to make some of the blocks as digital and retain some as analog due their properties and considering some parameters and feasibility for this specific application. The design would have PLL with DAC and an incrementer/decrementer block and digital FIR so that to reduce the capacitive and resistive components to achieve high speed due to lesser parasitic and lesser area. VCO will be retained as a analog component as digital VCO cannot achieve higher frequencies like the analog VCO. The design would be done by weighing the advantages and disadvantages of each block in the PLL for this specific application. Figure.1 shows the proposed PLL model.

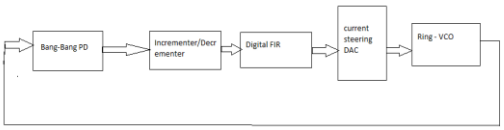

Fig.1. Proposed PLL model

In the PLL that will be implemented, we would use current steering thermometer, digital to analog convertor (DAC) and digital FIR filter to replace the LPF, to make the entire design capacitor free in order to reduce the delay and leakage current. Incrementer /Decrement are implemented and replace the charge pump which also contains the capacitive components. Leakage current is one of the most common sources of noise. Eliminating that would make the design work at higher frequencies.

This PLL will be designed and modeled for SerDes applications at 45nm technology. In the PLL, components such as phase detector (linear/non-linear), charge pump, analog filter and a voltage controlled oscillator occupies more than 80% of the total area. All components will not be designed in digital as a fully digital PLL would introduce

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quantization error at higher frequencies. In the modified design PD is retained, charge pump and filter is changed to digital domains which is incrementer/decrementer and DAC respectively.

A. Voltage controlled oscillator

Voltage controlled oscillator is one of the important blocks in the design of a phase locked loop. Here the oscillation frequency is controlled by the voltage applied at the input. Oscillator is a badly designed feedback system (positive feedback system). Ring Oscillator based VCO is most commonly used due to its easy integration and also due of the absence of capacitive and inductive components which introduce a lot of delay in the circuit.

1) Specifications for the VCO

- 8*3 Array of Ring oscillators
- 8 Phase clocks 1T apart[3]
- VCO work over a range of 2GHz to 6GHz
- VCO tune via current limiting[3]

The structure of array oscillator is mainly based on the coupled ring oscillators. Dependency of the frequency on the buffers can be broken by coupling many rings together. The delay resolution can be increased by the addition of rings. By doing this, all the rings will be forced to oscillate at the same frequency, which makes them uniformly offset in phase. This coupling creates this uniform spacing, which is the key idea for designing an array oscillator.

2) Design of 8*3 ring VCO

An array of the ring oscillators with the bias circuit is shown in figure 3. All the rings will be oscillating in the same phase. One of the inputs of the ring is called the coupling input and the other is the ring input [3]. Phase difference between the coupling and the ring input is zero.

The closed array connections are such that the top array notes, T_{opi} are connected to the bottom array nodes B_{oti+2} with uniform phase offset. Phase difference will uniformly span from the top to the bottom of the array, 2 delays of buffers in phase. Figure 3 shows the cadence schematic of array of ring oscillator (8*3) 8 rows and 3 columns and output.

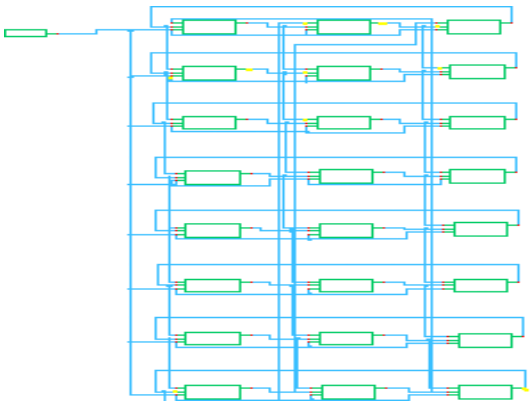

Fig.2. 8*3 Array of Ring VCO

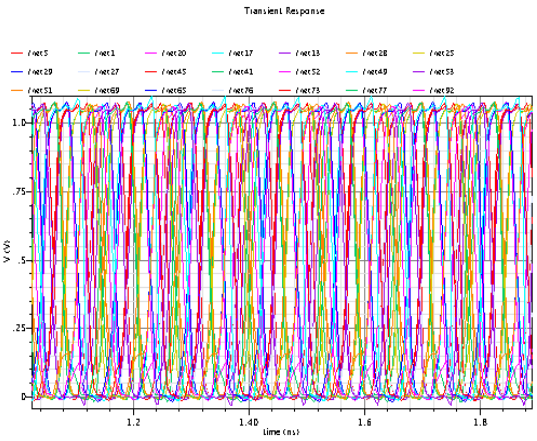

Fig.3. Output of Ring VCO

B. Phase Detector

In binary phase detectors the phase error detected is digitized. In this type of phase detector irrespective of the amount of leading phase the down signal increases significantly if the clock edge is leading the data edge [1]. But, the up signal increases significantly and down signal becomes low when the clock edge is lagging behind the data edge. If no data transition occurs, the PD remains in its previous state.

C. Incrementer/decrementer block

Incrementer/decrementer block is used to remove analog part charge pump. This incrementer/decrementer block is used as a counter. It consists of 8 bit ripple carry adders with D flip-flops. First carry input is termed INC input, which is incremented when UP signal is one. All DEC inputs are connected together, which are getting input DOWN signal as shown in Figure 4.

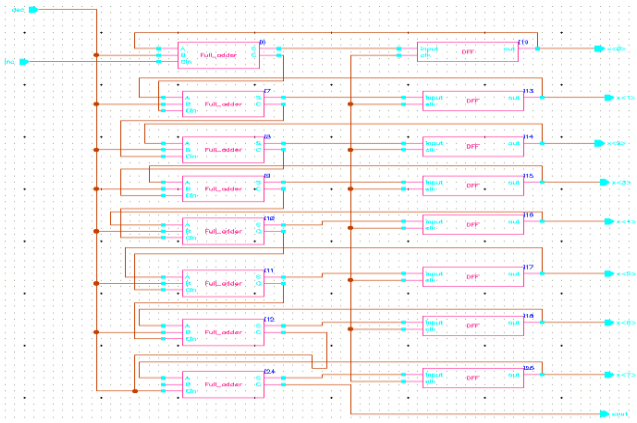

Fig.4. Incrementer/Decrementer block

D. Digital FIR filter

The design has a 13-tap filter with 8 bit outputs which then serves as an input to the current steering DAC. Each of the 13 taps is a shift register that stores the sampled 7 bit input values, multiplies the number with the corresponding coefficient and then shifts it right. The coefficients are multiplies by the input values and then added together. The digital FIR filter was implemented in VERILOG-A. Figure 5 below shows the code snippet of the FIR Filter.

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```
rxIn=rxIn +m * ((V(x[i]) > Vm) ? 1:0);
m=m*2;
end
$strobe("rxIn=%d", rxIn);
$strobe("ryOut=%d\n", ryOut);

if(enable==1) begin
//right shift to store past x values

for(i=12;i>0;i=i-1) begin
rx[i]=rx[i-1];
end
rx[0] = rxIn;

//Multiply
for(i=0;i<=12;i=i+1) begin
rxm[i]=(rx[i] * rc[i]);
end
//Add
ryOut=0;
for(i=0;i<=12;i=i+1) begin
ryOut=ryOut+rxm[i];
end
if(ryOut<0) begin
ryOut=0;
end

a=ryOut;
b=ryOut+ round;
ryOut=(ryOut + round) >> rcshift;
ryOutTmp=ryOut;
```

Fig.5. Code snippet of FIR Filter in Verilog-A

E. DAC-Digital to analog converter

The high level blocks in the DAC design includes register, row and column decoders which converts the binary inputs to the thermometer codes, array of current cells which is 16*16 where the output is controlled by the codes generated from the decoder that is the thermometer codes and an op-amp to convert current to output voltage.
We use current steering DAC as the reference current is divided in each and every branch and the branches are switched on and off depending upon the input codes. This current steering thermometer DAC results in high speed but has a very complex structure and also has some amount of power consumption and large area too.

1) Design specifications

There are four important blocks in this design [2]:

- Register
- Binary-to-thermometer decoder
- Current source array
- Differential op-amp

Figure 6 shows the blocks that was designed for the current steering DAC.

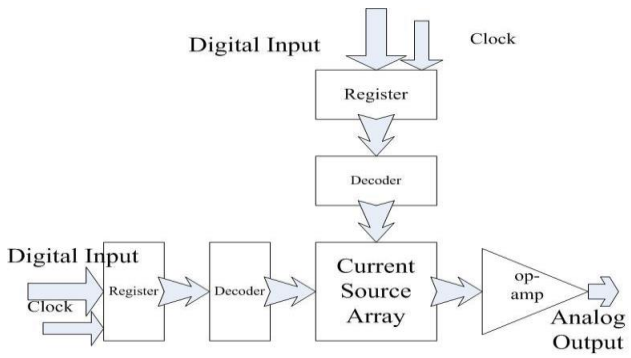

Fig.6.DAC Blocks

2) Binary to thermometer decoder

Binary codes are converter to thermometer codes by the decoder. It is called thermometer as it is similar to a mercury thermometer as after a particular temperature mercury is not present. Thermometer code needs a lot of bits, especially when the bit is large, only one bit changes every time to remove glitches or avoid them. Thermometer codes, switching from 000 0000 0111 1111 to 000 0000 1111 1111, only change one bit and avoid glitches.

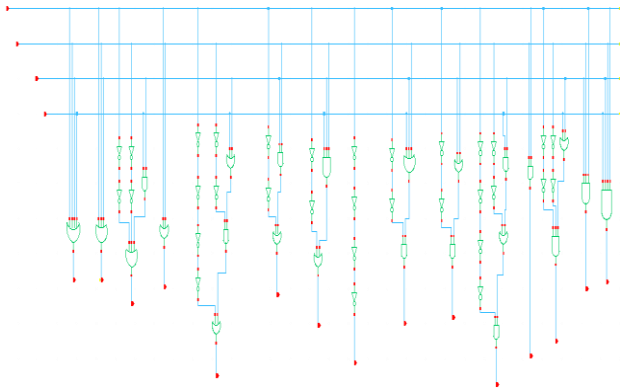

Fig.7. Binary to thermometer decoder

3) Current cell array

Figure 8 shows the overall schematic of the current cell array. The small rectangular on the top is the symbol of the bias and 16*16 array is consisted of identical current cells. All I_{out}, I_{out_neg} and clock signals are connected together. ROWN are connected to ROWN-1 above it and become row input signal; all COLN signals in some column are connected together to serve as column input signal [2]. Therefore, there are 15 row inputs and 15 column inputs.

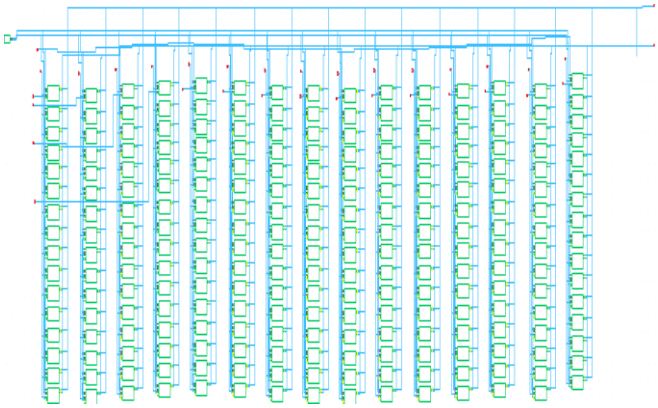

Fig.8. Schematic of current cell array (16*16)

4) Design of op-amp

Op-amp uses an NMOS diff-amp and a PMOS common-source amplifier. The compensating network contains a compensation capacitance and a zero-nulling resistor. This compensation network is used to make the op-amp stable. It is desirable that the open loop gain of the op-amp is much less than unity when the phase shift is 180. Gain was found to be 40.15dB and bandwidth of 20MHz with a current of 43.24μA.

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4) Overall design and simulation graphs of the DAC

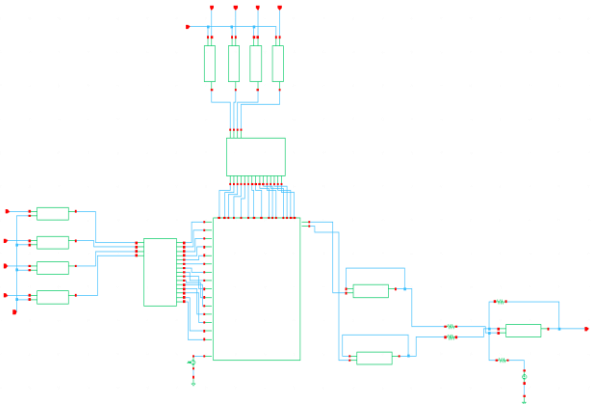

Fig.9. Overall DAC schematic

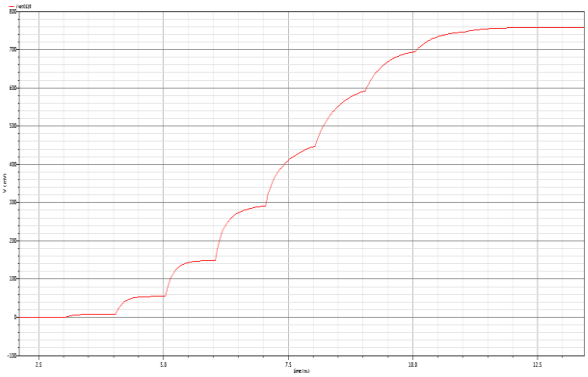

Fig.10. DAC simulation result

F. Simulation and results

All the blocks which were described above were connected together to test the PLL. Figure below shows the schematic diagram of the whole project. Input voltage for the VCO varies from 0 to 1 V. The incrementer/decrementer block uses the output of the phase detector and it works as a counter. Down signal is given to all the decrementer signals and up signal is given to INC signal of the first ripple carry adder. This counter output is given as an input to digital FIR and that is given as an input to the DAC. Current steering DAC is also one of the major and a huge block in the PLL. Since the output frequency is 6GHz, dividing by 256 logic is used before the signal goes as an input to the phase detector. Reference frequency is at 230 MHz.

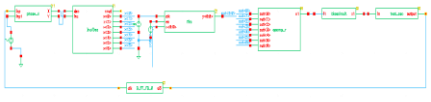

Fig.11. Overall Blocks of PLL

The below figures show the waveform of the PLL with all the blocks connected together and all the required parameters are measured. Table 1 shows the values of all the parameters measured. This PLL was operating at 6Gbps and it was considered a success for this project.

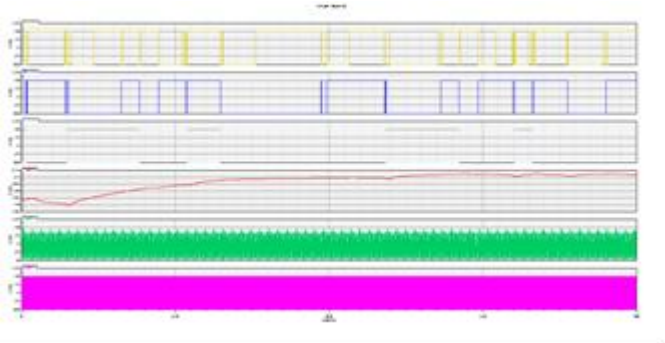

Fig.12. Overall waveforms of PLL

Table 1: Parameters measured

Parameters Measured	Values
Lock Time	6.2us
Reference Frequency	230MHz
Output Frequency	6GHz
Output Jitter	2ns
Technology	45nm

III. Conclusion

Low jitter PLL using DAC for SerDes transmitter was implemented successfully at 8Gbps speed for serial data links. This project was implemented in 45nm technology. As proposed this modified PLL has less area, high speed and moderate jitter. Each block in the design was verified individually and then it was verified as a system as a whole.

In this work the traditional parallel data links are replaced by serial links due to lot of advantages. Serial links are in greater demand in industries due to its fast operation. The low jitter PLL using DAC which is developed in this project can be implemented for a SerDes transmitter where the PLL's operation and speed becomes very crucial.

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[2] Yang Lin, "Design of an 8-bit CMOS Unit-Element Current-Steering Digital-to-Analog Converter", Thesis of University of Maine.
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