Optical, Material, and Electrical Characterizations of High-K Tantalum Pentoxide (Ta_2O_5) Dielectric Deposited on the Polycrystalline Silicon

Chyuan-Haur Kao, Hsiang Chen, Ching-Pang Chen

***Abstract*—To study annealing effects in Ta_2O_5 high-K dielectric devices, optical characterizations (Photoluminescence, PL and Cathodoluminescence, CL), electrical measurements and atomic force microscopy (AFM) were incorporated to examine high-k device performance. Compared with AFM images and electrical properties, luminescence observation was utilized to monitor the presence and the location of structural defects such as dangling bonds and traps. Since the defect states generated a continuous spectrum, relative defect concentrations could be detected by evaluating the intensity of defect-related luminescence. Optical characterizations were proven to be effective tools to evaluate the high-k material quality related to the device performance.**

***Key words*—high-K materials, Ta2O5, annealing, material analysis, optical characterization**

I. Introduction

Reducing the thickness of the SiO_2 storage capacitors has driven the development of high-density MOS dynamic random access memory (DRAM) to maintain the required charge storage level [1]. However, as the insulator thickness decreases, the SiO_2 insulator layer often is vulnerable to electron tunneling, causing the serious leakage current problem. Therefore, various high dielectric constant (k) materials have been recommended to replace SiO_2 to solve the leakage problem because the thicker film in high-k gate oxides can achieve the same equivalent oxide thickness (EOT). Over the past decade, various high dielectric constant (K) materials have been recommended to replace SiO_2 for solving the gate dielectric reliability issues. However, defect formation near the interface could degrade the dielectric quality and cloud the promise of achieving a high-k gate device. In this study, Ta_2O_5 was deposited by RF sputtering on polycrystalline silicon [2],[3] treated with post RTA annealing as a good method to mitigate defect formation [4],[5]. Defect luminescence observations [6] along with AFM analysis and electrical measurements was performed to evaluate the post RTA annealing effects on device performance.

Manuscript received February 10, 2015; revised April 24, 2015. This work was supported in part by the Ministry of Science and Technology the Taiwanese government under Grant 103-2221-206-011 .

Chyuan-Haur Kao is with the Department of Opto-Mechatronics and Materials, Chang Gung University 333, Tao-Yuan County, Taiwan, ROC. (e-mail: chkao@mail.cgu.edu.tw).

Hsiang Chen and Ching-Pang Chen are with the National Chi Nan University, Puli, Nantou County 54561, Taiwan, ROC (e-mail:hchen@ncnu.edu.tw Tel:886-49-2910960 Fax:886-49-2912238).

II. Experiment

To conduct the experiment, p-type Si wafers were thermally oxidized to have an oxidized layer of 550nm. Then, a polysilicon film of 300nm was deposited at 625^0C by a low pressure chemical vapor deposition (LPCVD) system. The film was implanted with phosphorous at a 5×10^{15} cm^{-2} dosage and 30KeV energy following activation for 30sec in an N_2 ambient at 950^0C to obtain a sheet resistance of 60~70 Ω/sq. Next, the native oxide was removed by dipping the film in a diluted hydrofluoric acid (HF) solution. A 35nm Ta_2O_5 gate dielectric was deposited by RF sputtering. After forming gate dielectrics, the samples were treated by rapid thermal annealing for 30sec in N_2 ambient at 600-900^0C to improve thin-film quality [7]. An aluminum gate of a thickness of 300nm was deposited on the samples. Self-aligned defining gates and gate dielectric patterns formed polyoxide capacitors using a two-step wet etching process. The 300nm Al gate and 35nm Ta_2O_5 gate dielectric layers were etched by an Al etching solution and wet etching, respectively. Aluminum/gate dielectric/n+ polysilicons were fabricated for this study. Al was deposited and patterned by photolithography to fabricate the high-k capacitor shown in Fig. 1

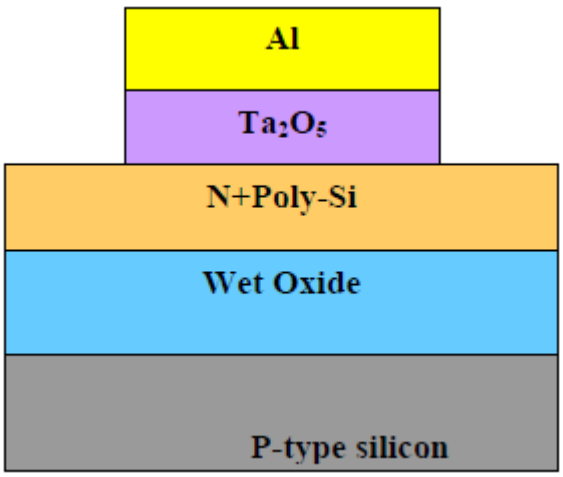

Fig. 1. The high-K capacitor structure

III. Results and Discussion

To investigate annealing effects, equivalent oxide thickness (EOT) from C-V measurements and charge to

ISBN: 978-988-19253-4-3
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

breakdown measurements (Weibull plots) under both polarities were conducted to evaluate the device reliability of the as-deposited and annealed samples [8]. Furthermore, AFM images were used to visualize the surface roughness of the high-k Ta_2O_5 dielectric. Finally, defect luminescence observations was utilized to gain insight into relative defect concentration. As for CL spectra, high kinetic energy electrons capable of deep penetration were used to excite the sample, allowing CL information to reveal changes in the deep oxide layer. In PL experiments, excitation photons accessed the shallow layers of the device to monitor the development of the high-K Ta_2O_5 layer and the high-k/polysilicon/oxide interface. Luminescence observation results, which were consistent with the electrical measurements and AFM analysis, recorded the locations and optimal annealing conditions of the defect improvements due to the annealing effects..

Table I EOT, surface roughness measured by AFM, and PL intensity of the oxide peak for the samples treated in different annealing conditions.

Annealing Temperature	Control (As-dep)	600 ^{0}C	800 ^{0}C	900 ^{0}C
EOT	97.1Å	80.7Å	73.7Å	92Å
Roughness of Ta_2O_5 Layer (RMS)	6.19 nm	5.232 nm	3.298 nm	5.578 nm
Oxide PL Peak Intensity (a. u.)	2199	2121	1225	1921

To analyze the performance of the dielectric as a gate device, electrical characterizations including EOT measurements, J-E characteristics under both polarity, charge-to-breakdown Weibull plots, and gate voltage shift versus stressed time were performed. A table of EOT extracted from high frequency C-V curves is shown in Table 1. EOT data extracted from C-V curves show measurements of 97.1Å, 88.7Å , 80.7 Å, 73.7 Å, and 92Å, respectively for the as-deposited and RTA annealed samples at 600 ,700, 800, and 900^{0}C. The capacitance values and relative dielectric constants (K) were also found about 86.4pF (14.04), 94.7pF (15.39), 104pF (16.9), 114pF (18.53), and 91.3pF (14.84) for the above samples, respectively. The sample annealed at 800^{0}C had the best electrical properties.

To investigate the electrical reliability improved by the annealing effect, as shown in Fig. 2(a) and (b), the high-k device with post-RTA annealing (RTA) at 800^{0}C had the largest charge-to-breakdown Q_{bd} and uniform Q_{bd} distribution under both positive (50μA/cm^2) and negative (-0.5mA/cm^2) constant current stress. The device reliability could be improved by mitigating dangling bonds and traps with RTA annealing. The charge-to-breakdown analysis corresponded with the EOT data.

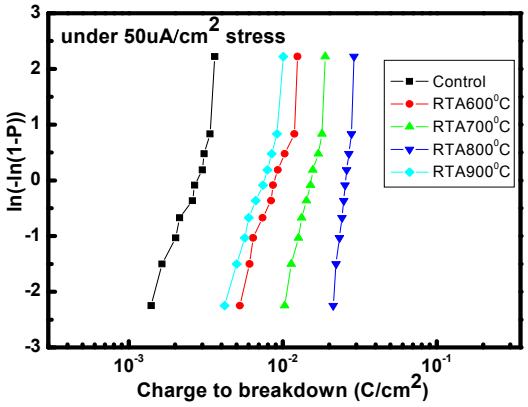

Fig2(a)

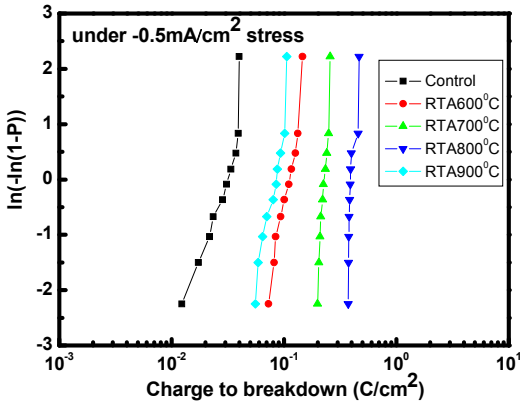

Fig 2(b)

Fig. 2. The Weibull charge to breakdown (Q_{bd}) plot of the device (a) under negative (b) positive constant current stress of the device in different annealing conditions.

Fig. 3 shows the AFM images of the Ta_2O_5 films for the as-deposited and RTA annealed samples at 600, 800, and 900^{0}C. AFM analysis was performed to examine the roughness of the devices in different annealing conditions. Compared with the as-deposited device and the device annealed in different conditions as shown in Table 1, the Ta_2O_5 layer of the device annealed at 800^{0}C had the smoothest dielectric surface, indicative of a well-crystallized structure. The root mean square (rms) values of the above four samples are 6.19nm, 5.232nm, 3.298nm, and 5.578nm, respectively. According to the AFM analysis, the post-RTA annealing treatment at 800^{0}C can passivate and reduce the trap states that existed in the Ta_2O_5 dielectric and the interface between the high-k Ta_2O_5 dielectric and polysilicon, improving quality.

To gain insight into defective structures, PL and CL measurements were utilized to zoom into defective structures such as dangling bonds and traps. Since the defect states generated a continuous spectrum, relative defect concentration could be detected by evaluating the intensity of defect-related luminescence. The PL and the CL results were measured from samples treated in different annealing conditions. As for the PL measurements shown in Fig. 4, the as-deposited sample has a strong defect-related luminescence

ISBN: 978-988-19253-4-3
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

spectrum. However, as the annealing temperature increased to 800^0C, the luminescence intensity drastically decreased by about 40%, signifying the dangling bonds and traps were greatly passivated by the annealing at 800^0 C. Since the PL measurements could detect changes in the Ta_2O_5 and the Ta_2O_5/poly/oxide interface, the defect structures were largely mitigated in these layers. Additionally, the trend was consistent with the charge-to-breakdown measurements and the AFM analysis. To tap into the deep oxide layer, CL was used to reveal differences in the samples at various annealing conditions. As shown in Fig. 4, the CL spectra do not have noticeable changes, signifying the annealing effect did not improve defect structures in the deep oxide layer. Furthermore, the peak between 450 nm and 500 nm was responsible for the oxide luminescence, since the luminescence peak taken from the oxide substrate fell in this range. The PL defect luminescence in the shallow high-k layer or the high-k/polysilicon/oxide interface decreased, but the CL defect luminescence in the deep oxide did not change, suggesting that the defect structures were improved in the high-k/polysilicon/oxide interface. As the annealing temperature further increased to 900^0 C, the PL luminescence intensity increased again and the defect structures in the interface returned. Moreover, the PL luminescence peak between 550 nm and 650 nm is likely responsible for the high-k Ta_2O_5 luminescence, since the peak could not be seen in the CL spectra. Similarly, the PL luminescence intensity decreased as the annealing temperature went up to 800^0 C and increased again at 900^0 C, signifying the defect structures in the Ta_2O_5 high-k layer were also mitigated at an annealing temperature of 800^0C. On the other hand, the PL luminescence change rate due to the annealing effect at 800^0 C with a wavelength range of 550 nm and 650 nm was 15%, and much less than the change rate between 450 nm and 550 nm, showing that annealing could improve the material quality in the high-k/polysilicon/oxdie interface more effectively than inside the high-k layer.

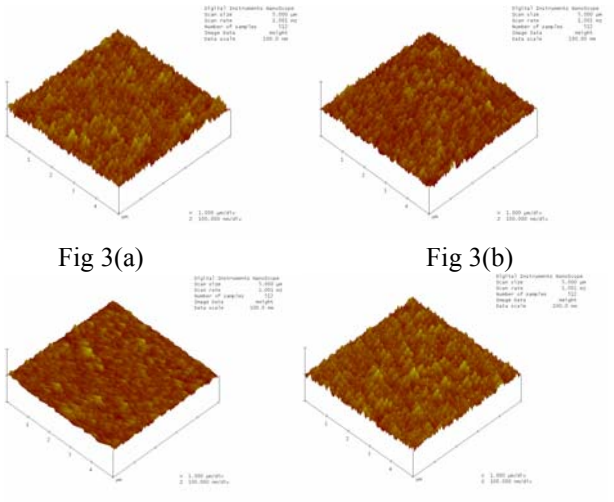

Fig 3(a) Fig 3(b)

Fig 3 (c) Fig 3 (d)

Fig. 3 AFM images of the high-k surface of (a) the as-deposited device, (b) the device annealed at 600^0 C ,(c) 800^0 C, and (d) 900^0 C.

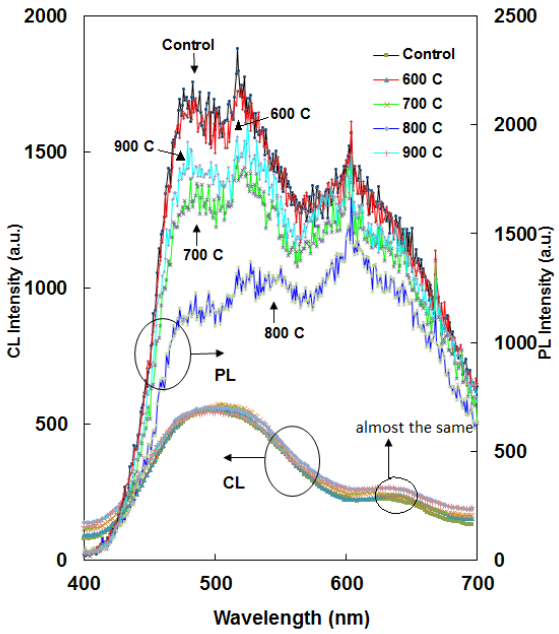

Fig 4. PL and CL spectra of the high-k devices in different annealing conditions

IV. Conclusion

This study used a combination of electrical measurements, AFM analysis, and optical characterization techniques to investigate the annealing effects on Ta_2O_5 high-k dielectric sputtered on polycrystalline silicon substrate. The optimal annealing temperature was found to be 800^0 C, and was consistent in the optical, material, and electrical measurements. Luminescence observations were proven to be effective tools to detect material quality related to device performance of the high-k Ta_2O_5.

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ISBN: 978-988-19253-4-3
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)