

# Analytical Investigation of Swing Factor for Nanoscale Double Gate MOSFET Including Gate-work-function Effect

T. Bentrchia, F. Djeflal and M. Meguellati

**Abstract**— Our aim in this work is to investigate through analytical modeling the impact of gradual variation of the gate work function on the device subthreshold performance expressed by the swing factor. Once the compact modeling is accomplished, a second stage for obtaining the best design of the device under critical channel length is presented using a genetic algorithm based approach. The obtained results confirm that the gate engineering based enhancements are promising solutions to deal with digital circuit drawbacks at nanoscale level.

**Index Terms**— linear graded gate, DG MOSFET, swing factor, genetic algorithm.

## I. INTRODUCTION

With the actual success in deploying electronic components in various applied fields, more efforts are accentuated on the scaling of their associated dimensions down to the nanoscale level. Such trend can be explained by the fact that a dramatic degradation of performance is resulted when reaching lengths below 100 nm as stated by the International Technology Roadmap for Semiconductors (ITRS), which is in turn reflected by the alteration of the main subthreshold parameters such as the drain induced barrier lowering or the swing factor [1]. The later criterion refers to the easiness of switching the device between ON-OFF states; it constitutes a paramount requirement for the design of efficient VLSI circuits and more particularly digital oriented applications [2].

In order to achieve this goal, compact and accurate modeling approaches that take into account different characteristics of the device are needed [3]. However, many drawbacks can be encountered when dealing with the obtained models due to the number of design parameters in addition to the nonlinearities existing within the models. For this reason, it would be worthy to consider the analytical modeling as a preliminary stage in an integrated framework that includes a second stage for optimization using some dedicated tools for instance metaheuristic methods. A framework having this structure allows the complete exploration and exploitation of the whole design space without neglecting imposed constraints [4].

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Our aim in this work is to investigate the influence of adopting a binary metal alloy ( $A_xB_{1-x}$ ) as a gate electrodes having continuous lateral concentration variation from the source side (material is A) to the drain side (material is B). The idea behind this work is that a linearly graded gate work function affects the vertical electric field in the channel leading to the restoration of the asymmetrical surface profile in nanoscale devices [5]. Based on the surface profile, we deduce a compact expression for the swing factor. In order to increase the device performance under critical channel length condition, we use a genetic algorithm based approach to get the best configuration within imposed intervals of the design parameters.

The remaining of this work is arranged as follows. The compact modeling steps of the surface potential and the swing factor are highlighted in Section 2. Section 3 presents the main obtained simulation results in addition to the optimization performance compared to random designs. Some concluding remarks are provided in Section 4.

## II. ANALYTICAL MODELING

Figure 1 depicts a typical cross sectional view of the DG MOSFET device considered in this study, where both gates are symmetrical and assumed to be made of a binary metal alloy with linear variation of constituents. In fact, the continuous variation of the gate work function affects the vertical electric field which restores the asymmetrical surface profile in nanoscale devices.

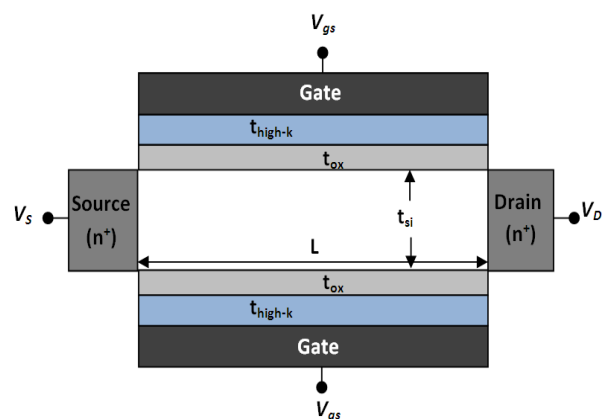


Figure 1. Cross sectional view of the linear graded DG MOSFET considered in this work.

Therefore, the effective work function of both gates in this case can be provided using a weighted sum expression as follows

$$\phi_{meff}(x) = \omega(x)\phi_b + (1 - \omega(x))\phi_a$$

where  $\phi_a$  and  $\phi_b$  are the elementary work functions of materials a and b respectively. The weighting factor  $\omega(x)$  is expressed by the horizontal component x normalized with respect to the channel length L.

#### A. Surface potential modeling

For the modeling purpose, quantum mechanical effects due to the field and the spatial confinements are neglected since free electrons in an undoped device are quite evenly spread in the whole silicon layer resulting in a small vertical electric field. Hence, in subthreshold regime, it is possible to describe the channel potential based on the well-known 2-D Poisson's equation

$$\frac{\partial^2 \psi(x, y)}{\partial x^2} + \frac{\partial^2 \psi(x, y)}{\partial y^2} = \frac{qN_A}{\epsilon_{Si}} \quad (2)$$

where  $\psi(x, y)$  denotes the 2-D potential profile,  $N_A$  the uniform channel doping and  $\epsilon_{Si}$  the silicon permittivity.

According to Young's parabolic approximation [6], a general form of the channel potential can be written as

$$\psi(x, y) = a(x) + b(x)y + c(x)y^2 \quad (3)$$

where a, b and c are unknown functions of x to be determined.

In order to solve Poisson equation, the following set of boundary conditions should be satisfied [7]

$$\begin{cases} \epsilon_{ox} \frac{V_{F,eff} - \psi(x, 0)}{t_{oxeff}} = \epsilon_{Si} \frac{\partial \psi(x, y)}{\partial y} \Big|_{y=0} \\ \epsilon_{ox} \frac{V_{B,eff} - \psi(x, t_{Si})}{t_{oxeff}} = \epsilon_{Si} \frac{\partial \psi(x, y)}{\partial y} \Big|_{y=t_{Si}} \end{cases} \quad (4)$$

with the effective oxide thickness is expressed by the formula

$$t_{oxeff} = t_1 + (\epsilon_1 / \epsilon_2) t_2 \quad (5)$$

By applying the symmetry condition of the potential profile with respect to the middle of the channel ( $y = \frac{t_{Si}}{2}$ ), an explicit formula is deduced as

$$\psi(x, y) = \psi_s(x) + \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{\psi_s(x) - V_g^*}{t_{oxeff}} y - \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{\psi_s(x) - V_g^*}{t_{oxeff} t_{Si}} y^2 \quad (6)$$

where  $\psi_s(x)$  represents the surface potential at Si/SiO2 interfaces given by  $y = 0$  and  $y = t_{Si}$ .

We get an ordinary differential equation that deals only with the surface potential  $\psi_s(x)$  by substituting (6) in (2)

$$\frac{d^2 \psi_s(x)}{dx^2} - \frac{1}{\lambda^2} \psi_s(x) = D(x) \quad (7)$$

with  $\lambda$  and  $D(x)$  are defined by  $\sqrt{\frac{\epsilon_{Si} t_{oxeff} t_{Si}}{2\epsilon_{ox}}}$  and

$$\frac{qN_A}{\epsilon_{Si}} - \frac{2\epsilon_{ox} \left( V_{gs} - \phi_a + \frac{(\phi_a - \phi_b)x}{L} \right)}{\epsilon_{Si} t_{oxeff} t_{Si}} \text{ respectively.}$$

The general solution of such equation has the form

$$\psi_s(x) = -\lambda^2 D(x) + A_1 e^{\left(\frac{x}{\lambda}\right)} + A_2 e^{-\left(\frac{x}{\lambda}\right)} \quad (8)$$

Based on the values of the potential profile at boundaries ( $\psi(0, y) = V_{bi}$  and  $\psi(L, y) = V_{bi} + V_{ds}$ ), the coefficients A1 and A2 are obtained as

$$\begin{cases} A_1 = \frac{V_{bi} e^{\left(\frac{L}{\lambda}\right)} - D_1 \lambda^2 - V_{bi} + V_{ds} e^{\left(\frac{L}{\lambda}\right)} + D_2 \lambda^2 e^{\left(\frac{L}{\lambda}\right)}}{e^{\left(\frac{L}{\lambda}\right)} - 1} \\ A_2 = \frac{\left( V_{bi} + V_{ds} + D_2 \lambda^2 - V_{bi} e^{\left(\frac{L}{\lambda}\right)} - D_1 \lambda^2 e^{\left(\frac{L}{\lambda}\right)} \right)}{e^{-\left(\frac{L}{\lambda}\right)} - 1} \end{cases} \quad (9)$$

#### B. Swing factor modeling

The subthreshold swing is defined as the variation in the gate voltage required changing the subthreshold drain current by one decade. It should be as small as possible in order to have good switching characteristics for the device. Based on the assumption that the subthreshold current is proportional to the free carrier density at the virtual cathode, the subthreshold swing model in its general form is given by [8]

$$S = \frac{\partial V_{gs}}{\partial \log I_{ds}} = V_t \ln(10) \times \left[ \frac{\int_0^{t_{Si}/2} e^{V_{min}/V_t} \left( \frac{\partial \psi_{min}}{\partial V_{gs}} \right) dy}{\int_0^{t_{Si}/2} e^{V_{min}/V_t} dy} \right]^{-1} \quad (10)$$

An approximated solution for this integral is proved to have the following form

$$S = \frac{kT}{q} \ln(10) \times \left[ \frac{\partial \psi_s(x_{min})}{\partial V_{gs}} \right]^{-1} \quad (11)$$

where the position of minimum electrostatic potential is given by

$$x_{min} = \lambda \log \left( \frac{\left( \lambda \phi_a - \lambda \phi_b + \sqrt{4A_1 A_2 L^2 + \lambda^2 \phi_a^2 - 2\lambda^2 \phi_a \phi_b + \lambda^2 \phi_b^2} \right)}{2A_1 L} \right) \quad (12)$$

### III. RESULTS AND DISCUSSION

In this section, we present a performance comparison of the linear graded and conventional MOSFETs where the surface potential and the swing factor are the main criteria in focus of the discussion. The parameter values used for simulation are listed in Table I.

TABLE I. SIMULATION PARAMETER VALUES OF THE LINEAR GRADED DG MOSFET STRUCTURE

Parameter	Value	
	Notation	Value
Oxide layer thickness	$t_1$	1 nm
High-k layer thickness	$t_2$	1.5 nm
Drain/source doping	$N_{DS}$	$1 \times 10^{20} \text{ cm}^{-3}$
Intrinsic doping	$n_i$	$1.45 \times 10^{10} \text{ cm}^{-3}$
Channel doping	$N_A$	$1 \times 10^{15} \text{ cm}^{-3}$
Channel thickness	$t_{Si}$	10 nm
Source side work function	$\phi_a$	5.65 eV
Drain side work function	$\phi_b$	4.28 eV
Gate voltage	$V_{gs}$	0.5 V
Drain voltage	$V_{ds}$	0.5 V

Figure 2 highlights the variation of the surface potential as a function of the position along the channel. It can be observed that with a linear graded gate, the point of minimum surface potential is shifted towards the source side. The low work function near the drain side allows reducing the drain voltage variation caused by the drain induced barrier lowering effect.

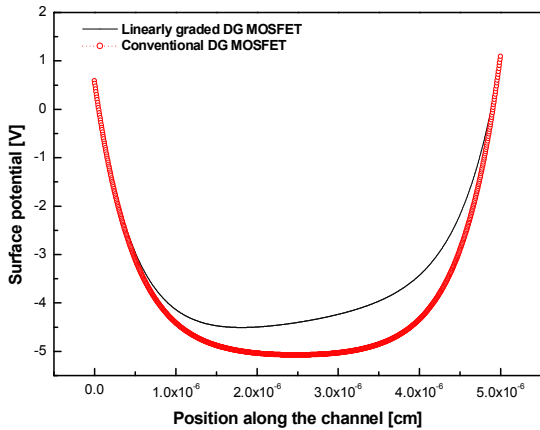


Figure 2. Variation of the surface potential as a function of the position along the channel ( $L=50 \text{ nm}$ ).

The swing factor relative improvement gained by introducing the linear graded gate concept is illustrated in Figure 3. It is clear that the swing factor is significantly enhanced for the channel length at nanoscale level where an amelioration of about 3% is obtained. This means that the suppression of short channel effects can be efficiently conducted with the use of gate engineering strategies.

A more robust design procedure of the linear graded DG MOSFET under critical condition (the channel length takes its lowest value 10 nm), it is possible to use a genetic algorithm based optimization approach in order to obtain better swing factor for digital circuit applications.

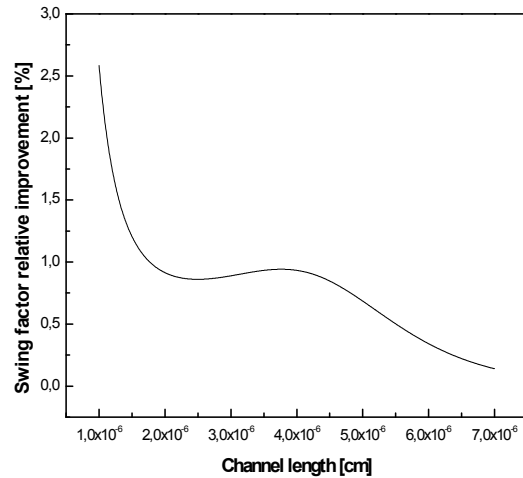


Figure 3. Variation of the swing factor relative improvement as a function of the channel length ( $L$  is varied from 10 nm to 70 nm).

The genetic algorithm has been proposed initially by Holland. In a similar way to natural operations, the algorithm adopts genetic operators such as selection, crossover and mutation in order to create descendent individuals with better properties [9-11]. In our optimization procedure, the tournament selection is employed, where a set of individuals is selected at random and the best individual is picked out of the set to be a parent. Scattered crossover creates a random binary vector. The genes where the vector is unity from the first parent and where the vector is zero from the second parent are selected and combined to form the child.

The optimization procedure is performed for 200 population size and a maximum number of generations equals to 200 because the convergence of the fitness function is obtained. The crossover rate is fixed to 0.8. Therefore, the minimization of the swing factor is considered as the objective function in this study. The design parameters forming the input vector in addition to their range of variation during the optimization are listed in the table below (Table II).

TABLE II. RANGE VALUES OF THE DESIGN PARAMETERS USED DURING THE SIMULATION

Parameters	Range values	
	Lower bound	Upper bound
$t_1$	0.5 nm	3 nm
$t_2$	1 nm	3 nm
$t_{Si}$	3 nm	8 nm
$\phi_a$	3 eV	6 eV
$\phi_b$	3 eV	6 eV
$V_{gs}$	0 V	1 V
$V_{ds}$	0 V	1 V

The design parameters are varied according to genetic operators and the best solution in the current population in

term of the swing factor is registered. The variation of the best swing factor as a function of the number of generations is shown in Figure 4, where the stability of the minimum objective function is reached after about 100 iterations.

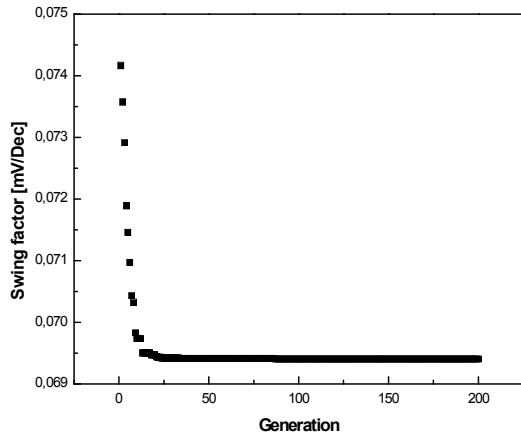


Figure 4. Evolution of the swing factor as a function of the number of generations.

The final optimized linear graded DG MOSFET design and its associated objective function are summarized in Table III, where the relative improvement of the swing factor after optimization is estimated to 57% compared to the conventional DG MOSFET. Moreover, it should be taken into account that the standard CMOS design tools assume values for the swing factor less than 100 mV/dec in order to be used for the design purposes of low power digital applications [12-13].

TABLE III. OBTAINED RESULTS FOR THE OPTIMIZED LINEAR GRADED DG MOSFET STRUCTURE

	<i>Parameter</i>	<i>Optimized value</i>
<i>Design parameters</i>	$t_1$	0.5 nm
	$t_2$	1 nm
	$t_{Si}$	3 nm
	$\phi_a$	6 eV
	$\phi_b$	3 eV
	$V_{gs}$	1 V
	$V_{ds}$	0 V
<i>Objective function</i>	S	68.8

#### IV. CONCLUSION

In this work, we presented an analytical analysis of the linear graded DG MOSFET structure, where the swing factor is compared with respect to the conventional case. As the work function of the gate varies smoothly from high value near the source to low value near the drain, it offers better control over the channel region. The application of genetic algorithm has allowed the optimal design of the investigated structure under critical 10 nm channel length. The obtained

subthreshold results have shown a significant improvement in switching characteristics of the device which makes it more appropriate to be included within digital circuit applications.

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