DIBL and Subthreshold Swing Effect on Carbon Nanotube Field Effect Transistor

Soheli Farhana, AHM Zahirul Alam, and Sheroz Khan, *Member, IAENG*

***Abstract*— Silicon based devices are getting problem with the limitation of channel length for fabrication of the miniature size. Short channel effects are creating such problem of the silicon devices. Thus CNT is a smart choice for replacement with the silicon. A brief analysis of the effect of short channel carbon nanotube field effect transistor (CNTFET) is elucidated in this paper. The analysis of the CNTFET model shows the Drain Induced Barrier lowering (DIBL) and sub-threshold Swing (S) of CNTFET with the channel of 14nm. The analysis of SS and DIBL shows the best electronics performance of CNT. High-k transistor can be fit for this material such as Hfo2 performs low subthreshold swing because of get large gate capacitance. This analysis is necessary for the design of a lower scaling channel of CNTFET.**

***Index Terms*—Carbon nanotube, DIBL, subthreshold swing, transistor**

I. Introduction

THE drain-induced barrier lowering (DIBL) and subthreshold swing (SS) are required parameter for scaling and low power consumption transistor modeling. In building the CNTFET circuits, subthreshold leakage current (Isub), I_{ON}, I_{OFF} currents are also important parameters for transistor modeling in the semiconductor industry. Basically low power consumption of FET will be set by the lower value of sub threshold swing. An imperative task in a FET is to turn a transistor "ON" with the least amount voltage swing required. The gate voltage known as subthreshold swing is required to change the drain current.

For nano scale modeling, the major difficulties of the semiconductor industry are the drain-induced barrier lowering (DIBL) is considered due to the short channel effect and to the bulk effect the subthreshold swing [1]. The interband tunneling current for FET is developed in recent years [2]–[7]. The subthreshold swings are characterized by few researchers for the development of field effect transistor. A double gated CNTFET was developed with the subthreshold swing of 40mV/dec [5]. Doping is found very low in CNTFET due to the small channel length, thus drain induced barrier lowering (DIBL) can be realized in between drain and source for their electrostatic interaction. On the other hand, the effect of narrow channel lowering of the source-junction is DIBL.

In this paper, a brief analysis is elaborated for the development of a CNTFET. The proposed CNTFET model is also presented in the next part of this paper.

II. CNTFET Model

The device geometry involves the insertion of Schrödinger's equation to analyze the density of states and effective masses caused by the effects in valance and conduction bands. The (25,0) intrinsic zigzag CNT is implanted on the gate insulator. The thickness of the insulator is 2 nm. A 14nm long CNT with the diameter of 1.95 nm, and band gap E_g of 0.44 eV is embedded with the FET. An illustration for CNTFET 3D layout model is shown in Fig. 1.

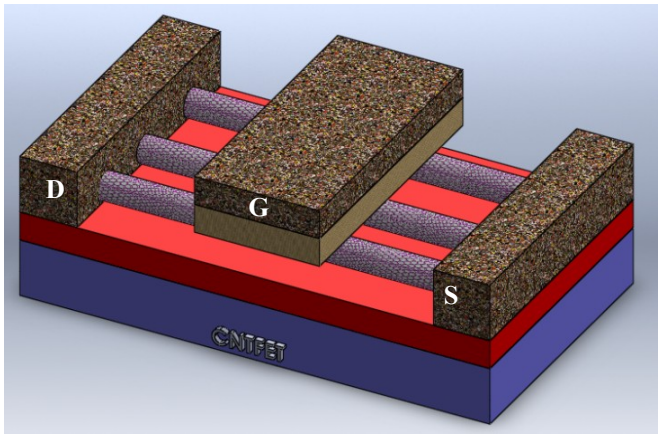

Fig. 1. Cross sectional view of a CNTFET

III. Modeling Methodology

A. Methodology for Subthreshold Swing (SS)

Subthreshold swing (SS) is the main performance factor CNTFET. Subthreshold swing (SS) can be defined by,

$$SS = \left| \frac{d \log_{10} G}{dV_g} \right|^{-1} \quad (1)$$

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The channel conductance is responsible for the variation of the gate conductance.

The smallest subthreshold swing is achieved when a traditional transistor change gate voltage, that causes the following effect,

$$\frac{dE_{c,v}}{d(eV_g)} = -1 \tag{2}$$

In the idle mode of transmission probability, the calculation of conductance is stated in equation (3). In this calculation, the energies are considered less than the lower value of valance band. Thus the conductance become,

$$G = 2G_0 \exp\left(\frac{E_v - E_F}{kT}\right) \tag{3}$$

And the subthreshold swing is

$$SS = \left|\frac{d\log_{10} G}{dV_q}\right|^{-1} = \left(\frac{d\log_{10} G}{d(E_v/e)}\right)^{-1} = \frac{kT}{e}\ln 10 \tag{4}$$

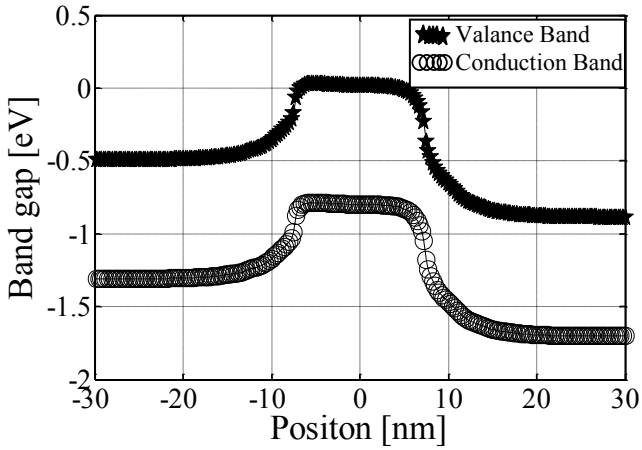

Fig. 2. Diagram of the subthreshold swing of a field-effect transistor

B. Methodology for Drain-induced Barrier Lowering

Different lengths of the various transistors in size show the device performances reduction in the circuit operation. Serious degradation can be generated by short channel effects in transistors can lead to of the device characteristics as the different length scales. Silicon or other bulk semiconductor materials are used to fabricate traditional transistors, thus short channel effect is realized in these transistors. On the contrary, carbon nanotube transistors short channel effects are not extensively studied in the previous researches. The resistive contacts of short channel effects in CNTFETs are briefly analyzed here. In Fig. 3, a sketch is considered for a semiconducting carbon nanotube that attached in between a source and drain electrode. Carbon nanotube is present in the channel region. SiO_2 wrapped the CNT and a gate covers the SiO_2. In the channel dielectric region, two metals are embedded with the two terminals of the carbon nanotube as shown in Fig. 3. A rectangular gate covers the dielectric. The central dielectric and the contacts are separated in the above structure in Fig. 3. The analysis of this model is used zigzag carbon nanotube with the chirality of (25,0), where an optimum band gap was found [8]. Three dimensions Poisson's equation is used to find the value of CNT potential. Furthermore, the boundary conditions and the charge on the nanotube are also analyzed at the drain and source contacts. Nonequilibrium Green's function is used to calculate current and charge in ballistic systems.

Threshold voltage can be shifted by the increment of the source drain voltage which caused the symptom of the drain-induced barrier lowering (DIBL). The scaling of the DIBL can be achieved if the factor of the channel length is scaled as follows,

$$\alpha = \sqrt{R_T + l} \tag{5}$$

Where, R_T is the CNT radius and l is the length of the CNT.

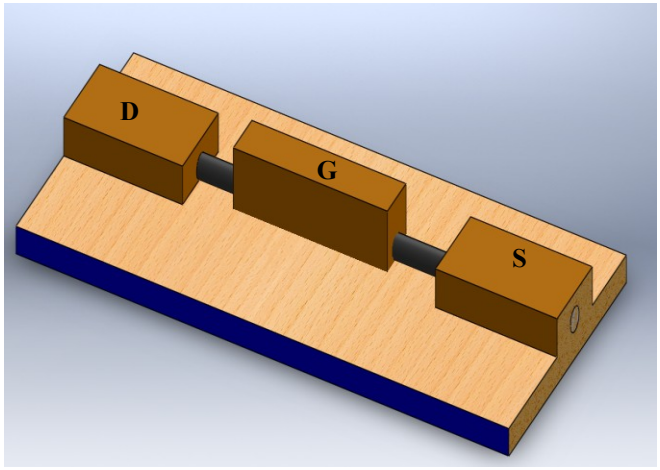

Fig. 3. Device simulations nanotube transistor sketch

C. Analysis

The research considered a (25, 0) CNT which results in a band gap of ~ 0.44 eV and a diameter of ~ 1.95 nm. A coaxial gate was placed around the intrinsic part of the nanotube and separated by an oxide with thickness of 1.5 nm. At this inspect, the temperature was kept at 300 K. In addition, source Fermi level was – 0.32, dielectric constant was 3.9. Fig. 6 represents the I-V characteristics of CNTFET with respect to Vgs. To analyze the performance after 0.85, αG was varied from 0.88 to 1.5 maintaining interval of 0.02. According to the Fig. 6, drain current still maintain the increasing trends while reaching to 1.5. In this experiment, since the capacitance and the gate potential are incorporated with inverse relationship, the total capacitance decrease. Fig. 4 shows the flowchart of the steps for subthreshold swing and DIBL that occurred in the proposed model.

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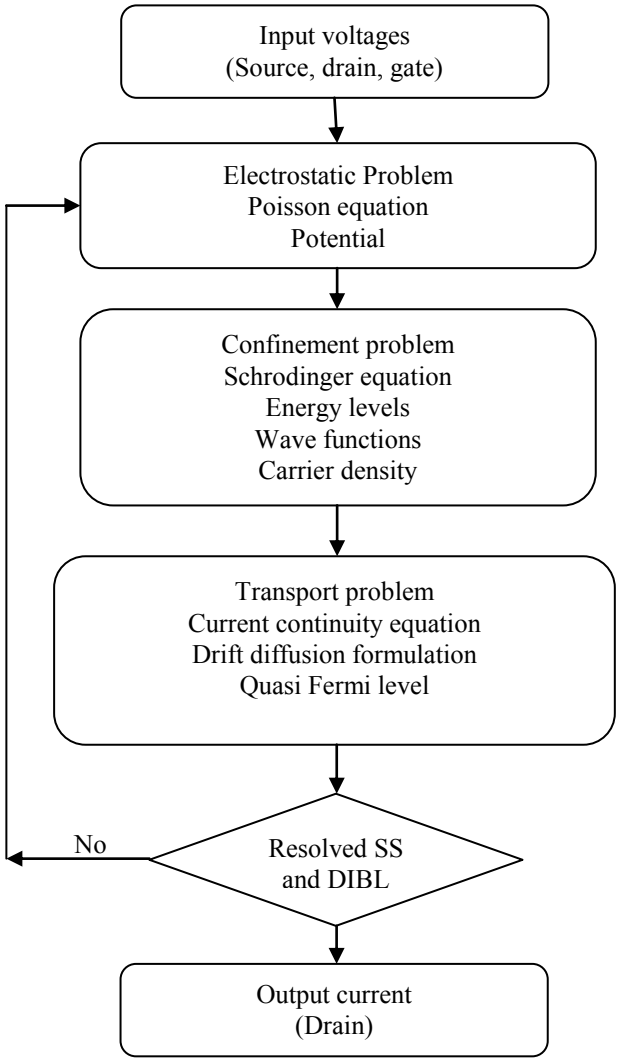

Fig. 4. Flowchart for the working principals of SS and DIBL for a CNTFET

The flow of transistor shrinking is depends on the most important parameter subthreshold swing (SS). Furthermore, the optimum value of the current ON/OFF ratio is also be generated from subthreshold swing (SS). All the minimum values are required for small size transistor. The size transistor also pays attention on the low energy and low threshold voltage for its operation. The lowest theoretical limit for SS is 60mV/decade at room temperature [9]. Initially, subthreshold swing decreases with high gate control coefficient and its bottom out in between 1.2 to 1.3. Afterwards, swing starts increasing and comes close to its theoretical limit which is shown in Fig. 7. This observation indicates that, higher gate control coefficient is desired in order to have fast CNFET response.

The transistor channel can be driven from pinch-off region to conduction by the effect of drain induced barrier lowering (DIBL). The transistor leakage current is also caused from the effect of DIBL. The threshold voltage also can be shifted by DIBL which damage the gate voltage effectiveness to drive the transistor. In addition, the transistor device performances should be reduced abruptly from the effect of DIBL. Only accurate circuit design should get rid from these DIBL effects of the transistor. During the application of high voltage of the transistor, DIBL effect can be realized once the channel carrier's barrier height reaches at the edge of the source. Fig. 8 shows that, DIBL decrease with increasing gate control coefficient. In fact, it is an advantage of CNTFET while nanometer regime.

IV. Results and Discussions

The proposed model as shown in Fig. 1 has been simulated to verify the current -voltage characteristics. An N-CNTFET dc characteristic is analyzed and simulated in PSPICE. Modeling of CNTFET with the I-V characteristics analysis is obtained for a channel length 14nm and width 26nm. Fig. 5 shows I_{DS} versus drain voltage (V_{DS}) of a CNTFET with the length of 14nm. For the 14nm gate length, we found a drive current I_D=690μA at V_{ds}=V_{gs}=0.4V, giving an I_{ON}/I_{OFF}= 4*103. The transconductance in the saturation region is gm=1.8 mS, which is found at Vds=0.4V for V_{gs}=V_{DD}=0.4V will minimize the ON/OFF current ratio. The relation of drain current and gait voltage is shown in Fig. 6.

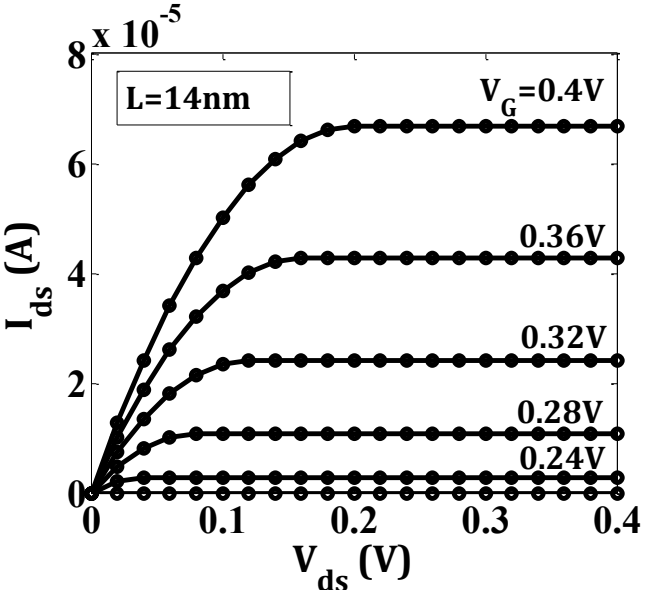

Fig. 5. Drain current versus drain voltage for (25,0) CNTFET

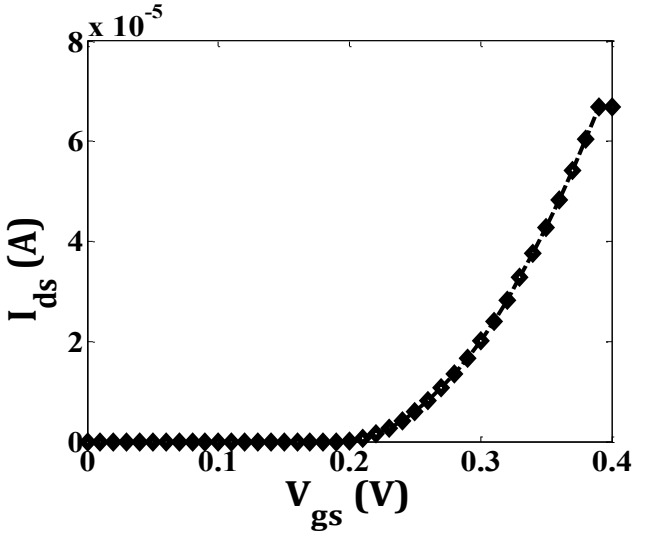

Fig. 6. Drain current versus gate voltage for (25,0) CNTFET

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Fig. 7 shows SS versus L_G comparing with different channel length of the (25,0) zigzag CNTFET. The tiny body of planar at L_G=14nm the device has smaller drain induced barrier lowering (DIBL) and SS.

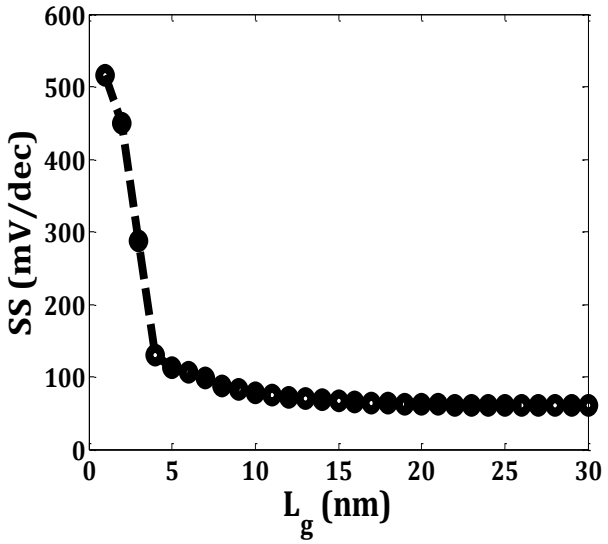

Fig. 7. SS versus L_G comparing with different channel lengths

Fig. 8 compares DIBL versus L_G for different channel length of CNTFET. The top gate CNTFET shows the important improvement of DIBL.

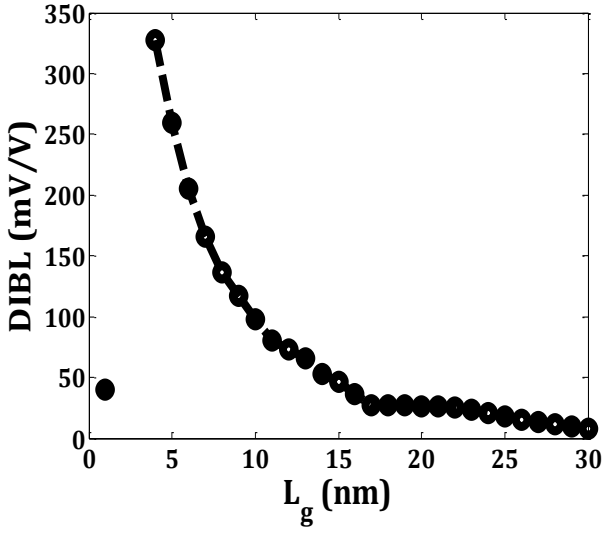

Fig. 8. DIBL versus LG comparing with different channel lengths

In this experiment, increments of the source drain voltage from 0.1 V to 0.2 V which shift the threshold voltage of 190 mV that produces the DIBL. The (25, 0) CNTFET is considered to simulate for the device characterization. The subthreshold swing 68.14 mV/decade is achieved from this analysis. Threshold voltage is shifting during the increment of V_{gs} from 0.1 to 0.4 voltages. This is a sign of the DIBL. The channel length 14 nm is extensively develops both the DIBL and subthreshold swing, that is 53.19mV/decade and 68mV/decade, correspondingly.

V. Conclusions

A solid model of 3D CNTFET top-gate with channel length of 14nm has been simulated. The device geometry requires inclusion of Schrödinger's equation to calculate electron/hole effective masses and density of states due to the perturbations in conduction and valance bands. By achieving the better values of DIBL and SS of the device, CNTFET shows an excellent behavior of as the electrostatics material. This device is suited for high-k FET, such as $Hf0_2$ low subthreshold swing because of get large gate capacitance. The proposed model shows the value of SS and DIBL to design top gate CNTFET device. This structure can be able to update the scaling of the semiconductor device. In low power consumption, future CNTFET device will be designed by using this proposed model.

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