

Asynchronous Sequential Symbol Synchronizers based on Pulse Comparison by Positive Transitions at Quarter Bit Rate

Antonio D. Reis, Jose F. Rocha, Atilio S. Gameiro and Jose P. Carvalho

Abstract— This work studies the asynchronous sequential symbol synchronizers based on pulse comparison by positive transitions at quarter bit rate. Their performance will be compared with the standard reference asynchronous symbol synchronizers based on pulse comparison by both transitions at bit rate. For the reference and proposed variants, we consider two versions which are the manual (m) and the automatic (a). In systems with no linear distortion, the synchronizers of positive transitions can be preferable to the both transitions. The objective is to study the four synchronizers and evaluate their output jitter UIRMS (Unit Interval Root Mean Square) versus input SNR (Signal Noise Ratio).

Index Terms—Synchronism, Digital Communications

I. INTRODUCTION

This work studies the asynchronous sequential symbol synchronizer based on pulse comparison operating by positive transitions at quarter bit rate (ap/4). Their jitter is compared with the reference asynchronous synchronizers operating by both transitions at bit rate (ab) [1, 2].

For both, reference and proposed variant, we consider the versions manual (m) and automatic (a) [3, 4, 5, 6, 7].

The difference between the reference and proposed synchronizer is in the symbol phase comparator since the other blocks are similar. The phase comparator compares the input variable pulse duration P_v with the intern reference fixed pulse duration P_f and the error pulse P_e synchronizes the VCO (Voltage Controlled Oscillator) [8, 9, 10].

The synchronizer regenerates the data, recovering a clock (VCO) that samples and retimes the data [11, 12, 13, 14].

Fig.1 shows the blocks of the general symbol synchronizer.

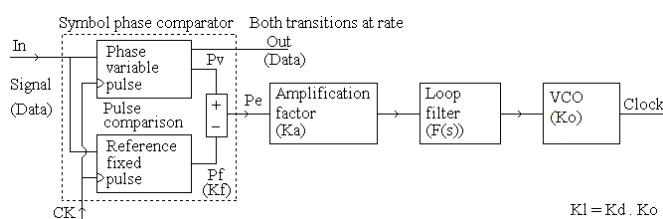


Fig.1 Synchronizer based on pulse comparison

K_f is the phase comparator gain, $F(s)$ is the loop filter, K_o is the VCO gain and K_a is the loop amplification factor that controls the root locus and then the loop characteristics.

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In priori and actual-art state was developed various synchronizers, now is necessary to know their performance.

The motivation of this work is to create new synchronizers and to evaluate their performance with noise. This contribution increases the knowledge about synchronizers.

Following, we present the reference variant, asynchronous sequential symbol synchronizers based on pulse comparison by both transitions at bit rate, with versions manual (ab-m) and automatic (ab-a). Next, we present the proposed variant, asynchronous sequential symbol synchronizer based on pulse comparison by positive transitions at quarter bit rate, with versions manual (ap-m/4) and automatic (ap-a/4).

After, we present the design and tests. Then, we present the results. Finally, we present the conclusions.

II. REFERENCE BY BOTH AT BIT RATE

The standard reference, asynchronous sequential symbol synchronizers based on pulse comparison operating by both transitions at bit rate has two versions which are the manual (ab-m) and the automatic (ab-a) [1, 2]. The versions difference is in the phase comparator, the variable pulse P_v is common but the fixed P_f is different. Their jitter- SNR curves are the general quality reference.

A. Reference by both at rate manual (ab-m)

The block P_v , shown below, produces a variable pulse P_v between the input bits and VCO. The manual adjustment delay with Exor produces a manual fixed pulse P_f (Fig.2).

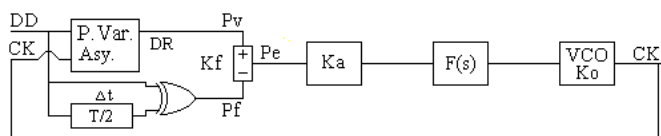


Fig.2 Asynchronous by both at rate and manual (ab-m)

The comparison between the pulses P_v and P_f provides the error pulse P_e that forces the VCO to synchronize the input. The block P_v is an asynchronous circuit (Fig.3).

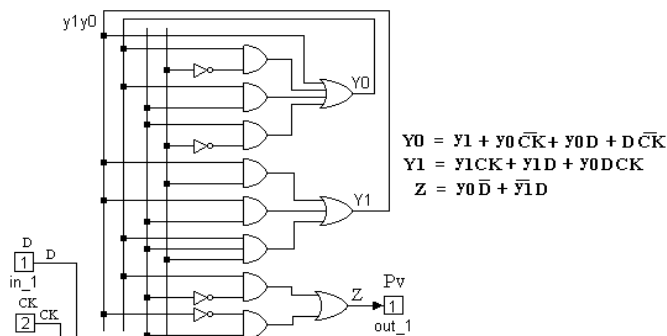


Fig.3 Intern aspect of the block P_v

Fig.4 shows the waveforms of the reference manual (equal to the corresponding synchronous version) [3].

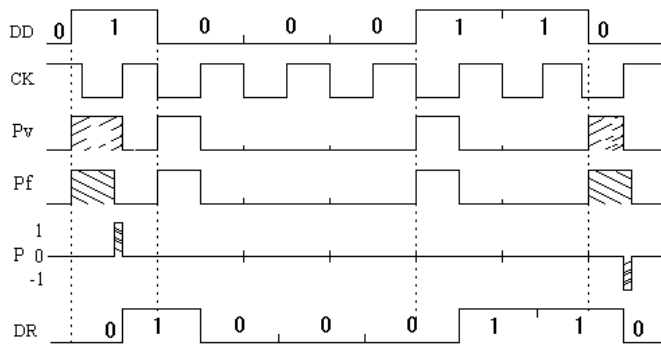


Fig.4 Waveforms of the asynchronous by both at rate manual

The error pulse P_e diminishes during the synchronization time and disappear at the equilibrium point.

B. Reference by both at rate automatic (ab-a)

The block P_v , common with anterior, produces the variable pulse P_v between input and VCO. The block P_f , shown below, produces the comparison fixed pulse P_f (Fig.5).

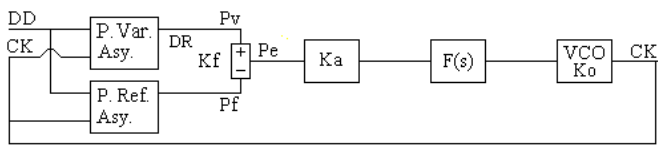


Fig.5 Asynchronous by both at rate and automatic (ab-a)

The comparison between the pulses P_v and P_f provides the error pulse P_e that forces the VCO to follow the input. The block P_f is an asynchronous circuit (Fig.6).

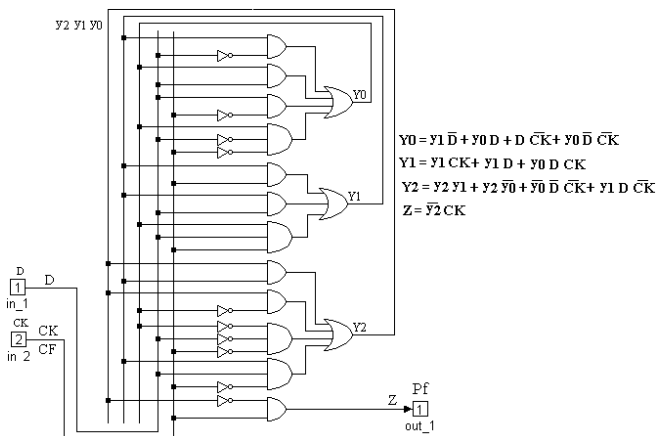


Fig.6 Intern aspect of the block P_f

Fig.7 shows the waveforms of the reference automatic (equal to the corresponding synchronous version) [3].

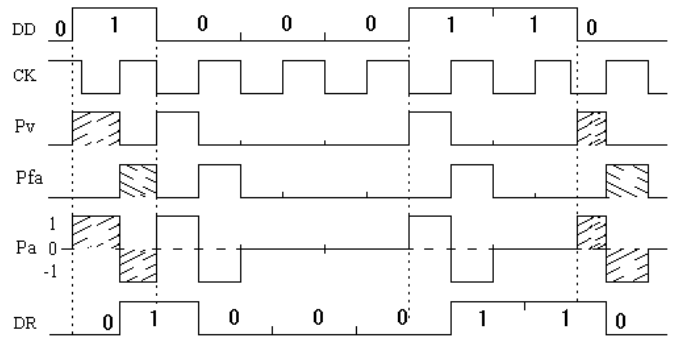


Fig.7 Waveforms of the asynchronous by both at rate automatic

The error pulse P_e don't disappear, but the variable area P_v is equal to the fixed P_f at the equilibrium point.

III. PROPOSAL BY POSITIVE AT QUARTER BIT RATE

The new proposal, asynchronous sequential symbol synchronizers based on pulse comparison operating by positive transitions at quarter bit rate has also two versions namely the manual (ab-m/2) and the automatic (ab-a/2) [3]. The versions difference is in the phase comparator, the variable pulse P_v is common but the fixed P_f is different [4]. Their jitter- SNR curves will be compared with the previous.

A. Proposal by positive at quarter manual(ab-m/4)

The block P_v produces the variable pulse P_v between input transitions and VCO. The manual adjustment delay $T/2$ with Exor produces a fixed pulse P_f (Fig.8).

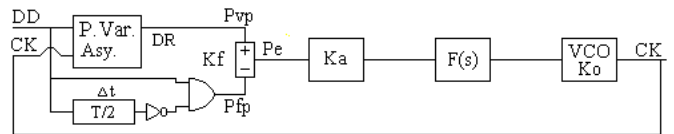


Fig.8 Asynchronous by positive at quarter rate manual (ap-m/4)

The comparison between pulses P_v and P_f provides the error pulse P_e that forces the VCO to synchronize the input. The block P_v is an asynchronous circuit (Fig.9).

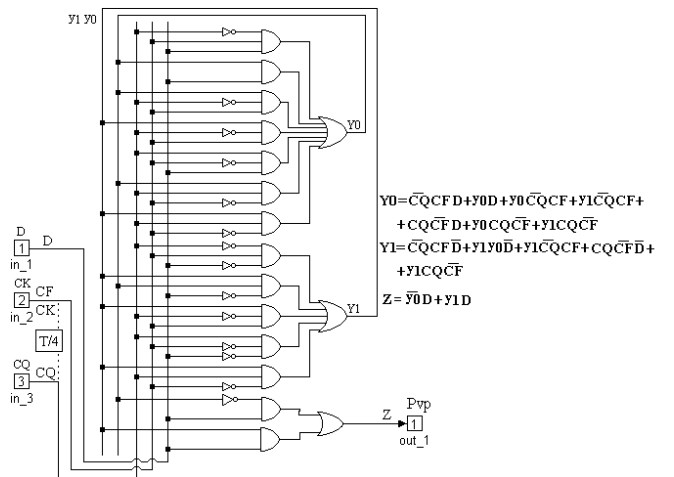


Fig.9 Intern aspect of the block P_v

Fig.10 shows the waveforms of the proposed manual (equal to the corresponding synchronous version) [3].

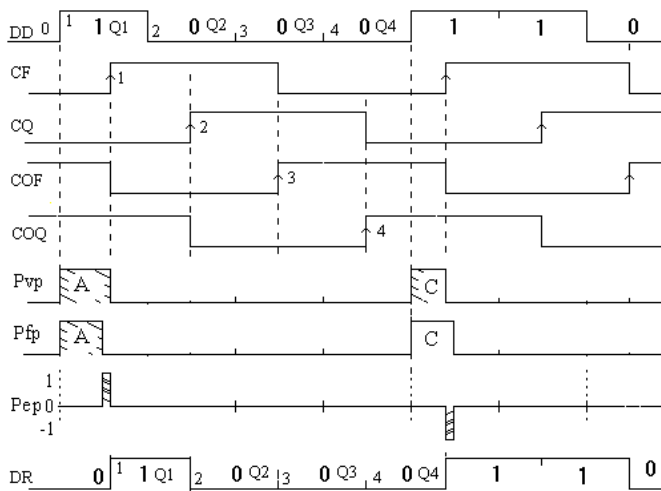


Fig.10 Waveforms of the asynchronous positive at quarter manual

The error pulse P_e diminishes during the synchronization time and disappear at the equilibrium point.

B. Proposal by positive at quarter automatic (ab-a/4)

The block P_v , that is common, produces the variable pulse P_v between input and VCO. The block P_f , shown below, produces the comparison fixed pulse P_f (Fig.11).

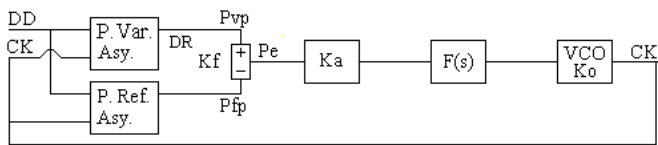


Fig.11 Asynchronous by positive at quarter rate automatic (ap-a/4)

The comparison between the pulses P_v and P_f provides the error pulse P_e that forces the VCO to follow the input. The block P_f is an asynchronous circuit (Fig.12).

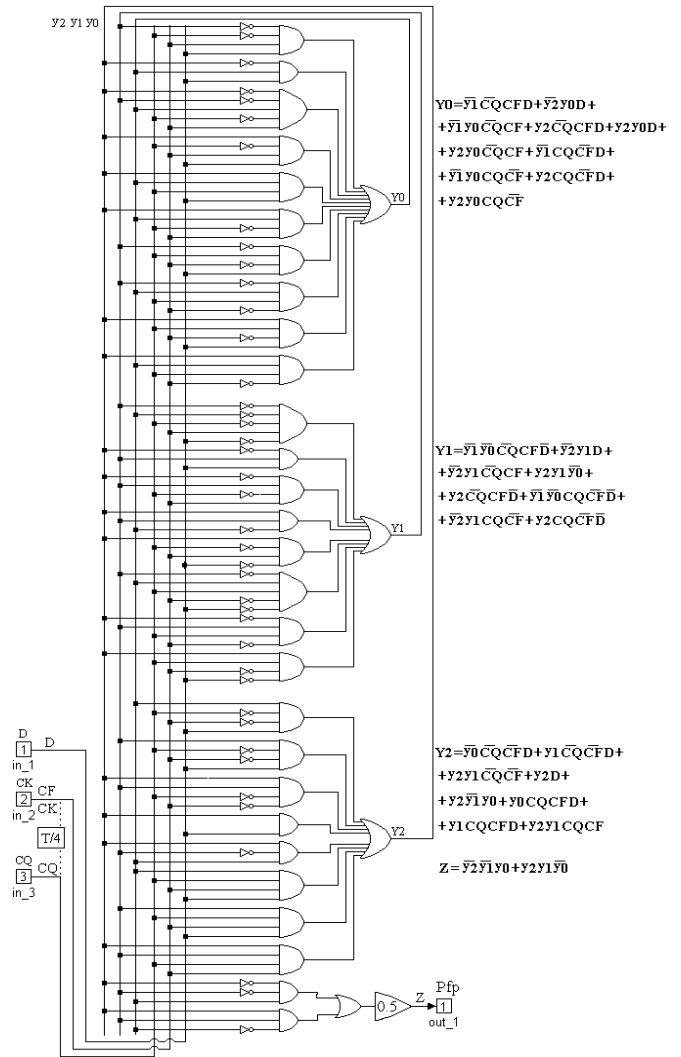


Fig.12 Intern aspect of the block Pf

Fig.13 shows the waveforms of the proposed automatic (equal to the corresponding synchronous version) [3].

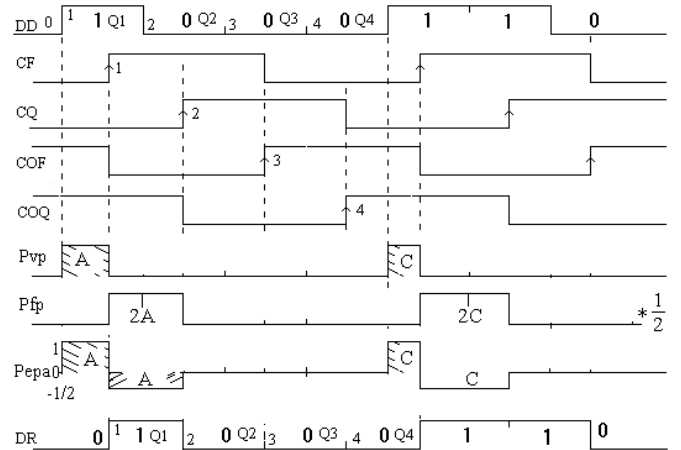


Fig.13 Waveforms of asynchronous positive at quarter automatic

The error pulse P_e don't disappear, but the variable area P_v is equal to the fixed P_f at the equilibrium point.

IV. DESIGN, TESTS AND RESULTS

We present the design, tests and results of the various synchronizers [5].

A. Design

We design all the synchronizers with the same loop gain conditions to have guaranteed results. The loop gain is $Kl = Ka.Kf.Ko$, where Kf and Ko are fixed. The Ka is the variable parameter that controls the loop characteristics.

To facilitate the analysis, we use normalized values for the bit rate $tx=1$ baud, clock frequency $f_{CK}=1$ Hz, extern noise bandwidth $Bn=5$ Hz and loop noise bandwidth $Bl=0.02$ Hz.

We apply a power signal $Ps= A_{ef}^2$ with power noise $Pn= No.Bn= 2\sigma_n^2.\Delta\tau.Bn$, where σ_n is the noise standard deviation and $\Delta\tau=1/f_{Samp}$ is the sampling period.

Then, the relation between SNR and noise variance σ_n^2 is $SNR= Ps/Pn= A_{ef}^2/(No.Bn)= 0.5^2/(2\sigma_n^2*10^{-3}*5)= 25/\sigma_n^2$ (1)

Now, for each synchronizer, we must measure the output jitter UIRMS versus the input SNR

- 1st order loop:

The used cutoff loop filter $F(s)= 0.5$ Hz, which is 25 times greater than $Bl= 0.02$ Hz, eliminates the high frequency but maintains the loop characteristics. The transfer function is

$$H(s)= \frac{G(s)}{1+G(s)} = \frac{KdKoF(s)}{s+KdKoF(s)} = \frac{KdKo}{s+KdKo} \quad (2)$$

the loop noise bandwidth is

$$Bl = \frac{KdKo}{4} = Ka \frac{KfKo}{4} = 0.02 \text{ Hz} \quad (3)$$

So, with $(Km=1, A=1/2, B=1/2, Ko=2\pi)$ and loop bandwidth $Bl=0.02$, we obtain respectively the Ka , for analog, hybrid, combinational and sequential synchronizers, then

$$Bl=(Ka.Kf.Ko)/4 = (Ka.Km.A.B.Ko)/4 \rightarrow Ka=0.08*2/\pi \quad (4)$$

$$Bl=(Ka.Kf.Ko)/4 = (Ka.Km.A.B.Ko)/4 \rightarrow Ka=0.08*2.2/\pi \quad (5)$$

$$Bl=(Ka.Kf.Ko)/4 = (Ka*1/\pi*2\pi)/4 \rightarrow Ka=0.04 \quad (6)$$

$$Bl=(Ka.Kf.Ko)/4 = (Ka*1/2\pi*2\pi)/4 \rightarrow Ka=0.08 \quad (7)$$

For the analog PLL, the jitter is

$$\sigma_\phi^2=Bl.No/Ae f^2=0.02*10^{-3}*2\sigma_n^2/0.5^2=16*10^{-5}.\sigma_n^2 \quad (8)$$

For the others PLLs, the jitter formula is more complicated.

- 2nd order loop:

It is not used here, but provides similar results.

B. Tests

We used the following setup to test synchronizers (Fig.14)

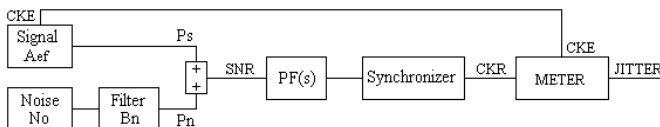


Fig.14 Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock, the difference is the jitter.

C. Results

We present the results in terms of output jitter UIRMS versus input SNR. Fig.15 shows the jitter- SNR curves of the four synchronizers which are the both rate manual(ab-m), the both rate automatic (ab-a), the positive quarter rate manual (ap-m/4) and the positive quarter rate automatic (ap-a/4).

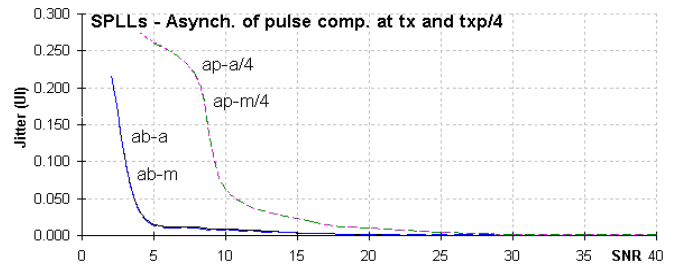


Fig.15 Jitter-SNR curves of the 4 synchro. (ab-m,ab-a,ap-m/4,ap-a/4)

We observe that, in general, the output jitter UIRMS decreases gradually with the input SNR increasing.

We verify that, for high SNR, the four jitter curves tend to be similar. However, for low SNR, the variant asynchronous both at rate manual (ab-m) and automatic (ab-a) are better than the variant asynchronous positive at quarter rate manual (ap-m/4) and automatic (ap-a/4).

V. CONCLUSIONS

We studied four synchronizers involving the standard reference variant asynchronous by both transitions at bit rate with versions manual (ab-m) and automatic (ab-a) and the new proposed variant asynchronous by positive transitions at quarter bit rate with versions manual (ap-m/4) and automatic (ap-a/4). Then, we tested and compared the jitter-SNR curves.

We observed that, in general, the output jitter UIRMS curves decrease gradually with the input SNR increasing.

We verified that, for high SNR, the four synchronizers jitter curves tend to be similar, this is comprehensible since all the synchronizers are digital, with equal noise margin. However, for low SNR, the variant asynchronous by both at rate with their versions manual (ab-m) and automatic (ab-a) are better than the variant asynchronous by positive at quarter rate with their versions manual (ap-m/4) and automatic (ap-a/4), this is comprehensible because the variant by both transitions at rate has minus states than the variant by positive transitions at quarter rate and then, the time to pass from the error state to the correct state is lesser in the 1st case.

In the future, we are planning to extend the present study to other types of synchronizers.

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REFERENCES

- [1] Jean C. Imbeaux, "performance of the delay-line multiplier circuit for clock and carrier synchronization", IEEE Jou. on Selected Areas in Communications p.82 Jan. 1983.
- [2] Werner Rosenkranz, "Phase Locked Loops with limiter phase detectors in the presence of noise", IEEE Trans. on Communications com-30 N°10 pp.2297-2304. Oct 1982.
- [3] Hans H. Witte, "A Simple Clock Extraction Circuit Using a Self Sustaining Monostable Multivibrat. Output Signal", Electronics Letters, Vol.19, Is.21, pp.897-898, Oct 1983.
- [4] Charles R. Hogge, "A Self Correcting Clock Recovery Circuit", IEEE Tran. Electron Devices p.2704 Dec 1985.
- [5] Antonio D. Reis, Jose F. Rocha, Atilio S. Gameiro, Jose P. Carvalho "A New Technique to Measure the Jitter", Proc. III Conf. Telecommunications pp.64-67 FFoz-PT 23-24 Apr 2001.

- [6] Marvin K. Simon, William C. Lindsey, "Tracking Performance of Symbol Synchronizers for Manchester Coded Data", IEEE Transactions on Communications Vol. com-2.5 N°4, pp.393-408, April 1977.
- [7] J. Carruthers, D. Falconer, H. Sandler, L. Strawczynski, "Bit Synchronization in the Presence of Co-Channel Interference", Proc. Conf. on Electrical and Computer Engineering pp.4.1.1-4.1.7, Ottawa-CA 3-6 Sep. 1990.
- [8] Johannes Huber, W. Liu "Data-Aided Synchronization of Coherent CPM-Receiver" IEEE Transactions on Communications Vol.40 N°1, pp.178-189, Jan. 1992.
- [9] Antonio D'Amico, A. D'Andrea, Reggianni, "Efficient Non-Data-Aided Carrier and Clock Recovery for Satellite DVB at Very Low SNR", IEEE Jou. on Sattelite Areas in Comm. Vol.19 N°12 pp.2320-2330, Dec. 2001.
- [10] Rostislav Dobkin, Ran Ginosar, Christos P. Sotiriou "Data Synchronization Issues in GALS SoCs", Proc. 10th International Symposium on Asynchronous Circuits and Systems, pp.CD-Ed., Crete-Greece 19-23 Apr. 2004.
- [11] N. Noels, H. Steendam, M. Moeneclaey, "Effectiveness Study of Code-Aided and Non-Code-Aided ML-Based Feedback Phase Synchronizers", Proc. IEEE Int Conf. on Comm.(ICC'06) pp.2946-2951, Ist.-TK, 11-15 Jun 2006.
- [12] A. D. Reis, J. F. Rocha, A. S. Gameiro, J. P. Carvalho "Carrier Phase Lock Loop and Bit Phase Lock Loop", Proc. IX Symposium on Enabling Optical Network and Sensors (SEONs) p.CD-Edited, Aveiro-PT 1-1 July 2011.
- [13] A. D. Reis, J. F. Rocha, A. S. Gameiro, J. P. Carvalho "Optical Digital Communication Systems and Synchronism", Proc. 7th UBI International Conference on Engeneering (for Economic Development) - ICEUBI 2013, pp. CT8-11.7, Covilhã-PT 27-29 November 2013.
- [14] A. D. Reis, J. F. Rocha, A. S. Gameiro, J. P. Carvalho, "Asynchronous Sequential Symbol Synchronizers based on Pulse Comparison by Both Transitions at Quarter Bit Rate", Proc. World Congress on Engineering 2015 'WCE 2015' pp.416-420, London-UK 1-3 July 2015.