Designing and Simulation of High Efficiency DC-DC Buck Converter Using the Tools Simetrix and Cadence

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***Abstract*—This paper presents the design and simulation of a High Efficiency DC/DC buck converter for mobile applications and systems on a chip (SOC) designed with CMOS technology 0.18 µm using SIMetrix and Cadence simulators. The circuit of the proposed buck converter was designed with both poly and 5 metals. First we compare the performance of the converter modes internal and external coil and the yield of sleep modes and bybass. Finally we present results of simulation of current and output voltages. The range of the supply voltage is [2,5V-5.5V], the nominal switching frequency is 50MHz.**

Index Terms— DC/DC Buck, High Efficiency, CMOS technology, Simetrix and Cadence Simulators.

I. INTRODUCTION

THIS section include the advantages, the characterization and the utilization of the DC-DC buck Converter. Power consumption has become one of the most important issues in modern electronics due to increased complexity and speed of the system. In order to curb the effect of power on a system as a whole, multiple power domains have been proposed as an architecture scheme for low power design. To support multi-Vdd, an array of supply voltages needs to be generated. DC/DC converters can be integrated on chip and convert the input voltage to different voltage levels internally. The first method is convenient for relative low currents (few hundreds of mA) because the cost of an extra switch in the buck scheme limits the power efficiency. To miniaturize the DC-DC converter, the used strategy increases the operating frequency to reduce inductance and capacitance. Target is to obtain small values to enable on-chip or in-package integration, [1-4]. The request of currents below 1 A makes reasonable the sizes of power switches. The dynamic dissipation is relatively low and the operational frequency can be increased from nowadays 5 MHz to several tens or hundreds of MHz. However, high switching frequency causes a quadratic increase of power in the control circuit that quickly becomes a non-negligible fraction of the dynamic dissipation, thus reducing efficiency. Buck converter aims at efficiencies higher than a linear regulator for a large range of the output current [5-25]. If the generated voltage Vout is D times the supply voltage, the efficiency of the linear regulator is D. Therefore, the goal is to keep system efficiency well above D for an extended range of output current. Just obtaining very high switching frequency [1, 2] is not practical. The goal of this design is to achieve for 1-A output current, efficiency higher than what reported in published research results, [3, 4].

This design reduces the power of the control loop at high switching frequency by a novel control strategy. Instead of using op-amps, the design employs current mode processing followed by a voltage-to-pulse converter. The total required current is as low as 45 µA for switching frequencies up to 120 MHz. The buck converter, fabricated in a 0.18-µm CMOS technology with both poly and 5 metals, achieves 93% peak efficiency with 0.3A output current, 2.5-V output voltage, 50-MHz switching frequency and 5.5-V supply voltage. 22µF capacitor and requires clock and Vref/Vramp input of 1,23V.

II. DESIGN TOOLS

A. Simetrix Smulator

The SIMetrix user interface provides an environment where multiple views can be managed within a window [26]. There are a range of views, for example content related views such as the Schematic Editor, Symbol Editor and Waveform Viewer, along with more system related views such as the Command Shell and File Viewer. By dragging a views title bar, views can be rearranged within a window into the layout that best suits the needs. We note that there are conceptually two types of views within SIMetrix. The first, System Views, provide tools to operate the program, which includes the Command Shell and File Viewer. The second, Workspace Views, provide means for developing and reviewing designs, which includes the Schematic Editor and Waveform Viewer.

Catena Software's SIMetrix/SIMPLIS is a popular Circuit Simulation package. SIMetrix/SIMPLIS is a combination ® of two independent circuit simulators: SIMetrix, a SPICE-

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based simulator with numerous enhancements including custom models for power transistor devices; and SIMPLIS, a fast simulator that uses piecewise linear approximations and includes useful analysis modes for switching power supply circuits.

Circuit Simulation using SIMetrix and SIMPLIS in Altium Designer is similar to using Advanced Sim, Altium Designer's built-in simulator. Altium Designer supports SIMetrix/SIMPLIS in three main ways: Direct Simulation from Altium Designer using SIMetrix/SIMPLIS Using models from the SIMetrix/SIMPLIS model library, not only in the native SIMetrix and SIMPLIS simulators but in also in Altium Designer's built-in simulator Exporting Schematics containing simulation models to SIMetrix/SIMPLIS format.

B. Cadence Simulator

Analog Design Environment (ADE) is integrated on Cadence Custom IC Design software. The user can simulate his design (schematic, extracted layout, vhdl, etc.) using the ADE [27]. This tutorial explains necessary steps required in preparing your design and using ADE to simulate the circuit. The tutorial assumes that you have the inverter cell with schematic and symbol views created as described in "Virtuoso Schematic Composer Tutorial" (available on class website).

In the Cadence AMS simulator, compiled objects (modules, macromodules, and user-defined primitives) and other derived data are stored in libraries. The library structure uses a Library Cell: View approach, where:

- A library relates to a specific design or to a reference library.
- Cells relate to specific modules or building blocks of the design.
- Views relate to different representations of the building blocks.

III. Principles of PWM Buck Converters

This section covers the theoretical aspects of the DC-DC Buck converter. A practical method of designing the sliding coefficients is also introduced.

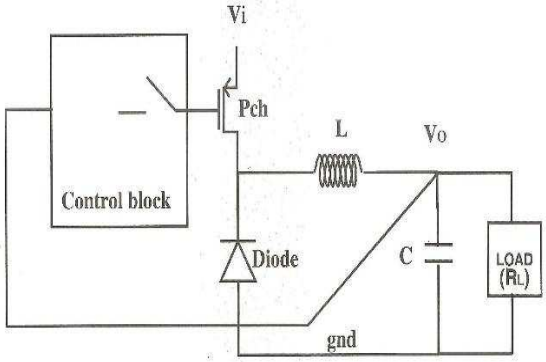

Fig. 1. Bsic Buck Converter Topology.

This converter gives an output voltage vo smaller than the input voltage vs. It is based on the circuit of figure 1.

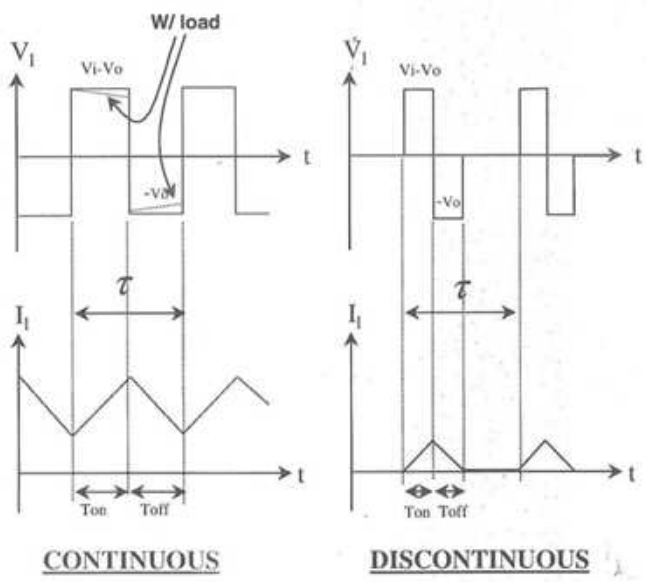

Fig. 2. Inductor voltage and inductor Current.

The figure 2 show the voltage and the current of the inductor in continuous and discontinuous mode.

The operation of a buck converter can be divided into two time according to the state of Pch switch Fig.1 The ON state where the transistor Pch (Q) is on. The current through the inductance increases linearly. The voltage across the diode is negative, no current the crosses. The off-state when the transistor Pch (Q in the equations below) is blocked. The diode becomes conductive. it provides the continuity of the current in the inductor. The current through the inductor decreases.

The buck converter with ideal switching devices will be considered here which is operating with the switching period of T and duty cycle D, [1]. The state equations corresponding to the converter in continuous conduction mode (CCM) can be easily understood by applying Kirchhoff's voltage law on the loop containing the inductor and Kirchhoff's current law on the node with the capacitor branch connected to it. When the ideal switch is ON, the dynamics of the inductor current $i_L(t)$ and the capacitor voltage $v_C(t)$ are given by,

$$\begin{cases} \dfrac{di_L}{dt} = \dfrac{1}{L}(V_{in} - v_o) \\ \dfrac{dv_o}{dt} = \dfrac{1}{C}(i_L - \dfrac{v_o}{R}) \end{cases}, \quad 0 < t < dT, \quad Q:ON$$

and when the switch is OFF are presented by,

$$\begin{cases} \dfrac{di_L}{dt} = \dfrac{1}{L}(-v_o) \\ \dfrac{dv_o}{dt} = \dfrac{1}{C}(i_L - \dfrac{v_o}{R}) \end{cases}, \quad dT < t < T, \quad Q:OFF$$

A. Conduction continue

The voltage of the control of the MOS M1(Fig.4) allows the successive alternation of operating modes ON and OFF (by applying a rectangular voltage PWM to the gate of MOS M1). During the ON state M1 operates in its linear region between the drain and the source from which it is equivalent

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to a low resistance R_{DS}.

The d.d.p between its terminals is V_{DS} = = $R_{DS}i*$ $R_{DS}i_L$.

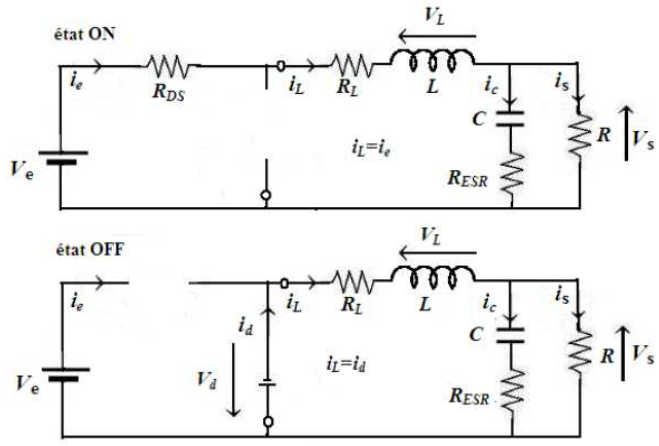

Fig. 3. Mode ON and Mode OFF of DC-DC Buck Converter

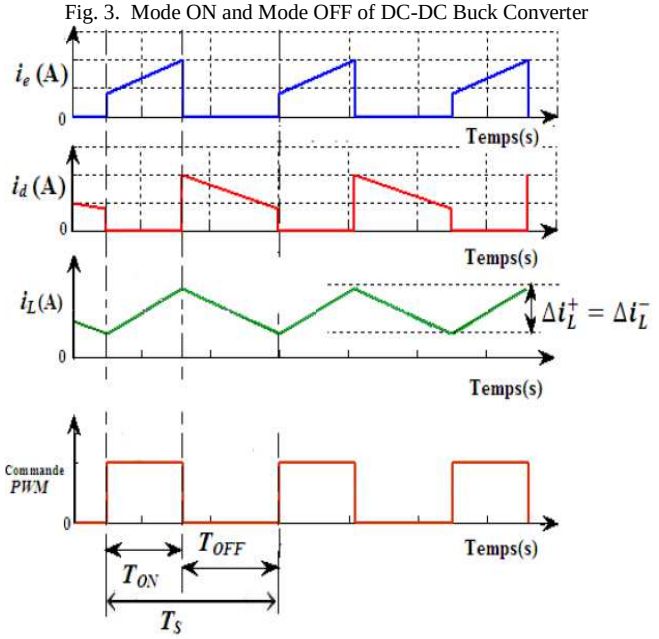

Fig. 4. Current and voltages obtained by continuous conduction of the buck converter

B. Conduction Discontinuous

In some cases, the amount of energy required by the load is low enough to be transferred in a shorter time than a switching period. During this part of the period the transistor M1 and the diode D_a are blocked. [19] The current through the coil is canceled (I_L = 0). The difference between the conduction and continuous conduction is added a third time (standby state) D_{3*}Ts in the period Ts. The circuits of Fig.3 apply except that T_{OFF} is different from (1 - D)*Ts. Fig.5 illustrates the variation with time of the current in the transistor ie, the current id in the diode, the current iL through the coil and the PWM voltage control of buck converter in discontinuous conduction mode.

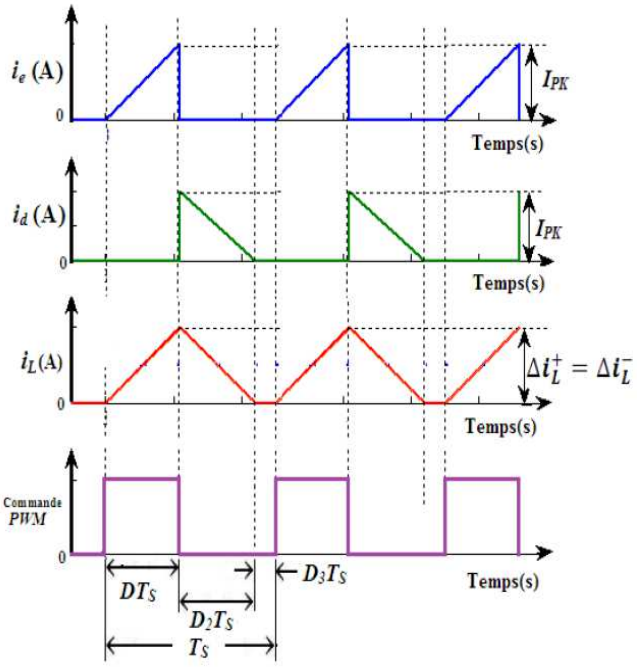

Fig. 5. Current and voltages obtained by discontinuous conduction in a buck converter.

IV. Simulation Results and Discussions

Experimental results show that, at the minimum 2.5V supply, the output control range is [0,5V- 2,45V] with an output current up to 0.3A.

Figure1 shows the yields depending on the load current of the converter internal mode (internal coil) and external mode (external coil). Figure 6 shows the yields depending on the load current of the converter to sleep mode (standby) and ON Mode (Bypass).

The high voltage causes a greater dynamic dissipation This reduces the yield to low current. However low power control (only 35 µA) holds the overall yield nearly a decade under the peak. Figure 7 and Figure 8 shows the currents and voltages across the components of the proposed buck converter, table 1 shows a comparison of the results of the proposed buck converter with references. The simulation results shows that the proposed converter is improved in performance for all modes compared the results.

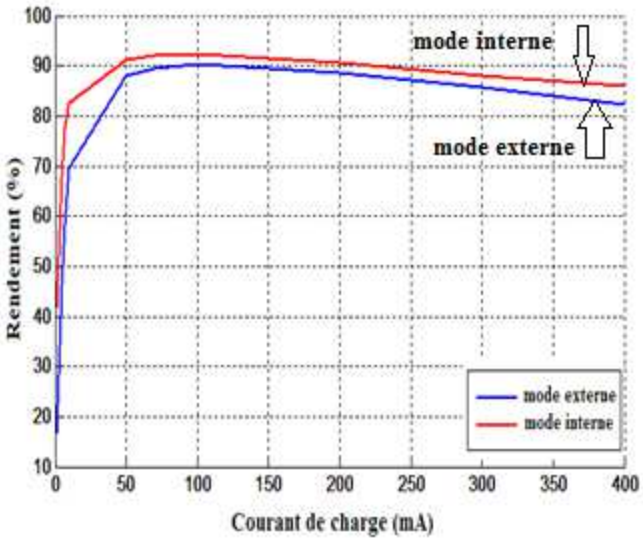

Fig.5. Efficiency Versus the load current performance in internal mode and the external mode

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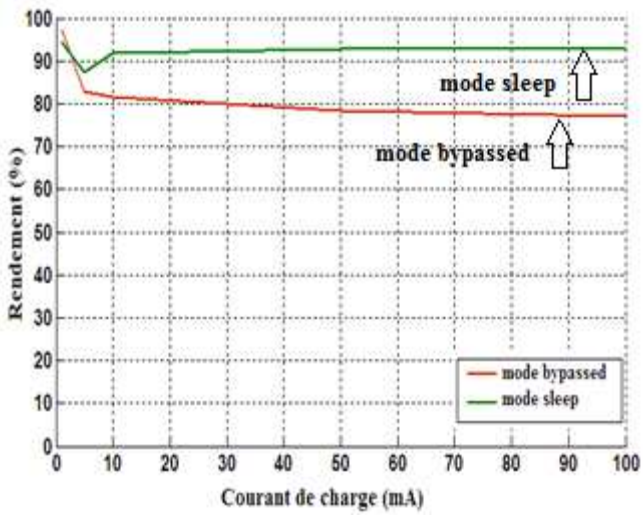

Fig.6. Efficiency Versus the load current

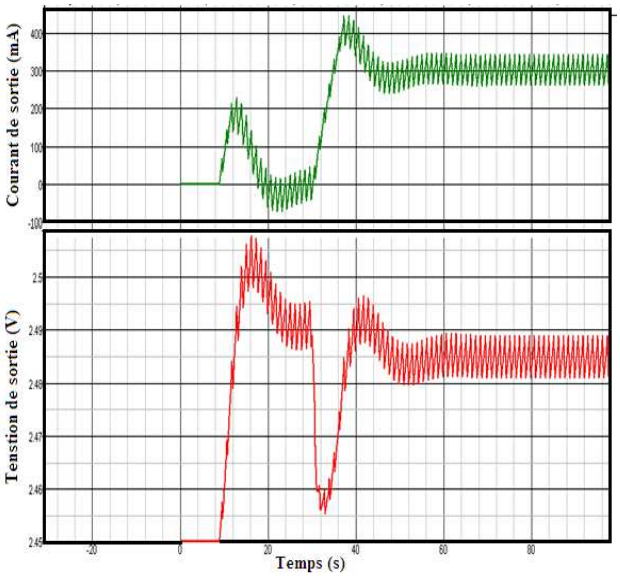

Fig.7. out voltage and output current of the proposed Buck Converter

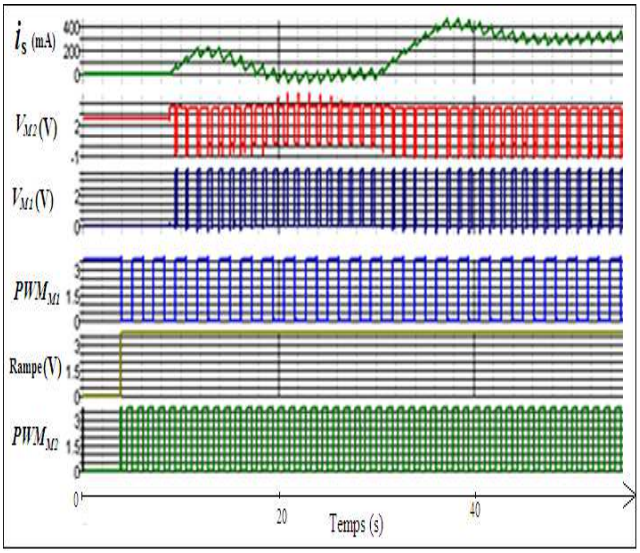

Fig.8. Simulation results of the proposed DCDC Buck Converter

Table 1
Shows a comparison of the results of the proposed buck converter with references.

Reference	Ve(min)	Vs(min)	Fs	Technology	efficiency
[17]	2,5 V	1,8 V	50 MHz	0,13 µm 2-poly 6-metal CMOS	76%
Proposed Buck	2,5 V	0,5 V	50 MHz	0,18 µm 2-poly 5-metal CMOS	90%

V. Conclusion

This paper presented the design and simulations of a DC/DC buck Converter dedicated for mobile applications and systems on a chip (SOC) with CMOS technology 0.18 microns using SIMetrix and Cadence simulators. We achieved a new PWM circuit for controlling this model for different loads to optimize converter efficiency in ON mode (bypass) and sleep mode (standby). We compared the results of the converter output modes internal and external coil bobbin. This model was used of current values of different loads. Against internal loop feedback between the output and the input of the power transistors ensures a switching voltage to zero in real time. This reduces the energy consumed by these transistors and achieves an efficiency of over 90% for a variety of charges. In addition, an external reaction against-loop is used in the PWM circuit to follow the new reference voltage.

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