FPGA Based BLDC Motor Drive For Telescopes

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Abstract - DC motors are well-known for their torquespeed characteristics. It is also known that the brushes and commutators used in brush motors pose maintenance problems due to their wear and Electro Magnetic Interference (EMI) due to the arcing in the brushes and commutator. These EMI affect the low level signals as faced in the radio telescope focal plane instruments. BLDC motors address both these problems and while giving the desirable torque-speed characteristics reduces the maintenance problems posed by the brush dc motors and offer methods for EMI reduction. Many papers have been reported on the BLDC motor controller implementation with microcontrollers, DSPs and FPGAs. The FPGA approach gives the desirable features like electronic commutation and generates the PWM gating pulses to the MOSFET 3-ph full bridge inverter for precise speed controller implementation in an easy programmable way. In this work, a modified approach for PWM generation which achieves accurate speed controller and avoids the triangular carrier comparison is reported. The mathematical modeling has been listed and Simulink modeling is also implemented. A controller has been built in the laboratory for the verification of the expected performance as the Simulink model predicts.

Index terms – BLDC, FPGA, Telescope, PWM, Simulink

I. INTRODUCTION

BLDC motors are gaining acceptance in a progressive way both as main axis drives and for focus control in telescopes. This paper focuses mainly on implementing a focus drive for telescopes. The basic function of a Focus Motor drive in a telescope is to move the secondary accurately to bring the celestial objects to a good focus in the Cassegrain plane. The motor speeds can vary over a range. The low speed requirement compels the designer to use gearboxes with a high gear ratio. Most often, the load is highly nonlinear due to static friction at very low speeds. This necessitates the use of an innermost current loop for torque control for maintaining speed accuracy.

I. CONSTRUCTION AND OPERATION OF THE BLDC MOTOR

A 3-ph BLDC motor consists of a stator made out of laminated steel, slotted and stacked up to carry the 3-ph windings. A BLDC motor with three coils and configured in a star pattern is considered in this work. The rotor in a typical BLDC motor is made out of permanent magnets. (Ref. 1&2)

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A. Electronic Commutation

To make the motor rotate, the coils are energized in a predefined sequence, making the motor turn in one direction. Running the sequence in the reverse order makes the motor run in the opposite direction. The direction of the current determines the orientation of the magnetic field generated by the stator coils. The magnetic field attracts and repels the permanent magnet rotor. By changing the current flow in the coils and thereby the polarity of the magnetic fields at the right moment and in the right sequence, the motor rotates. Alternation of the current through the stator coils is referred to as 'commutation'. A 3-ph BLDC motor has six states of commutation. In six step commutation, only two out of the three BLDC motor windings are energized at a time. The energization sequence is dependent on the rotor position and the motor manual specifies which of the two phases of its three phase windings needs to be energized to obtain continuous torque. The energization sequence for the BLDC motor (Model. AK -21E) is shown in fig 1. Table 1 lists the rotor position and the pair of windings energized. Fig 2 shows the 3-Ph inverter and the stator coil excitation scheme



Fig 1. 6 stages of commutation

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Sectors Degree	Coil Excitation	MOSFET ON
0-60°	W-V	T5,T4
60°-120°	W-U	T5,T2
120°-180°	V-U	T3,T2
180°-240°	V-W	T3,T6
240°-300°	U-W	T1,T6
300°-360°	U-V	T1,T4

Table I sector versus coil excitation



Fig 2-3 phase inverter and stator coil excitation.

Steps are equivalent to 60 electrical degrees. So six steps make a full, 360 degree rotation. When all six states in the commutation sequence have been executed, the sequence is repeated to continue the rotation of the motor. This sequence represents a full electrical rotation. For motors with multiple pole pairs the electrical rotation does not correspond to mechanical rotation. For example in the BLDC motor used in this work, 3 pairs of Poles are used. The mechanical rotation corresponds to three electrical rotations. In a BLDC motor, the commutation is achieved using feedback sensors. Hall Effect Sensors, Resolvers and Optical encoders are commonly used feedback sensors. In this work, a resolver fitted to the motor shaft has been used as the feedback device, whose two signals are converted to a precise shaft position, using a resolver to digital converter (AD2S83) with a resolution of 12-bit.

II. ROLE OF FPGA IN BLDC MOTOR CONTROLLER

Though BLDC drive controllers have been implemented in various ways using microcontrollers and DSPs (ref. 4, 5, 6 & 7), the FPGA approach has been selected due to its flexibility in implementing various functions of the drive. In this work FPGA forms the controller to read-out resolver to digital converter, perform electronic commutation and read the servo error from the analog to digital converter, to implement speed control function by controlling the width of the PWM gated pulses. This scheme of FPGA role in BLDC motor speed controller is shown in fig 3.





For e.g., in the BLDC motor selected in this work, the no. of poles is 6 and for a 50 Hz supply, the speed works out as 1000 rpm. The period of this supply is 20 msec. and the duration of each stage of the 6 step commutation is 3.33 msec. Thus the variable frequency can be configured according to the rpm required. The variable voltage is obtained, using PWM technique by modifying the width of the pulses. This variable voltage sends variable current to the stator coils, according to the required torque of the load.

OPTO

SPEED CONTROLLER OF BLDC MOTOR

ISOLATOR

IN

τN

SERVO

FPGA

SPARTAN-3

Fig 3- FPGA as BLDC motor Controller

RDC

0800

III.

MOSFET

DRIVER

6 -

BLDC MOTOR

GATE

PHASE INVERTER

> 3 EXCITATION STATOR SIGNALS

In this work a hybrid approach has been selected for the BLDC motor speed controller. While the speed loop and the current loop have been implemented using operational amplifiers, the digitized error is read by the FPGA to compute the pulse width sent to the gate control of MOSFETs. A closed loop speed controller requires a reference speed to follow. The motor speed is fed back for determining the error between the reference speed and the motor speed. This error is amplified and fed to a current loop where the error in speed controller and the actual current measured are compared to determine the torque error. This error is amplified and fed to a 8-bit Analog to Digital Converter (Model ADC.0800) This digitized error is fed to the FPGA to determine the PWM width so as to control the stator voltage and current fed to the stator coils. This speed-controller scheme is shown in fig 4.



Fig 4. Block Diagram of Speed Control of a BLDC

The generated gated signals are passed on through optoisolators to the MOSFET gate drivers. The typical PWM waveforms are shown in fig 5.

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Fig 5.Typical PWM waveform exciting the stator Coils.

IV. MATHEMATICAL MODEL AND SIMULINK SIMULATION

A. Electrical Model

$$RI(s) + LsI(s) = V(S) - Ks\theta(s)$$
(1)

$$I(s)(R + Ls) = V(s) - Ks\theta(s)$$
(2)

$$I(s) = \frac{V(s) - Ks\theta(s)}{R + Ls}$$
(3)

B. Mechanical Model

$$J\frac{dw}{dt} + Bw = T_e + T_l$$
(4)

$$Jsw(s) + Bw(s) = K_t I(s) - T_l$$
(5)

$$w(s)[Js + B] = K_t \frac{V(s) - KS\theta(s)}{R + LS}$$
(6)



Fig 6. Block diagram of the BLDC motor

$$G_{v}(s) = \frac{w(s)}{v(s)} = \frac{K}{(R+Ls)(B+Js)+k^{2}}$$
 (7)



Fig 7.Simulation block diagram of the BLDC motor

A three phase BLDC motor equation can be represented as

$v_a = Ri_a + L\frac{di_a}{dt} + e_a$	(8)
$v_b = Ri_b + L\frac{di_b}{dt} + e_b$	(9)
$v_c = Ri_c + L\frac{di_c}{dt} + e_c$	(10)
$e_a = Kf(\Theta_e)w$	(11)
$e_b = Kf\left(\Theta_e - \frac{2\pi}{3}\right)w$	(12)

$$e_c = Kf\left(\Theta_e + \frac{2\pi}{3}\right)w \qquad (13)$$
$$T = \frac{(e_a i_a + e_b i_b + e_c i_c)}{(14)}$$

$$T_e - T_l = J \frac{dw}{dt} + Bw$$
(15)



Fig 8. Block diagram of speed control of BLDC motor



Fig 9.Actual circuit of proportional speed and current loop controller

The Simulink diagram for the specified system is shown in the figure 10.



Fig 10.Simulink Model for BLDC motor controller.

The simulation is performed in MATLAB. The simulation results for closed loop operation of the motor are shown below:



Fig 11.Stator Current waveform.

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Fig 12. Phase Back EMF waveform



Fig 13.Motor speed response.

V. HARDWARE DESCRIPTION

A. BLDC Motor

The Kollmorgen motor AKM 21E (Ref.3) has been used in this work in bringing up the speed controller in our laboratory. This BLDC motor has a resolver mounted on its rotor shaft to provide rotor angular position. This motor provides a rated torque of 0.41Nm at the rated speed of 7000 rpm. Other features of this motor are listed below:

Rated Power	:	0.3KW
Back emf constant	:	10.2 V /Krpm
Torque constant	:	0.41 Nm /Arms
Static friction	:	0.002Nm
Viscous Damping	:	0.0046Nm/Krpm
Inertia	:	0.107Kg-Cm squared

B. FPGA

The Spartan-3 FPGA (Ref.12) with advanced process technology delivers more functionality in BLDC motor controller. The Spartan-3 family is a superior alternative to mask programmed ASICs. To avoid the high initial cost, the lengthy development cycles, and the inherent inflexibility of conventional ASICs. FPGA programmability permits to the modification in the field without disturbing the hardware setup, which is impossibility with ASICs. The Spartan-3 XC3S400 device consist of 896 Configurable Logic Blocks (CLBs) contain RAM-based Look-Up Tables (LUTs) to implement logic and storage elements so no need of external memory. Input/output Blocks (IOBs) control the flow of data between the 116 I/O pairs. Digital Clock Manager (DCM) blocks provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase shifting clock signals.

C. RDC

The resolver mounted on the motor shaft works on the transformer principle. The primary winding is on the resolver's rotor and depending on its shaft angle; the induced voltage in the two secondary windings shifted by 90 degrees would be different. The position information is obtained in a digital format using an Analog Devices Resolver to Digital Converter (RDC) (AD2S83)(Ref.11). The RDC also provides velocity signal in analog form with a 32.5 rpm/rps.

D. Hall Sensor for measuring motor current

LEM sensor HX10P has been used for measuring motor current. This Hall Sensor can measure upto \pm 10A and provides an output of \pm 4V for the full range current. This LEM sensor output is compared with the speed controller output to generate the torque error.(Ref.13)

E. Analog to Digital Converter

A 8-bit analog to digital converter from Analog Devices (ADC 080) has been used to convert the torque error into a digital number. The conversion speed of this ADC is 50 microseconds. With an input range of \pm 5V. (ref.14)

VI. SOFTWARE ROUTINES

BLDC motor controller is mainly working in three stages. Initially FPGA reads the current position value through RDC and generates the commutation sequence which activates suitable MOSFETs in inverter bridge circuit. Once motor starts rotating it provides motor feedback as resolver. Secondly resolver data is converted into digital form with the help of RDC. RDC provides not only position in digital form which provides servo error as a velocity feedback. Servo error is converted into digital form with the help of ADC0800. Thirdly to overcome from these errors PWM signal are used. Motor speed varies with respect to change in voltage. To achieve the variation in voltage here PWM signals are generated and controlled through generating different duty cycle.100% duty cycle provides full speed. The duty cycle value varies to achieve error free result with respect to velocity feedback in terms of digital.

VII. EMI AND ITS REDUCTION IN BLDC DRIVE

EMI problems arise due to the sudden changes in voltage (dv/dt) or currents (di/dt) levels in a waveform (Refs.9). For example, in the inverter that is used in BLDC drives,

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switching occurs to generate the quasi-square waveform and pulse width modulation is often used to control the voltage supplied to the motor to control its speed. Any fast switching device creates similar high dv/dt and di/dt in the waveforms. A conductor carrying a high dv/dt acts like an antenna, and the radiated high frequency wave may couple to a sensitive signal circuit as in Radio Telescope detectors. Parasitic coupling capacitor may carry this noise signal through ground wire. Similarly, a high di/dt current wave may create conducted EMI through a parasitic mutual inductance. Proper shielding, noise filtering, careful equipment layout and grounding have been used in this work to reduce the EMI problems (Ref.10).

VIII. CONCLUSION

A BLDC motor Spartan-3 based BLDC motor controller was built and tested in two rpms. The speed following worked within the designed band of 4%. Though this initial effort focused on the controller for a modest power rated motor, this effort would help in building a more powerful BLDC controller to address the main drives in telescopes.

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