Prefilter Bandwidth Effects in Data Phase Synchronizers of Closed Loop

Antonio D. Reis, Jose F. Rocha, Atilio S. Gameiro and Jose P. Carvalho

Abstract – **This work studies the prefilter bandwidth effects on the data phase synchronizers of closed loop.**

The prefilter changes its bandwidth, first B1=∞ (infinite), after B2=2.tx and next B3=1.tx, tx is the bit rate.

We consider also four data phase synchronizers or data phase lock loop namely the analog (DPLL_ana), hybrid (DPLL_hib), combinational (DPLL_cmb) and sequential (DPLL_seq).

The objective is to study the prefilter bandwidth with the four data synchronizers and to evaluate their output jitter UIRMS (Unit Interval Root Mean Square) versus input SNR (Signal to Noise Ratio).

***Index Terms*—Prefilter, Digital Communication Systems**

I. INTRODUCTION

This work studies the effects of the prefilter of three bandwidths applied before four data phase synchronizers.

The prefilter selects one of its 3 bandwidths B, first B1=∞ (infinite), after B2=2.tx and next B3=1.tx. tx is the bit rate.

We consider also four data synchronizers namely the analog (DPLL_ana), hybrid (DPLL_hib), combinational (DPLL _cmb) and sequential (DPLL_seq). The difference between them is in the phase comparator [1, 2, 3, 4, 5, 6, 7].

The synchronizer has a phase comparator and a VCO (Voltage Controlled Oscillator) and synchronizes the VCO output clock feedback with the main input data transitions. The clock samples and retimes the data and deternines, in parte, the system quality [8, 9, 10, 11, 12, 13].

The synchronizer has three main blocks which are the input adapter circuit, the clock recovery and the output decision circuit. The adapter generates a pulse T/2 to facilitate the synchronism. Fig.1 shows the prefilter with the synchronizer.

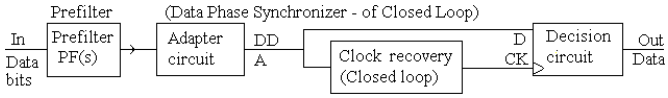

Fig.1 Prefilter with the data phse synchronizer of closed loop

PF(s) is the prefilter (low pass). The other blocks are the phase comparator gain Kf, the loop filter (Fs), the VCO gain Ko and the loop gain factor Ka, that controls the root locus and then the loop characteristics.

In prior and actual art- state was developed various synchronizers, now it is need to know their performance.

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The motivation is to see the prefilter effects. This contribution increases the knowledge about synchronizers.

Following, we present the prefilter with its three different bandwidths (B1=∞, B2=2.tx, B3=1.tx).

After, we present the four data bits phase synchronizers of closed loop: analog (DPLL_ana), hybrid (DPLL _hib), combinational (DPLL_cmb) and sequential (DPLL_seq).

Next, we present the design and tests. Then, we present the results. Finally, we present the conclusions.

II. PREFILTER BANDWIDTH EFFECTS

The prefilter, applied before the synchronizer, filters the noise but disturbs slightly the signal. The prefilter bandwidth B is switched between 3 values (B1=∞, B2=2.tx, B3=1.tx).

Fig.2 shows the prefilter with its three bandwidths.

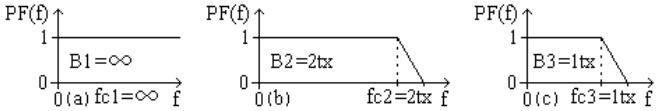

Fig.2 Three prefilter bandwidths: a) B1=∞; b) B2=2.tx; c) B3=1.tx

a) First (Fig.2a), the prefilter has a bandwidth equal to infinite (B1= ∞).

b) Second (Fig.2b), the prefilter has a bandwidth equal two times the bit rate (B2 = 2.tx).

c) Third (Fig.2c), the prefilter has a bandwidth equal to the bit rate (B3 = 1.tx).

We will evaluate the three bandwidth effects (B1, B2, B3) on the jitter-SNR curves of the four data synchronizers.

III. FOUR SYNCHRONIZERS OF CLOSED LOOP

This synchronizer has all its components inside of the loop. We consider four DPLL (Data Phase Lock Loop) namely the analog, hybrid, combinational and sequential [1, 2].

The difference between them is within the phase comparator since the others blocks are equal.

A. Analog closed loop data synchronizer

The analog closed loop synchronizer has a phase comparator based on analog components such as the multiplier (Fig.3).

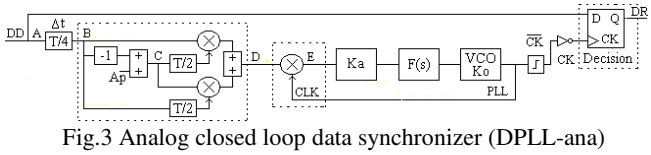

Fig.3 Analog closed loop data synchronizer (DPLL-ana)

This DPLL inputs (main input and VCO output feedback) are both analog.

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B. Hybrid closed loop data synchronizer

The hybrid closed loop synchronizer has a phase comparator based on hybrid components such as the real switch (Fig.4).

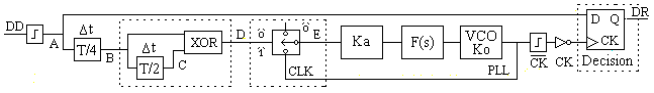

Fig.4 Hybrid closed loop data synchronizer (DPLL-hib)

This DPLL main input is digital but the VCO output feedback continues to be analog.

C. Combinational closed loop data synchronizer

The combinational closed loop synchronizer has a phase comparator based on combinational components such as the AND gate (Fig.5).

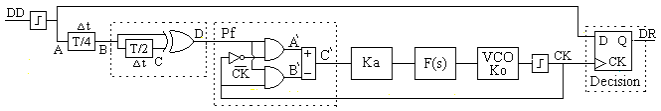

Fig.5 Combinational closed loop data synchronizer (DPLL-cmb)

This DPLL inputs (main input and VCO output feedback) are both digital, but the output is only function of the inputs.

D. Sequential closed loop data synchronizer

The sequential closed loop synchronizer has a phase comparator based on sequential components such as the flip flop (Fig.6).

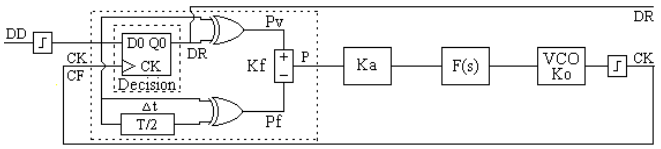

Fig.6 Sequential closed loop data synchronizer (DPLL-seq)

This DPLL inputs (main input and VCO output feedback) are both digital, but the output is function of the inputs and also of the state.

IV. DESIGN, TESTS AND RESULTS

We show the design, tests and results of the various synchronizers [5].

A. Design

We design all the sysnchronizers with the same loop gain conditions, to get reliable resuslts. The loop gain is Kl=KdKo=KaKfKo, where Kf and Ko are fixed and Ka is the loop gain, that controls the roots and the loop characteristics.

To simplify the analysis, we use normalized values for the bit rate tx=1baud, clock frequency fck=1Hz, extern noise bandwidth Bn= 5Hz and loop noise bandwidth Bl= 0.02Hz.

We use a signal power Ps= A^2_{ef} with noise power Pn= No.Bn= $2\sigma n^2.\Delta\tau.Bn$, where σn is the noise standard deviation and $\Delta\tau$ =1/fSamp is the sampling period. The relation between SNR and noise variance σn^2 is

$$SNR= Ps/Pn= A^2_{ef}/(No.Bn)= 0.5^2/(2\sigma n^2*10^{-3}*5)= 25/\sigma n^2 \quad (1)$$

So, for each synchronizer, we must measure the output jitter UIRMS versus the input SNR

- 1st order loop:

The loop filter F(s)=1, with cutoff fc=0.5Hz that is 25 times greater than Bl= 0.02Hz, eliminates the high frequencies but maintains the loop characteristics. The transfer function is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKoF(s)}{s+KdKoF(s)}=\frac{KdKo}{s+KdKo} \quad (2)$$

the loop noise bandwidth is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (3)$$

So, with (Km=1, A=1/2, B_a=1/2, B_h=0.45, Ko=2π) and loop bandwidth Bl=0.02, we obtain respectively the Ka, for analog, hybrid, combinational and sequential sysnchronizers:

$$Bl=0.02=(Ka.Km.A.B_a.Ko)/4 \rightarrow Ka_a=0.08*2/\pi \quad (4)$$
$$Bl=0.02=(Ka.Km.A.B_h.Ko)/4 \rightarrow Ka_h=0.08*2.2/\pi \quad (5)$$
$$Bl=0.02=(Ka*1/\pi*2\pi)/4 \rightarrow Ka_c=0.04 \quad (6)$$
$$Bl=0.02=(Ka*1/2\pi*2\pi)/4 \rightarrow Ka_s=0.08 \quad (7)$$

For the analog PLL, the jitter is

$$\sigma_\phi^2=Bl.No/Aef^2=0.02*10^{-3}*2\sigma n^2/0.5^2=16*10^{-5}.\sigma n^2 \quad (8)$$

For the others PLLs, the jitter formula is more complicated.

- 2nd order loop:

It is not used here, but it gives similar results.

B. Tests

Following Fig.7 shows the setup that was used to test the various synchronizers.

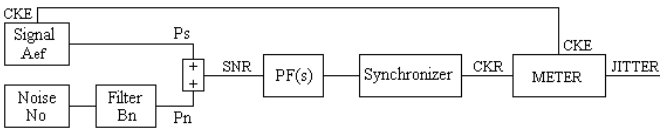

Fig.7 Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock without jitter, the difference is the jitter of the received clock.

C. Jitter measurer (Meter)

The jitter measurer (Meter) consists of a RS flip flop, which detects the random variable phase of the recovered clock (CKR), relatively to the fixed phase of the emitter clock (CKE). This relative random phase variation is the recovered clock jitter (Fig.8).

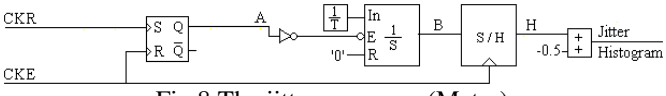

Fig.8 The jitter measurer (Meter)

The other blocks convert this random phase variation into a random amplitude variation, which is the jitter histogram.

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Fig.9 illustrates the operation of the jitter measurer.

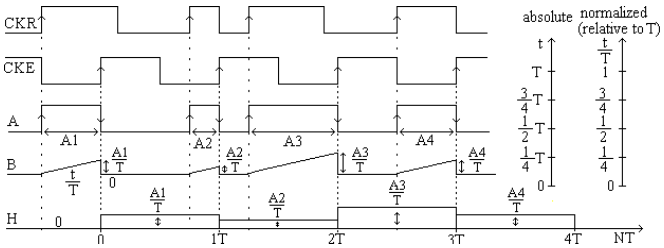

Fig.9 Waveforms at the jitter measurer

Then, the jitter histogram is sampled and processed by an appropriate program, providing the RMS jitter and the peak to peak jitter.

D. Results

We will present the results (output jitter - input SNR) for the prefilter with the four closed loop data synchronizers.

Fig.10 shows the jitter - SNR curves of the prefilter B1=∞ with the four data synchronizers of closed loop namely the analog (DPLL-ana), hybrid (DPLL-hib), combinational (DPLL-cmb) and sequential (DPLL-seq).

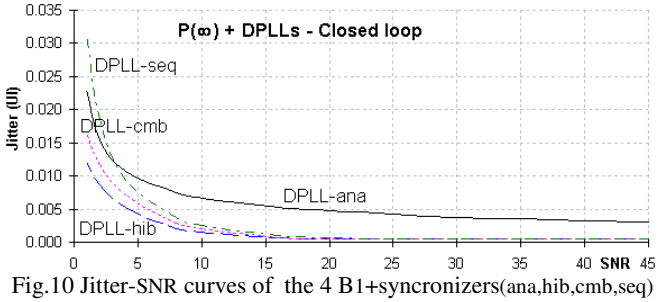

Fig.10 Jitter-SNR curves of the 4 B1+syncronizers(ana,hib,cmb,seq)

We see that, in general, the output jitter UIRMS decreases more or less exponentially with the input SNR increasing.

For prefilter B1=∞, for high SNR, we verify that the synchronizers with input limiter (DPLL-hib, DPLL-cmb, DPLL-seq) are similar and have a slightly advantage over the synchronizer without input limiter (DPLL-ana).

For low SNR, the synchronizers without intern memory (DPLL-ana, DPLL-hib, DPLL-cmb) have a slightly advantage over the synchronizer with intern memory (DPLL-seq).

Fig.11 shows the jitter - SNR curves of the prefilter B2=2.tx with the four data synchronizers of closed loop namely the analog (DPLL-ana), hybrid (DPLL-hib), combinational (DPLL-cmb) and sequential (DPLL-seq).

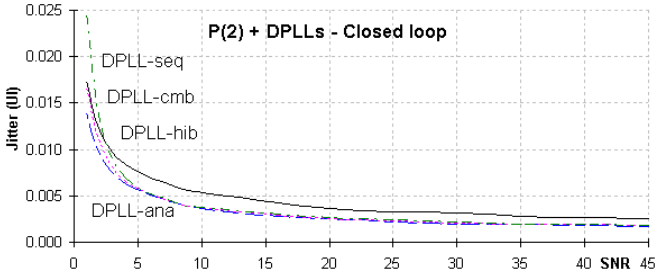

Fig.11 Jitter-SNR curves of the 4 B2+syncronizers(ana,hib,cmb,seq)

For prefilter B2=2.tx, it becomes the jitter - SNR curves more similar between them. For high SNR it is prejudicial, but for low SNR it is beneficial.

Fig.12 shows the jitter - SNR curves of the prefilter B3=1.tx with the four symbol synchronizers of closed loop namely the analog (DPLL-ana), hybrid (DPLL-hib), combinational (DPLL-cmb) and sequential (DPLL-seq).

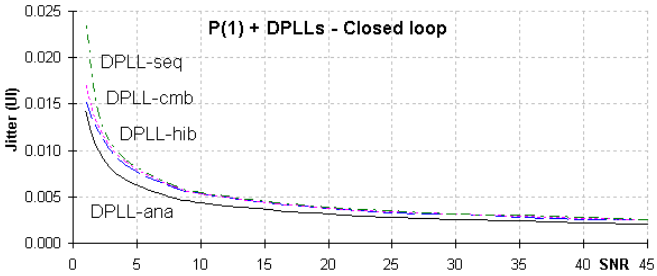

Fig.12 Jitter-SNR curves of the 4 B3+syncronizers(ana,hib,cmb,seq)

For prefilter B3=1.tx, it becomes the jitter - SNR curves still more similar between them. For high SNR it is more prejudicial (malefic) and for low SNR it is less benefic in relation to the previous case.

V. CONCLUSIONS AND FUTURE WORK

We studied the effects of the prefilter of three bandwidths B (B1=∞, B2=2.tx, B3=1.tx) applied before the four data synchronizers of closed loop namely the analog (DPLL-ana), hybrid (DPLL-hib), combinational (DPLL-cmb) and sequential (DPLL-seq). Then, we tested their output jitter UIRMS versus input SNR.

We noted that, in general, the output jitter UIRMS decreases gradually with the input SNR increasing.

For the prefilter B1=∞ (greater), for high SNR, we verified that the data synchronizers with input limiter (DPLL-hib, DPLL-cmb, DPLL-seq) are similar and have a slightly advantage over the other synchronizers without input limiter (SPLL-ana). This is comprehensible since the input limiter noise margin ignores low noise spikes.

However, for low SNR, the synchronizers with intern memory (DPLL-seq) have a slightly disadvantage over the synchronizers without intern memory (DPLL-ana, DPLL-hib, DPLL-cmb). This is comprehensible since the high noise spikes provokes error states that increases the jitter. Also, this disadvantage can be minimized with the prefilter. Anyway, the intern memory provides some project potentialities.

For the prefilter B2=2.tx (medium), it becomes the synchronizers jitter-SNR curves more similar between them.

For the prefilter B3=1.tx (lesser), it becomes the jitter - SNR curves still more similar between themselves.

The prefilter B3, for hign SNR, it is more prejudicial than B2, and for low SNR it is less bebeficial than B2.

In short, the prefilter is beneficial for low SNR and prejudicial for high SNR.

In the future, we are planning to study the effects of the prefilter in other new synchronizers.

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