Prefilter Bandwidth Effects in Carrier Phase Synchronizers

Antonio D. Reis, Jose F. Rocha, Atilio S. Gameiro and Jose P. Carvalho

Abstract - **This work studies the effects of the prefilter bandwidth on the carrier phase synchronizers.**

We apply three different prefilter bandwidth namely B1=¥ (infinite), B2=2.tx and B3=1.tx, where tx is the transmission rate.

We consider also four carrier wave phase synchronizers namely the analog (ana), the hybrid (hib), the combinational (cmb) and the sequential (seq).

The objective is to study the prefilter bandwidth with the four carrier synchronizers and to evaluate their output jitter UIRMS (Unit Interval Root Mean Square) versus input SNR (Signal to Noise Ratio).

***Index Terms*—Prefilter, Digital Communication Systems**

I. INTRODUCTION

This work studies the prefilter bandwidth effects on the jitter - noise behavior of four carrier synchronizer types.

The Butterworth prefilter, applied before the synchronizer, varies their bandwidth between three values: first B1=∞, next B2=2.tx and after B3=1.tx, tx is the transmission rate value.

The carrier phase synchronizers has four types namely the analog (ana), the hybrid (hib), the combinational (cmb) and the sequential (seq) [1, 2, 3, 4, 5, 6, 7, 8].

The difference between the four synchronizers is only in the phase comparator, hence, the other blocks are equals.

The carrier synchronizer is able to synchronize its output VCO (Voltage Controlled Oscillator) directly with the main input carrier. The VCO output carrier is an improved quality version of the input carrier [9, 10, 11, 12, 13, 14].

Fig.1 shows the prefilter followed of the synchronizer.

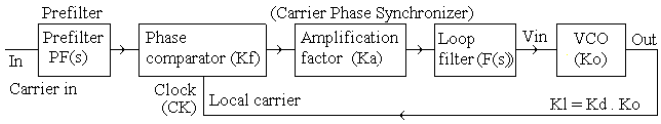

Fig.1 Prefilter with the carrier synchronizer

PF(s) is the prefilter (low pass). The synchronizer has various blocks namely, Kf is the phase comparator gain, (Fs) is the loop filter, Ko is the VCO gain and Ka is the loop gain factor, that controls the root locus and loop characteristics.

In prior and actual art-state was developed various synchronizers, now is necessary to know their performance.

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The motivation of this work is to create new synchronizers and to see the prefilter effects. This contribution increases the know how about the prefilter effects in synchronizers.

Following, we present the prefilter with their three different bandwidths (B1=∞, B2=2.tx, B3=1.tx). Next, we present the four carrier synchronizers namely the analog (ana), hybrid (hib), combinational (cmb) and sequential (seq).

After, we present the design and tests. Then, we present the results. Finally, we present the conclusions.

II. PREFILTER BANDWIDTH EFFECTS

The prefilter applied before the synchronizer, filters the noise but disturbs slightly the signal. The prefilter bandwidth is switched between three values (B1=∞, B2=2.tx, B3=1.tx).

Fig.2 shows the prefilter with their three bandwidths.

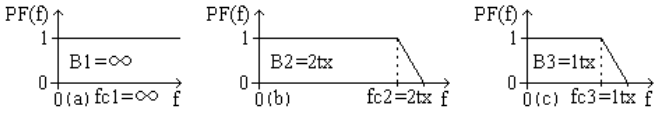

Fig.2 Three bandwidths prefilter: B1=∞ (a), B2=2.tx (b), B3=1.tx (c)

a) First (Fig.2a), the prefilter has a bandwidth equal to infinite (B1= ∞).

b) Second (Fig.2b), the prefilter has a bandwidth equal two times the transmission rate (B2 = 2.tx).

c) Third (Fig.2c), the prefilter has a bandwidth equal to the transmission rate (B3 = 1.tx).

We will evaluate the three bandwidth effects (B1, B2, B3) on the jitter-SNR curves of the four carrier synchronizers.

III. FOUR CARRIER PLLs

We present the four carrier phase synchronizers, or carrier phase lock loop (CPLL), namely the analog, the hybrid, the combinational and the sequential. The difference between them is only in the phase comparator [2].

A. Analog carrier PLL

The analog carrier PLL has a phase comparator based on the ideal multiplier (analog component) (Fig.3).

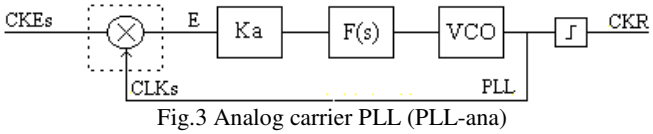

Fig.3 Analog carrier PLL (PLL-ana)

The phase comparator inputs (main input and VCO output feedback) are both analog.

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B. Hybrid carrier PLL

The hybrid carrier PLL has a phase comparator based on the switch or real multiplier (hybrid component) (Fig.4).

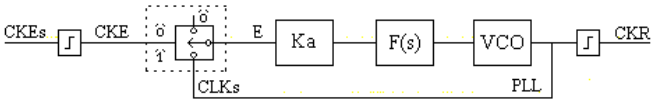

Fig.4 Hybrid carrier PLL (PLL-hib)

The phase comparator main input is now digital, but the input coming from the VCO output feedback is still analog.

C. Combinational carrier PLL

The combinational carrier PLL has a phase comparator based on the exor gate (combinational component) (Fig.5).

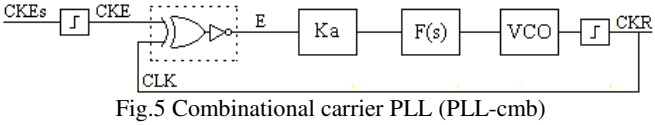

Fig.5 Combinational carrier PLL (PLL-cmb)

The phase comparator inputs (main input and VCO output feedback) are both digital. The output is only function of the inputs.

D. Sequential carrier PLL

The sequential carrier PLL has a phase comparator based on the flip flop (sequential component) (Fig.6).

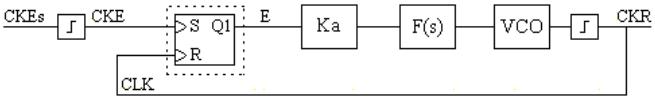

Fig.6 Sequential carrier PLL (PLL-seq)

The phase comparator inputs (main input and VCO output feedback) are both digital. The output is function of the inputs and phase comparator state (circuit with memory).

IV. DESIGN, TESTS AND RESULTS

We will present the design, the tests and the results of the referred synchronizers [5].

A. Design

To get guaranteed results, it is necessary to dimension all the synchronizers with equal conditions. Then it is necessary to design all the loops with identical linearized transfer functions.

The general loop gain is Kl=Kd.Ko=Ka.Kf.Ko where Kf is the phase comparator gain, Ko is the VCO gain and Ka is amplification factor that controls the root locus that provides the desired characteristics.

For analysis facilities, we use a normalized transmission rate tx=1baud, what implies also normalized values for the others dependent parameters. So, the normalized clock frequency is fCK=1Hz.

We choose a normalized external noise bandwidth Bn = 5Hz and a normalized loop noise bandwidth Bl = 0.02Hz. Later, we can disnormalize these values to the appropriated transmission rate tx.

Now, we will apply a signal with noise ratio SNR given by the signal amplitude Aef, noise spectral density No and external noise bandwidth Bn, so the SNR = $A^2_{ef}/(No.Bn)$. But, No can be related with the noise variance σn and inverse sampling Δτ=1/Samp, then $No=2\sigma n^2.\Delta\tau$, so:

$SNR=A^2_{ef}/(2\sigma n^2.\Delta\tau.Bn) = 0.5^2/(2\sigma n^2*10^{-3}*5)= 25/\sigma n^2$ (1)

After, we observe the output jitter UI as function of the input signal with noise SNR. The dimension of the loops is

- 1st order loop:

The loop filter F(s)=1 with cutoff frequency 0.5Hz (Bp=0.5 Hz is 25 times bigger than Bl=0.02Hz) eliminates only the high frequency, but maintain the loop characteristics.
The transfer function is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKoF(s)}{s+KdKoF(s)}=\frac{KdKo}{s+KdKo} \quad (2)$$

the loop noise bandwidth is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (3)$$

Then, for the analog synchronizers, the loop bandwidth is
$Bl=0.02=(Ka.Kf.Ko)/4$ with (Km=1, A=1/2, B=1/2; Ko=2π)
$(Ka.Km.A.B.Ko)/4 = 0.02 \rightarrow Ka_a=0.08*2/\pi$ (4)

For the hybrid synchronizers, the loop bandwidth is
$Bl=0.02=(Ka.Kf.Ko)/4$ with (Km=1, A=1/2, B=0.45; Ko=2π)
$(Ka.Km.A.B.Ko)/4 = 0.02 \rightarrow Ka_h=0.08*2.2/\pi$ (5)

For the combinational synchronizers, the loop bandwidth is
$Bl=0.02=(Ka.Kf.Ko)/4$ with (Kf=1/π; Ko=2π)
$(Ka*1/\pi*2\pi)/4 = 0.02 \rightarrow Ka_c=0.04$ (6)

For the sequential synchronizers, the loop bandwidth is
$Bl=0.02=(Ka.Kf.Ko)/4$ with (Kf=1/2π; Ko=2π)
$(Ka*1/2\pi*2\pi)/4 =0.02 \rightarrow Ka_s=0.08$ (7)

The jitter depends on the RMS signal Aef, on the power spectral density No and on the loop noise bandwidth Bl.

For the analog PLL the jitter is $\sigma\phi^2=Bl.No/Aef^2$
$\sigma\phi^2 = Bl.2.\sigma n^2.\Delta\tau/Aef^2=0.02*10^{-3}*2\sigma n^2/0.5^2=16*10^{-5}.\sigma n^2$ (8)
For the others PLLs the jitter formula is more complicated.

- 2nd order loop:

The second order loop is not shown here, but the results are identical to the ones obtained above for the first order loop.

B. Tests

The following figure (Fig.7) shows the setup that was used to test the various synchronizers.

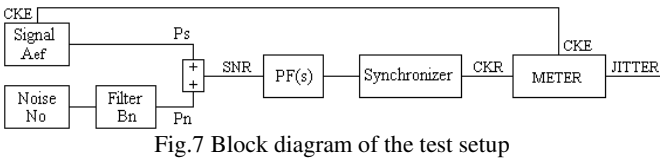

Fig.7 Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock without jitter, the difference is the jitter of the received clock.

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C. Jitter measurer (Meter)

The jitter measurer (Meter) consists of a RS flip flop, which detects the random variable phase of the recovered clock (CKR), relatively to the fixed phase of the emitter clock (CKE). This relative random phase variation is the recovered clock jitter (Fig.8).

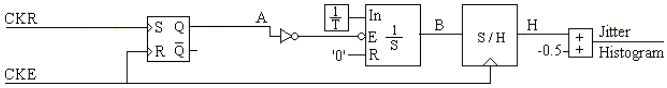

Fig.8 The jitter measurer (Meter)

The other blocks convert this random phase variation into a random amplitude variation, which is the jitter histogram.

Fig.9 shows the operation mode of the jitter measurer.

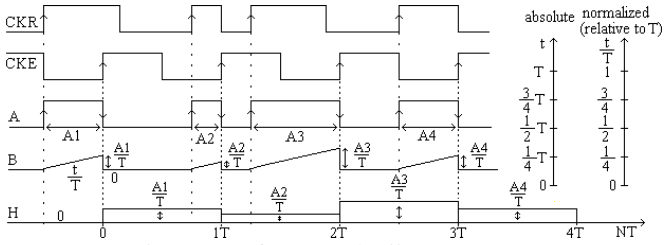

Fig.9 Waveforms at the jitter measurer

Then, the jitter histogram is sampled and processed by an appropriate program, providing the UIRMS jitter and the peak to peak jitter UIPP.

D. Results

We present the results (output jitter UIRMS - input SNR) for the prefilter with the four carrier PLLs.

Fig.10 shows the jitter-SNR curves of the prefilter bandwidth B1= ∞, with the four carrier PLLs: analog (PLL-ana), hybrid (PLL-hib), combinational (PLL-cmb) and sequential (PLL-seq).

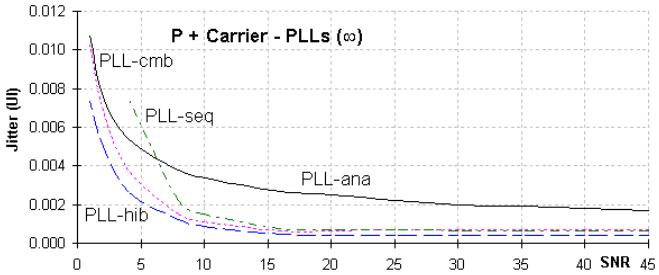

Fig.10 Jitter-SNR curves of the four P1+PLLs (P-a, P-h, P-c, P-s)

We observe that, generally, the output jitter diminishes almost exponentially with the input SNR increasing.

For the prefilter with B1= ∞, we verify that, for high SNR, the carrier PLL without input limiter (PLL-ana) is disadvantageous over the others with input limiter (PLL-hib, PLL-cmb, PLL-seq). However, for low SNR, the carrier PLL with phase comparator with intern memory (PLL-seq) is slightly disadvantageous over the others with phase comparator without intern memory (PLL-ana, PLL-hib, PLL -cmb). This disadvantage can be minimized with a prefilter.

Fig.11 shows the jitter-SNR curves of the prefilter bandwidth B2= 2.tx, with the four carrier PLLs: analog (PLL-ana), hybrid (PLL-hib), combinational (PLL-cmb) and sequential (PLL-seq).

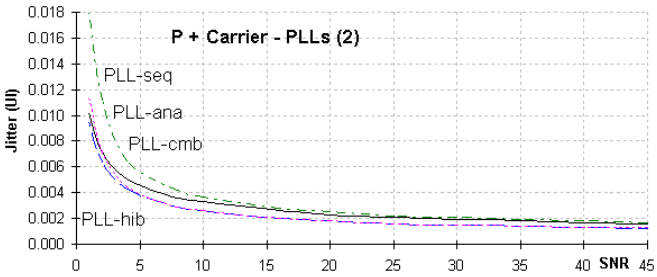

Fig.11 Jitter-SNR curves of the four P2+PLLs (P-a, P-h, P-c, P-s)

We verify that, the prefilter bandwidth B2 = 2.tx becomes the four synchronizer jitter-SNR curves more similar one another.

Fig.12 shows the jitter-SNR curves of the prefilter bandwidth B2= 2.tx, with the four carrier PLLs: analog (PLL-ana), hybrid (PLL-hib), combinational (PLL-cmb) and sequential (PLL-seq).

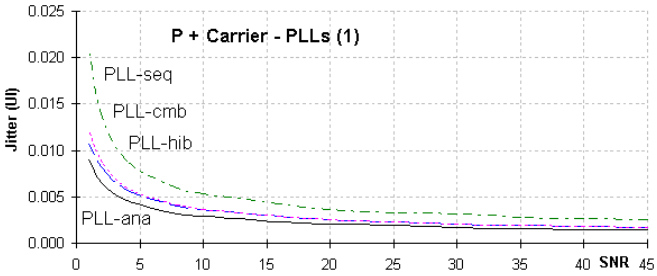

Fig.12 Jitter-SNR curves of the four P3+PLLs (P-a, P-h, P-c, P-s)

We note that, the prefilter bandwodth B3 = 1.tx becomes the four synchronizer jitter-SNR curves still more similar between them.

V. CONCLUSIONS AND FUTURE WORK

We studied the prefilter of three bandwidths (B1= ∞, B2=2.tx, B3=1.tx) applied before the four carrier synchronizers (PLL-ana, PLL-hib, PLL-cmb, PLL-seq).

We noted that, in general, the output jitter decreases almost exponentially with the input SNR increasing.

For the prefilter B1=∞ (greater), we verified that, for high SNR, the carrier PLL without input limiter (PLL-ana) is disadvantageous in relation to the others with input limiter (PLL-hib, PLL-cmb, PLL-seq). This is comprehensible since the digital limiter noise margin ignores low noise spikes. However, for low SNR, the carrier PLL with phase comparator with intern memory (PLL-seq) is disadvantageous over the others with phase comparator without intern memory (PLL-ana, PLL-hib, PLL-cmb). This is comprehensible since the high noise spikes provokes commutations to the error states that contributes to the jitter. Anyway, this disadvantage can be minimized with a prefilter.

For the prefilter B2=2.tx (medium), the four synchronizer jitter - SNR curves becomes more similar one another.

For the prefilter B3=1.tx (lesser), the four synchronizer jitter - SNR curves becomes still more similar to each other. Then, the prefilter tends to approximate the synchronizers jitter-SNR curves. So, the prefilter is prejudicial for high SNR and beneficial for low SNR.

In the future, we are planning to study the effects of the prefilter in other synchronizers types.

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