Carrier Phase Synchronizers

Antonio D. Reis, Jose F. Rocha, Atilio S. Gameiro and Jose P. Carvalho

***Abstract*— This work studies four carrier phase synchronizers (CPS) or carrier Phase Lock Loop (CPLL). The synchronizers are based in a loop with VCO (Voltage Controlled Oscillator) that synchronizes the output feedback with the input. We consider four carrier synchronizers namely the analog, hybrid, combinational and sequential. The difference between them is in the phase comparator. The main objective is to study the synchronizers output jitter UIRMS (Unit Interval Root Mean Square) versus input SNR (Signal to Noise Ratio).**

***Index Terms*—Synchronism, Digital Communications**

I. INTRODUCTION

The carrier phase synchronizer (CPS) is a Phase Lock Loop (PLL) with a particular phase comparator prepared to synchronize with input carrier signals [1, 2, 3, 4, 5, 6, 7, 8].

The PLL synchronizes its VCO directly with an input carrier signal [9, 10, 11, 12, 13, 14, 15, 16].

The PLL is a feedback device based in a phase comparator, a filter and a local oscillator VCO. The main input and VCO feedback enter the phase comparator. The phase error forces the VCO to follow the input carrier.

So, the receiver VCO input is the band base signal that firstly modulated the transmitted emitter VCO carrier.

This work studies four carrier phase synchronizers namely the analog, hybrid, combinational and sequential. The difference between them is only in the phase comparator since the other blocks are equals. Fig.1 shows the general blocks diagram of the carrier phase synchronizers.

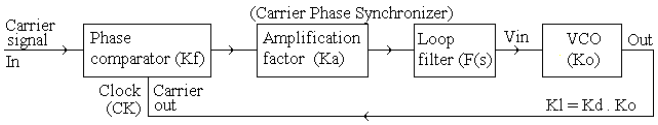

Fig.1 Configuration of the carrier phase synchronizer

Kf is the phase comparator gain, F(s) is the loop filter, Ko is the VCO gain and Ka is the loop amplification that controls the root locus and hence, the loop desired characteristics.

In prior and actual art-state was developed various synchronizers, now is necessary to know their performance.

The motivation of this work is to create new synchronizers and to evaluate their performance.

Following, we present the four carrier PLLs, namely the analog, the hybrid, the combinational and the sequential.

After, we present the project and tests. Then, we present the results. Finally, we present the conclusions.

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II. FOUR CARRIER PLLs

We present the four carrier PLLs, namely the analog, the hybrid, the combinational and the sequential. The difference between them is in the phase comparator [2].

A. Analog carrier PLL (PLL-ana)

The phase comparator of this carrier PLL is based on the ideal multiplier (analog component) (Fig.2).

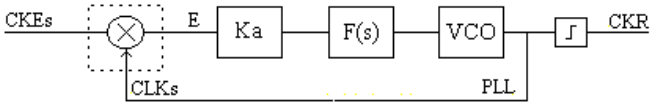

Fig.2 Fig.2 Analog carrier PLL (PLL-ana)

The phase comparator inputs (main input and VCO output feedback) are both analog.

Following Fig.3 shows the operation mode of the analog carrier PLL.

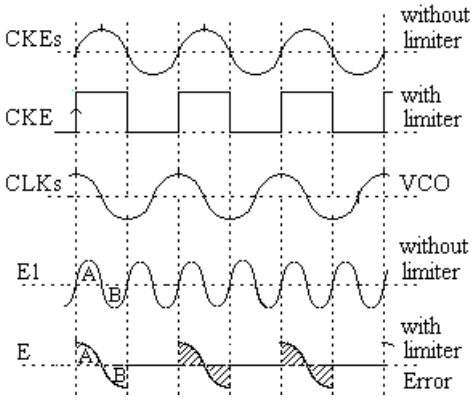

Fig.3 Waveforms of the analog carrier PLL (PLL-ana)

The output wave CLKs synchronizes in quadrature (90º) with the input wave CKEs. In phase (0º) the error signal E=1, in phase opposition (180º) E=-1 and in quadrature (90º) E=0. If the VCO frequency fVCO diminishes, tends to stay in phase (A>B) then fVCO increases and goes to the equilibrium point.

B. Hybrid carrier PLL (PLL-hib)

The phase comparator of this carrier PLL is based on the switch or real multiplier (hybrid component) (Fig.4).

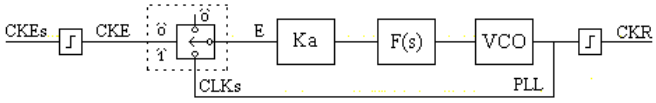

Fig.4 Hybrid carrier PLL (PLL-hib)

The phase comparator main input is now digital, but the input coming from the VCO output feedback is still analog.

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Following Fig.5 shows the operation mode of the hybrid carrier PLL.

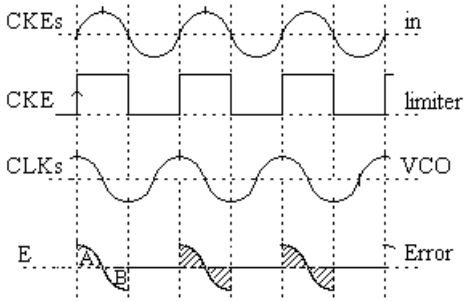

Fig.5 Waveforms of the hybrid carrier PLL (PLL-hib)

The output wave CLKs synchronizes in quadrature (90º) with the input wave CKE. In phase, the error signal E=1, in phase opposition E=-1 and in quadrature E=0. If the VCO frequency f_{VCO} diminishes, tends to stay in phase (A>B) then f_{VCO} increases and goes to the equilibrium point.

C. Combinational carrier PLL (PLL-cmb)

The phase comparator of this carrier PLL is based on the exor gate (combinational component) (Fig.6).

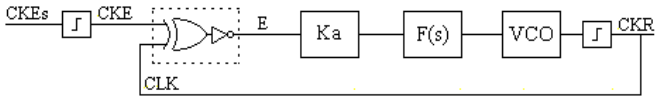

Fig.6 Combinational carrier PLL (PLL-cmb)

The phase comparator inputs (main input and VCO output feedback) are both digital. The output is only function of the inputs.

Following Fig.7 shows the operation mode of the combinational carrier PLL.

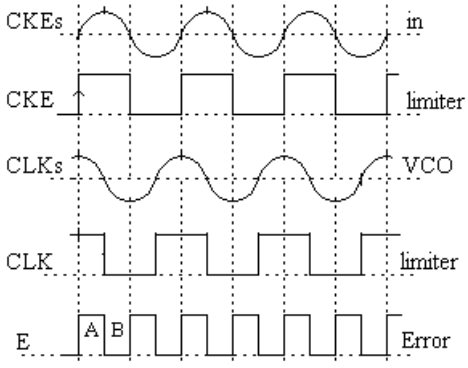

Fig.7 Waveforms of the combinational carrier PLL (PLL-cmb)

The output wave CLK synchronizes in quadrature (90º) with the input wave CKE. In phase, the error signal E=1, in phase opposition E=0 and in quadrature E=0.5. If the VCO frequency f_{VCO} diminishes, tends to stay in phase (A>B) then f_{VCO} increases and goes to the equilibrium point.

D. Sequential carrier PLL (PLL-seq)

The phase comparator of this carrier PLL is based on the flip flop (sequential component) (Fig.8).

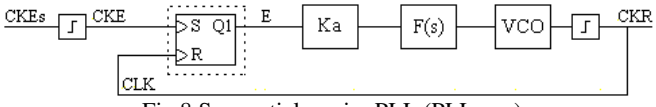

Fig.8 Sequential carrier PLL (PLL-seq)

The phase comparator inputs (main input and VCO output feedback) are both digital. The output is function of the inputs and phase comparator state (circuit with memory).

Following Fig.9 shows the operation mode of the sequential carrier PLL.

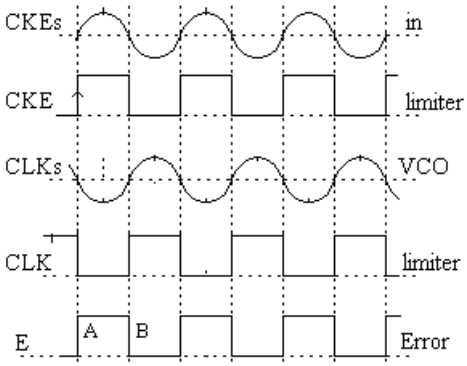

Fig.9 Waveforms of the sequential carrier PLL (PLL-seq)

The output wave CLK synchronizes in phase opposition (180º) with the input wave CKE. In phase (0^+), the error signal E=1, in phase (0^-) E=0 and in phase opposition (180º) E=0.5. If the VCO frequency f_{VCO} diminishes, tends to stay in phase (A>B) then f_{VCO} increases and goes to the equilibrium point.

III. PROJECT, TESTS AND RESULTS

We present the project, the tests and the results of the referred synchronizers [5].

A. Project

We project all the synchronizers with the same loop gain conditions to have guaranteed results. The loop gain is Kl = Ka.Kf.Ko, where Kf and Ko are fixed. Ka is the variable parameter that controls the roots and loop characteristics.

To facilitate the analysis, we use normalized values for the bit rate tx= 1baud, clock frequency fCK=1Hz, extern noise bandwidth Bn=5Hz and loop noise bandwidth Bl=0.02Hz.

We apply a power signal $Ps= A^2_{ef}$ with power noise $Pn= No.Bn= 2\sigma n^2.\Delta\tau.Bn$, where σn is the noise standard deviation and $\Delta\tau = 1/fSamp$ is the sampling period.

Then, the SNR is related with the noise variance σn^2

$SNR= Ps/Pn= A^2_{ef}/(No.Bn)= 0.5^2/(2\sigma n^2 * 10^{-3} * 5)= 25/\sigma n^2$ (1)

Now, for each synchronizer, we must measure the output jitter UIRMS versus input SNR.

- 1st order loop:

The loop filter F(s)=1 has cutoff 0.5Hz, which is 25 times greater than Bl= 0.02Hz, it eliminates the high frequency but maintains the loop characteristics. The transfer function is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKoF(s)}{s+KdKoF(s)}=\frac{KdKo}{s+KdKo} \quad (2)$$

the loop noise bandwidth is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (3)$$

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So, with (Km=1, A=1/2, B=1/2, Ko=2π) and loop bandwidth Bl=0.02, we obtain respectively the Ka, for analog, hybrid, combinational and sequential synchronizers, then

$$Bl=(Ka.Kf.Ko)/4 = (Ka.Km.A.B.Ko)/4 \rightarrow Ka_a=0.08*2/\pi \quad (4)$$
$$Bl=(Ka.Kf.Ko)/4 = (Ka.Km.A.B.Ko)/4 \rightarrow Ka_h=0.08*2.2/\pi \quad (5)$$
$$Bl=(Ka.Kf.Ko)/4 = (Ka*1/\pi*2\pi)/4 \rightarrow Ka_c=0.04 \quad (6)$$
$$Bl=(Ka.Kf.Ko)/4 = (Ka*1/2\pi*2\pi)/4 \rightarrow Ka_s=0.08 \quad (7)$$

For the analog PLL, the jitter formula is

$$\sigma_\phi^2=Bl.No/Aef^2=0.02*10^{-3}*2\sigma n^2/0.5^2=16*10^{-5}.\sigma n^2 \quad (8)$$

For the others PLLs, the jitter formula is more complicated.

- 2nd order loop:

It is not used here, but provides similar results.

B. Tests

We used the following setup to test the various synchronizers (Fig.10).

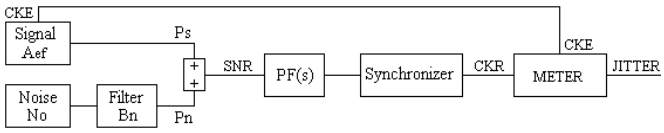

Fig.10 Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock without jitter, the difference is the jitter of the received clock.

C. Jitter measurer (Meter)

The jitter measurer (Meter) consists of a RS flip flop, which compares the receiver clock random phase (CKR) with the emitter clock fixed phase (CKE). This relative random phase variation is the recovered clock jitter (Fig.11).

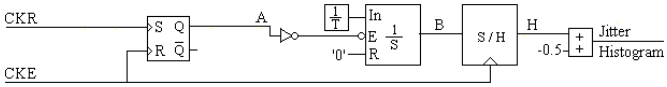

Fig.11 The jitter measurer (Meter)

The other blocks (reset integrator and sampler) convert this random phase variation into a random amplitude variation, which is the jitter histogram.

Fig.12 illustrates the operation of the jitter measurer.

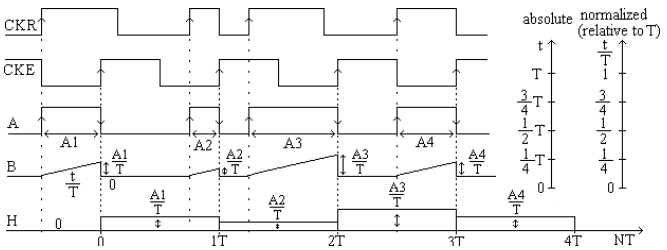

Fig.12 Waveforms at the jitter measurer

Then, the jitter histogram is sampled and processed by an appropriate program, providing the RMS jitter and the peak to peak jitter.

D. Results

We present the results in terms of output jitter UIRMS versus input SNR. Fig.13 shows the jitter-SNR curves of the four carrier PLLs: analog carrier PLL (PLL-ana), hybrid carrier PLL (PLL-hib), combinational carrier PLL (PLL-cmb), sequential carrier PLL (PLL-seq).

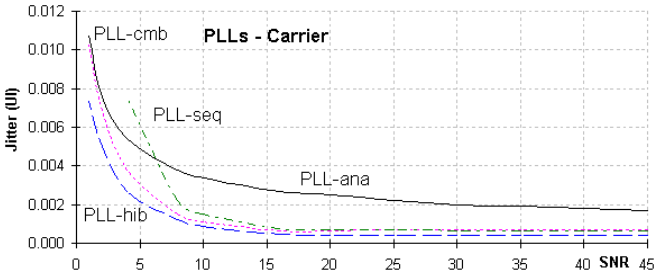

Fig.13 Jitter-SNR curves of the four PLLs (P-a, P-h, P-c, P-s)

We observe that, generally, the output jitter decreases almost exponentially with the input SNR increasing.

We verify that, for high SNR, the carrier PLL without input limiter (PLL-ana) is disadvantageous over the others with input limiter (PLL-hib, PLL-cmb, PLL-seq). However, for low SNR, the carrier PLL with intern memory in its phase comparator (PLL-seq) is slightly disadvantageous over the others without intern memory in its phase comparator (PLL-ana, PLL-hib, PLL-cmb). This disadvantage can be minimized with a prefilter.

IV. CONCLUSIONS

We studied four carrier PLLs, namely the analog (PLL-ana), the hybrid (PLL-hib), the combinational (PLL.cmb) and the sequential (PLL-seq).

We observed that, in general, the output jitter diminishes almost exponentially with the input SNR increasing.

We verified that, for high SNR, the carrier PLL without input limiter (PLL-ana) is disadvantageous over the others with input limiter (PLL-hib, PLL-cmb, PLL-seq). This is comprehensible since the digital limiter noise margin ignores low noise spikes. However, for low SNR, the carrier PLL with intern memory in its phase comparator (PLL-seq) becomes disadvantageous over the others without intern memory in its phase comparator (PLL-ana, PLL-hib, PLL-cmb). This is comprehensible since the high noise spikes provokes random commutations causing the error state that contributes to the jitter. Anyway, this disadvantage can be minimized with a prefilter.

These jitter-SNR observations can be useful, to choose the appropriate carrier PLL in each situation.

In the future, we are planning to extend this study to other synchronizers types.

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