

Investigation of the Effect of Varying Silicon Die Size and Thickness on a Small Outline Transistor on the Silicon Die Crack Using Finite Element Method

Hannah Erika R. Ducusin, Jennifer .J. Fabular, Richard Raymond N. Dimagiba, Manolo G. Mena

Abstract— The current trend for electronic products, especially those in telecommunications, is to be more compact. To match the demand for compact products, a size reduction of electronic product components such as the small outline transistor (SOT) is therefore needed. This work utilized the finite element method with a fracture mechanics approach to analyze the effect of varying geometric parameters on the J-integral of the existing crack on the silicon die. The J-integral values obtained generally showed a peak value with the mid-sized silicon die. The J-integral value generally decreased with die thickness but was found to be minimum at around 100 μm die thickness. A further reduction in thickness resulted in an increase in J-integral. Results from the simulations will be helpful in determining the effect of these parameters on the reliability of the package with respect to die crack risk and can be utilized to guide improvements on the existing package design.

Index Terms—ANSYS, die crack, j-integral, small-outline transistor

I. INTRODUCTION

SEMICONDUCTORS are one of the essential parts in electronic devices. These have three major applications namely, telecommunications, automotive and mobile systems [1]. The miniaturization trend in these devices will also mean a change in the size of the components inside them. Fundamental building blocks such as the small outline diodes (SOD) and small outline transistor (SOT) also shrink together with these devices. Consequently, parts of the SOD or SOT such as the dies should also become smaller and thinner in order to fit in a smaller area.

The silicon die is brittle and is prone to rapid propagation of fracture [2]. Loads applied to it may cause stresses that could result in cracks and, in more severe cases, fracture.

Hannah Erika R. Ducusin, M.Sc. is an Assistant Professor of the Department of Mechanical Engineering, University of the Philippines Diliman (corresponding author, e-mail: hrducusin@up.edu.ph).

Jennifer J. Fabular, M.Sc. is an Assistant Professor of the Department of Mechanical Engineering, University of the Philippines Diliman (e-mail: jjfabular@up.edu.ph).

Richard Raymond N. Dimagiba, PhD is a Senior Lecturer of the Department of Mechanical Engineering, University of the Philippines Diliman. (e-mail: dimagiba@gmail.com).

Manolo G. Mena, PhD is a Full Professor of the Department of Mining, Metallurgical, and Materials Engineering, University of the Philippines Diliman (e-mail: manolo.mena@coe.upd.edu.ph).

At the early stage of the SOD or SOT assembly, possible location of maximum stresses should be determined to monitor the state of the component as they undergo the assembly process. This may help in avoiding die cracking that may lead to failure on the package components.

Due to the small components, however, manufacturers of microelectronic devices have difficulty setting up physical experiments and testing certain parameters on the package to ensure reliability. Finite element analysis therefore becomes very useful since it can simulate conditions for the analysis of packages even with its small size.

In this study, the aim is to utilize Finite Element Analysis to investigate the effect of die size and thickness on the induced stress and crack response under thermal loading. A fracture mechanics approach was used to evaluate the propensity of the crack to propagate.

The aim is to determine which geometric parameter combination in the small outline transistor (SOT) will give the lowest risk of crack propagation.

II. METHODOLOGY

A. Model Description

Electronic packages such as SOT are composed of different materials. It usually consists of the leadframe, silicon die, wires, solder for the attachment of components and the encapsulant (Fig. 1). In this study, however, only the leadframe, solder and silicon die, as seen on Fig. 2, were utilized in the simulation since the focus will be on the cooling after the die attach process.

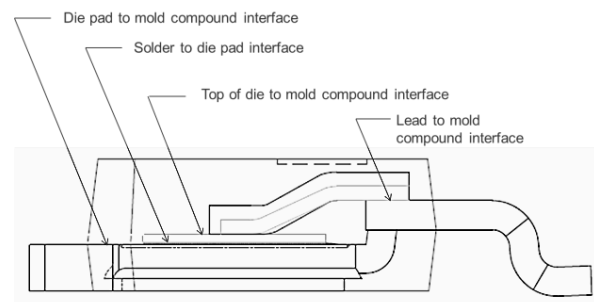


Fig. 1: 2D model of a wire-bonded SOT package.



Fig. 2: 3D Model of the SOT package used in the simulation.

A study on packaging assembly shows that during the process of die attachment the temperatures that the package may experience ranges from 260°C to 345°C [3]. During the aluminum wire bonding process, according to Pan and Freud [4], temperature can range from room temperature to 220 °C. The molding and the curing of the epoxy molding compound used on the package happens at a temperature of 175°C [5]. At the temperature ranges given by the studies, the die attach process has the highest temperature requirement among all other process that a package goes through. Processes occurring after the die attach can therefore be neglected since stresses that will be obtained from them will be less than the stresses after the die attach process.

B. Model Generation

A 3D model of the wire bonded SOT package was generated using Creo Parametric 2.0. This is composed only of three components – the leadframe, solder and silicon as illustrated in Fig. 2. Other components such as the wires and the mold compound were not modeled since they will not be necessary for the simulation, as mentioned.

Six assemblies were generated for the simulation. Each one was varying in die and solder sizes while maintaining the aspect ratio (L/W) at 0.8. In addition to the size change of the silicon die, thickness of the silicon die was changed, as well. The thickness of the silicon was changed from 200µm to 100µm. Table 1 shows the dimensions of the silicon die used for the simulations.

Dimensions of other components in the SOT package, such as the leadframe’s thickness of 0.8mm and the solder’s thickness equal to 0.03mm, remained the same.

TABLE I
SILICON DIE DIMENSIONS

Assembly	Length (mm)	Width (mm)	Aspect Ratio	Thickness (µm)
Assembly 1	3.2	4.0	0.8	200
	3.2	4.0		100
Assembly 2	2.2	2.7	0.8	200
	2.2	2.7		100
Assembly 5	1.2	1.5	0.8	200
	1.2	1.5		100

Material Assignment

The assignment of material properties is essential in order to properly simulate the behavior of the SOT package due to the thermal loads during actual package cooling. A static structural simulation was then carried out in ANSYS Workbench 16.0 after the model was imported to it to determine the stresses induced on the package. All components were modeled as isotropic elastic materials. Both thermal and mechanical properties of each material used in the package are listed in Table 2.

Boundary Condition

The boundary conditions are necessary to properly constrain the model. Supports assigned to the model represent the condition of the package on actual circumstance. The boundary conditions used for the package include one fixed support and three displacements assigned to different corners in the leadframe to restrict them from moving in the x or y or z directions.

Mesh Density Study

When assigning the number of elements in a mesh density, it is desired to have sufficient refinement without compromising computing time. A fine mesh is generally used since, in theory, it can give the best approximation of the solution.

TABLE 2
MATERIAL PROPERTIES

Material	Young's Modulus (GPa)	Poisson's ratio (-)	CTE (1E-6/K)	Density (g/cm ³)	Liquidus Temperature (°C)	Solidus Temperature (°C)
Copper Leadframe	120	0.35	17.7	8.9		
Die	169	0.23	1.00 (-100C) 2.35 (0C) 3.10 (100C) 3.50 (200C)	2.33		
Die Attach	23.33 (25 °C) 21.78 (80 °C) 20.52(125 C) 19.82 (150 C)	0.4	29	11.02	296	287

This study used the mesh refinement technique wherein meshes were done for the model, one being finer than the previous mesh. A total of three meshes were done for the whole SOT package, with 0.1mm, 0.05mm and 0.025mm element sizes for both the solder and silicon die. However, with these three meshes the maximum principal stresses were observed to have non-converging values and the location of the maximum principal stress was also observed to still be changing. A finer mesh was therefore generated until the location of the maximum principal stress became stable.

Due to the computer memory constraint, however, a body sizing of 0.025mm for the silicon die and solder on the whole SOT package was the smallest element size that can be run. A submodel was therefore necessary for the mesh refinement. The submodel consists of only the silicon die where the maximum principal stress occurs for the 0.05 and 0.025 element size. Six additional mesh refinements were done on the silicon die from 0.01875mm up to an element size 0.0125mm. The number of elements was approximated from 1 million to 4 million elements from the first refinement up to the last. Significant changes in the element size were seen but the location of the maximum principal stresses was observed to be on the same position, at the upper left corner of the silicon die, for all the finer meshes.

a. Submodel Creation

From the mesh refinement study, it was observed that as the mesh of the package is refined, the location of maximum principal stress became consistent in the upper left corner of the silicon die. A horizontal crack was induced in order to check if a failure might occur in the package. A submodel was therefore created from a portion of the silicon die. A crack was generated on the upper left corner of the silicon die, where the maximum principal stress was observed as shown in Fig. 3. The study made by Yuning Shi et al. and Calvez et al. [6], [7] found that the usual size of a crack occurring on the silicon die is 2-3 μ m. Given this crack size, a submodel was made to be large enough to fit the crack. The placement of the submodel was also essential to determine the stresses occurring in that small portion of the silicon die. The coordinate system of the submodel was very important in order to properly locate it and to have the right stresses relative to the whole model. A submodel with a 0.1mm x 0.1mm x 0.04mm dimension was then generated, positioned at the upper left corner of the silicon die and just above the solder, where the maximum principal stress occurred during the mesh refinement.

In the submodel mesh, a fine global mesh was used in order to have the right mesh for the crack model. A tetrahedron meshing method was also applied to the model in order to allow for crack generation.

b. Fracture Model

A crack was initiated on the upper left corner of the die representing the die edge defects brought about by the manufacturing of dice as seen on Fig. 4. The initiated crack and the corners in the bonded materials' interface present in the model causes stress singularities in the model. A simple

stress analysis will therefore not suffice, to compute for the stresses [8], [9], [10]. A fracture model was therefore necessary.

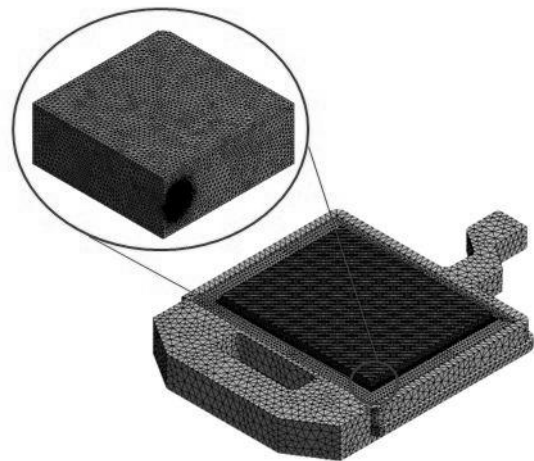


Fig. 3: Submodel

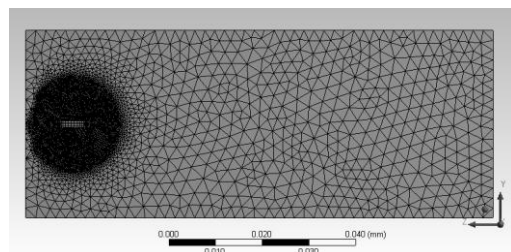


Fig. 4: Silicon die submodel

In this study, the 3 μ m crack size was used to obtain the J-integral at the extreme condition. The J-integral is a path independent failure criterion that is used for the computation of the energy flow to the crack tip to estimate the crack opening [11]. The crack generated was a semi-circular crack. The face where the crack was placed was the same as the location of the maximum principal stress obtained from the mesh refinement. The location of the crack was positioned as close to the edge of the silicon die as possible and at the middle of the silicon die thickness.

c. Thermo-mechanical Analysis

After all parameters were set, a simulation of the thermal condition of the cooling after the die attach process was applied to the whole model and the submodels. The package was made to cool down from melting temperature of the die attach material to the room temperature at 25 $^{\circ}$ C. The melting temperature of the die attach is 294 $^{\circ}$ C. This melting temperature is considered the stress free temperature. A total of 12 simulations were made to get the J-integral for each model with every change in die size and die thickness.

III. RESULTS AND DISCUSSION

The focus of this study was to evaluate the effect of the die thickness on the possibility of crack. Studies have shown that changes in these parameters greatly influence cracking on the silicon die. In this work, finite element analysis was done to obtain the J-integral of the silicon die crack with the varying die size and die thickness.

The SOT package in this study was cooled down from

the melting temperature of the solder to room temperature. The melting temperature of the solder used was 296°C. The following results were based on the cooling stage after the die attach process.

a. Maximum Principal Stress

The maximum principal stress distribution on the package after the cool down from the die attach process are presented on Fig. 5 and Fig. 6. Maximum principal stress is usually employed for brittle materials to check if it will fracture. If the maximum principal stress exceeds the ultimate tensile strength of the material, fracture will occur. Since the silicon die in the package is brittle it is important to know the maximum principal stress to asses for fracture.

The effect of the thermal loading applied to the package is presented in Fig. 5. It can be observed that the side surfaces of the die as well as the top surface of the leadframe experiences relatively higher stress compared to the other parts of the package. Looking closely at the die-solder interface in Fig. 6, the maximum principal stress occurs on the silicon die surface near the solder. Compared to the stress distribution of the whole package the stress on the side edges of the silicon die near the corners of the silicon die and solder interface was observed to be higher than the rest of the package. It was therefore necessary to check for the cracking possibility on these corners and side surfaces.

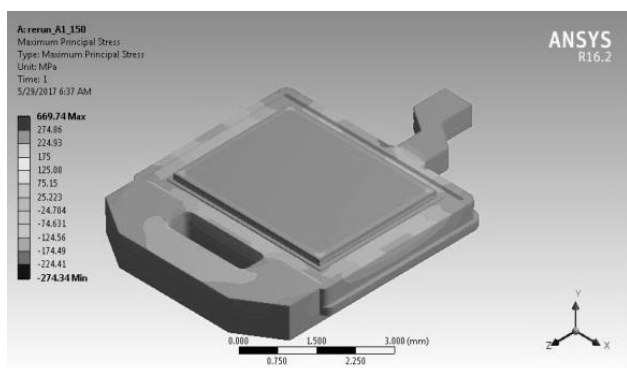


Fig. 5: Maximum principal stress on the whole package.

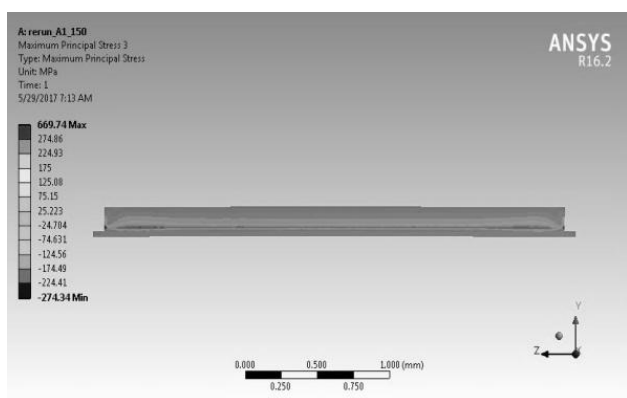


Fig. 6: Maximum principal stress on the die and solder.

b. Finite Element Simulation of Die Crack

In the previous sections, the model used to compute for the Maximum Principal Stress was assumed to be perfect materials without any flaw or defect. However, this is not the case in reality. Flaws, surface defects and cracks are

present in materials used in the package. Maximum principal stress analysis, however, does not usually consider defects.

In this study, the stresses are concentrated around the corner of the silicon die near the solder as seen on Fig. 6. Using the conventional stress analysis, the stresses around the corners of the silicon die will not converge due to the stress singularity and will not be able to get the correct solution to the problem. Fracture mechanics based method was therefore utilized. A 3µm horizontal crack initiated on the die surface near the die-solder interface was used. The crack length was found to be the usual crack size after the wafer processing according to the studies of Yuning [12] and Calvez [7]. The main objective was to get the J-integral, a fracture parameter, to check if the existing crack can propagate given the thermal conditions the package will undergo. The J-integral values were used to calculate for the stress intensity factor, K, and was then compared to the fracture toughness, Kc of the silicon die. In this section, the J-integral values obtained in the ANSYS simulation are presented. Calculation of the stress intensity factor K, using the J-integral values obtained from simulation, shows that the computed K for simulations were below the critical fracture toughness of 0.83-0.95 MPa-mm^{1/2} [13] as seen on Table 3. This indicates that in all the geometric variations, the crack will not likely propagate at the given conditions. It is still important, however, to look at the trends of the J-integral as the die size and die thickness decreases. Plots of the J-integral with respect to the die thickness and the die sizes are shown in Fig. 7 and Fig. 8.

It is noteworthy that the calculated stress intensity factor for the 200µm thick die for all the die sizes can still be considered near critical since it is almost 60% of Kc in the ideal condition. If other defects are present in the die, K could increase and the possibility of crack growth also increases.

TABLE 3
 VALUES OF J-INTEGRAL AND FRACTURE TOUGHNESS

Die Dimensions (mm)	Thickness (µm)	J-integral (mJ/mm ²)	K (MPa-mm ^{1/2})
4.0x3.2	200	0.001633	0.539757
4.0x3.2	100	0.000315	0.237136
2.75 x 2.2	200	0.001966	0.592309
2.75 x 2.2	100	0.000370	0.257028
1.5 x 1.2	200	0.001150	0.452937
1.5 x 1.2	100	0.000247	0.210016

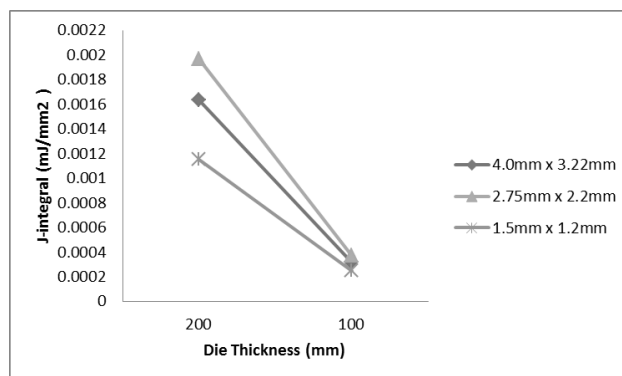


Fig. 7: J-integral vs die thickness.

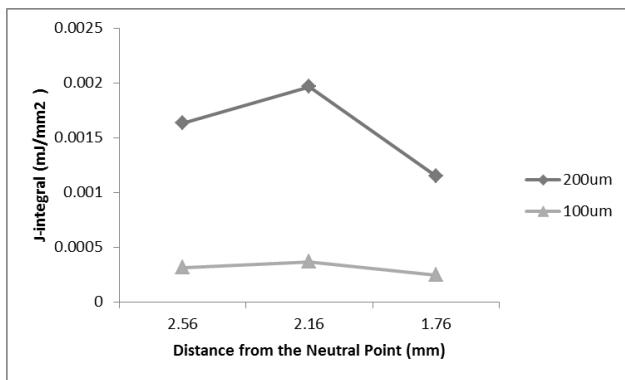


Fig. 8: J-integral vs die size

Fig. 7 shows that the thickness of the die greatly affects the behavior of the crack. The risk of crack propagation is exhibited by the value of J-integral; as the J-integral values increases, the risk of crack propagation also increases. The thicknesses considered in this study were 200µm and 100µm. As shown in Fig. 7, the J-integral is high at the 200µm thickness and low at 100µm.

Recall that the primary driving force in die crack is the CTE mismatch between the die and leadframe. This is affected by how well these two materials are bound by the solder die attach. In addition, this is also affected by how much the die or the leadframe opposes the relative contraction and expansion. A more rigid die will oppose the relative contraction more than a compliant one. Hence, the trend was that, as the die thickness decreases, J-integral also decreases. This trend was found to be similar to Chong's study [2], wherein they tested different thicknesses of silicon die for their strength using a three point bending test. Their tests show that the strength of the silicon die that is thicker will most likely fail earlier compared to thinner die. The thinner die, due to its flexibility can absorb higher stresses before failing compared to the thicker die which is more rigid.

The graph relating the J-integral to the die size is presented on Fig. 8. As observed from the plot, die size does not have significant influence on the J-integral as compared to the effect of the die thickness. It shows that die size only affects the thick die, while on thin die, there seems to be no effect. In the 200µm thick die, it can be seen that the value of the J-integral slightly decreases as the distance from the neutral point decreases or as the die size becomes smaller. The die size effect is not evident with a die thickness of 100µm.

IV. CONCLUSION

Different parameters have varying effects on the risk of crack propagation. The J-integral values obtained in all simulations shows that the initiated crack on the die is not likely to progress. The trend on how the crack behaves, however, is still essential in predicting when the crack might propagate.

The simulations show that in the die attach cooling process, high stress distribution occurs at the die surfaces near the solder. The maximum principal stress was located at one of the corners of the die at the die-solder interface. It was therefore necessary to check on that location for die

cracking.

Considering the horizontal crack on the silicon die, the J-integral was used to evaluate the risk of crack propagation of a 3µm crack. It was concluded that the optimum die thickness was at 100µm.

The behavior of the crack or the trends in the stresses obtained in this study shows that reduction in die size is not expected to greatly affect die cracking. Whereas, a reduction in die thickness is generally expected to reduce die crack risk. Therefore, it can be inferred from the study that continuous miniaturization can still be done but with careful consideration on the limits of the die thickness.

REFERENCES

- [1] A. Schubert, R. Dudek, R. Leutenbauer, R. Döring, J. Kloeser, H. Oppermann, B. Michel, H. Reichl, D. F. Baldwin, J. Qu, S. K. Sitaraman, M. Swaminathan, C. P. Wong, and R. Tummala, "Do chip size limits exist for DCA?," *IEEE Trans. Electron. Packag. Manuf.*, vol. 22, no. 4, pp. 255–263, 1999.
- [2] D. Y. R. Chong, W. E. Lee, J. H. L. Pang, T. H. Low, and B. K. Lim, "Mechanical failure strength characterization of silicon dice," *Proc. 5th Electron. Packag. Technol. Conf. EPTC 2003*, pp. 600–605, 2003.
- [3] "Semiconductor Packaging Assembly Technology," National Semiconductor Corporation, 2000. [Online]. Available: www.national.com.
- [4] J. Pan and P. Fraud, "Wire bonding challenges in Optoelectronics packaging," no. 313, pp. 1–8, 2004.
- [5] W. Van Driel, "Virtual thermo-mechanical prototyping of microelectronics devices," 2007.
- [6] Y. Shi, H. Chen, J. Wu, I. Shiu, and F. Wong, "Thermo-Mechanical Analysis and Design for SOD Package Based on Finite Element Method," vol. 2, no. 4, pp. 650–659, 2012.
- [7] D. Calvez, F. Roqueta, S. Jacques, L. Bechou, Y. Ousten, S. Ducret, D. Calvez, F. Roqueta, S. Jacques, L. Bechou, Y. Ousten, and C. Propagation, "Crack Propagation Modeling in Silicon: A Comprehensive Thermomechanical Finite-Element Model Approach for Power Devices," 2014.
- [8] L. L. Mercado and V. Sarihan, "Evaluation of Die Edge Cracking in Flip-Chip PBGA Package," *Intersoc. Conf. Therm. Thermomechanical Phenom.*, pp. 73–78, 2000.
- [9] L. Ileri and E. Madenci, "Crack Initiation and Growth in Electronic Packages," pp. 1–6, 1995.
- [10] M. A. Gonzalez, "Stress singularities and concentrations - Mesh convergence in FEA," 2015. [Online]. Available: <https://www.linkedin.com/pulse/stress-singularities-concentrations-mesh-fea-marcos-acín-gonzález>.
- [11] A. T. Zehnder, *Fracture Mechanics*. .
- [12] Y. Shi, "Thermo-mechanical Analysis and Design for Small-outline Packages (SOP) Based on Finite Element Method," no. August, 2010.
- [13] K. E. Petersen, "Silicon as Mechanical Material," *Proc. IEEE*, vol. 70, no. 5, pp. 420–456, 1982.