

# A Low-Voltage Fourth-Order Switched-Capacitor Filter with Dynamic Switching Bias OP Amps

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**Abstract**—Wideband filters employing OP Amplifiers (OP Amps) are required in sensing devices. A low-voltage 4<sup>th</sup>-order Switched-Capacitor Low-Pass Filter (SC LPF) employing 3-V power Low-Voltage Folded-Cascode CMOS OP Amps with a Dynamic Switching Bias circuit (LV DSBFC OP Amps) capable of processing video signals, which enables low power consumption and operation in wide bandwidths, is proposed. This SC LPF consists of two-stage biquadratic circuits cascading two 2<sup>nd</sup>-order SC LPFs to achieve the sufficiently sharp roll-off. In this circuit, dynamic charging operations through two-phase clock pulses during the on-state period of the OP Amps and non-charging operation during their remaining off-state period are separated. A load capacitance of the OP Amps, and a sample-hold circuit consisting of sampling switch and holding capacitor in this SC LPF, were optimized. Through SPICE simulations, it was shown that the 4<sup>th</sup>-order SC LPF with an OP Amp switching duty ratio of 50 % is able to operate at a 14.3 MHz high speed dynamic switching rate, allowing processing video signals. The roll-off response of this 4<sup>th</sup>-order SC LPF was greatly improved compared to that in the 2<sup>nd</sup>-order SC LPF. At over 5 MHz within the stop-band, a gain below -31.5 dB, which is suitable, was achieved. The power consumption of this 4<sup>th</sup>-order SC LPF reduced to 67 % of that observed in the static operation of the OP Amps, and decreased to 56.9 % of that in the 4<sup>th</sup>-order SC LPF with conventional 5-V power DSBFC OP Amps. Thus, the simulation results confirmed that the two-stage biquadratic SC LPF circuit configuration with the increased filter order of the fourth using 3-V power LV DSBFC OP Amps is useful for achieving a wide stop-band with a high attenuation and low power consumption.

**Index Terms**—switched capacitor circuit, filter, CMOS, operational amplifier, dynamic switching

## I. INTRODUCTION

WIDEBAND filters are essential for signal processing in video electronic appliances. Specifically, a wideband Low-Pass Filter (LPF) is needed in sensing devices such as a CCD camera handling a wide bandwidth video signal of over 2 MHz. The CMOS Switched Capacitor (SC) techniques suitable for realizing analog signal processing ICs, have promising use in video signal bandwidth circuits. It has been demonstrated that SC techniques using CMOS Operational Amplifiers (OP Amps) are useful for implementing analog functions such as filters [1]-[4]. However, the use of several OP Amps results in large power consumption and may cause

unstable operation. Until now, several approaches to decrease the power consumption of OP Amps have been considered, including the development of ICs that work at low power supply voltages [5], [6]. Especially, in the two-stage folded-cascode OP Amp operating at 1 V, resistive biasing and capacitive level shifter for the increase of output voltage swing are required. The requirement of four resistors for the resistive biasing makes it difficult to realize as an IC [6]. A clocked current bias scheme for folded-cascode OP Amps suitable for achieving a wide dynamic range has been typically proposed to decrease the power consumption of the OP Amp itself [7]. Because the circuit requires complicated four-phase bias-current control pulses and biasing circuits, it results in a large layout area and is not suitable for high speed operation.

Recently, the author proposed a Low-Voltage Folded-Cascode CMOS OP Amp with a Dynamic Switching Bias circuit (LV DSBFC OP Amp), of simple configuration, to provide low power consumption while maintaining high speed switching operation suitable for processing video signals and showed its practicability on a 2<sup>nd</sup>-order SC LPF [8]. However, its SC LPF has a problem of an insufficient roll-off gain characteristic. Though the availability of a 4<sup>th</sup>-order SC LPF with 5-V power DSBFC OP Amps was studied previously [9], its power dissipation was not low enough. Under the recent progress of miniaturization of equipment, the development of a practicable low-power LPF with low-voltage OP Amps is expected.

In this paper, a low-voltage 4<sup>th</sup>-order SC LPF employing LV DSBFC OP Amps with the 3-V power supply voltage, which enables lower power consumption and is suitable for achieving wide bandwidths IC due to the sufficiently sharp roll-off characteristic and low power supply voltage operation, is proposed. Its configuration under the optimization of sample-hold circuit and OP Amp load capacitance is shown in Section 2. The availability of this SC LPF for the performance of frequency response and power dissipation is evaluated in Section 3. Finally, conclusions are summarized in Section 4.

## II. LOW-VOLTAGE 4<sup>TH</sup>-ORDER SC LPF DESIGN

As a low-voltage 4<sup>th</sup>-order SC LPF, an IIR (Infinite Impulse Response) SC LPF with the Butterworth frequency characteristic employing 3-V power LV DSBFC OP Amps was designed. The high filter order of the fourth was chosen because it is expected to achieve a sharp roll-off gain characteristic. This 4<sup>th</sup>-order SC LPF was designed to achieve

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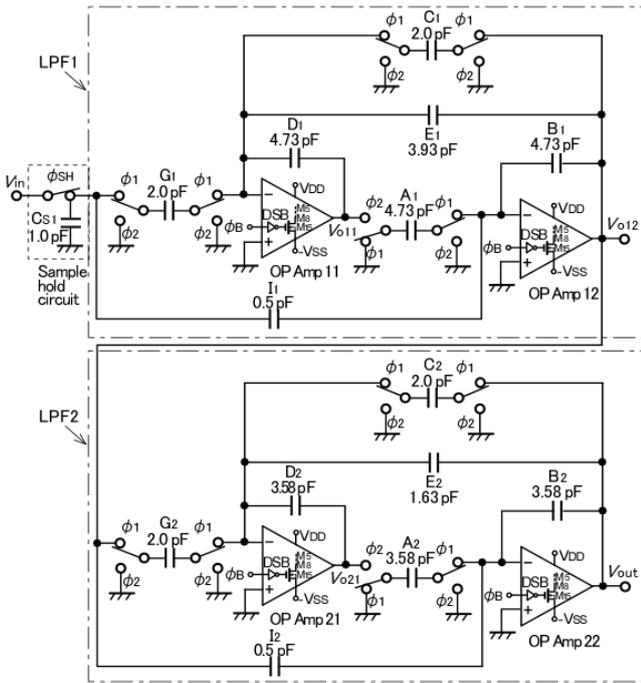


Fig. 1. Configuration of the 4<sup>th</sup>-order SC LPF.

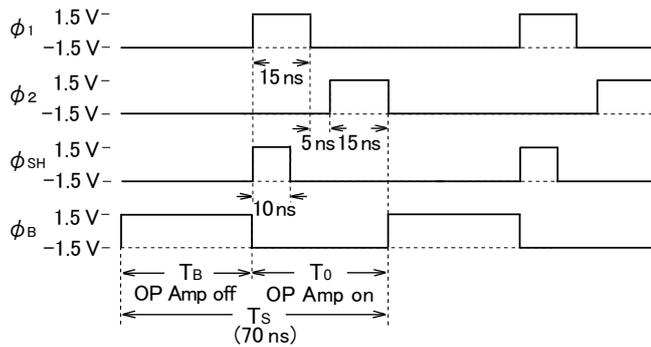


Fig. 2. Operation waveforms of the 4<sup>th</sup>-order SC LPF.

a roll-off characteristic with a gain of below -30 dB at over 4 MHz within the stop-band. The other design condition was set as follows. That is, a sampling frequency  $f_s=14.3$  MHz corresponding to four times of NTSC color subcarrier frequency 3.58 MHz and a cutoff frequency  $f_c=2$  MHz were chosen for this SC LPF, that enable it to process video signals. Under such condition, the theoretical Butterworth discrete-time transfer function obtained by bilinear transformation from s-region to z-region is given using the z-transform by (1).

$$H(z) = \frac{-0.10573(1+z^{-1})^2}{1-0.74578z^{-1}+0.16869z^{-2}} \cdot \frac{-0.13976(1+z^{-1})^2}{1-0.98582z^{-1}+0.54484z^{-2}} \quad (1)$$

This transfer function is rewritten as follows.

$$H(z) = H_1(z) \cdot H_2(z) \quad (2)$$

That is, the theoretical transfer function  $H(z)$  is a product of two independent transfer functions representing two kinds of 2<sup>nd</sup>-order SC LPFs. This means that the 4<sup>th</sup>-order SC LPF consists of a cascade connection of two 2<sup>nd</sup>-order SC LPFs. The circuit configuration realizing this transfer function is shown in Fig. 1 [9]. Its operation waveforms are shown in Fig.

2. The 4<sup>th</sup>-order SC LPF was designed referencing a SC biquadratic circuit with integrators [10]. This SC LPF consists of two-stage biquadratic circuits cascading two 2<sup>nd</sup>-order SC LPFs of LPF1 and LPF2, provided with a sample-hold circuit with a holding capacitor  $C_{s1}$  and a sampling switch controlled by  $\phi_{SH}$ , CMOS switches  $\phi_1$  and  $\phi_2$ , capacitors  $A_1, B_1, C_1, D_1, E_1, G_1, I_1, A_2, B_2, C_2, D_2, E_2, G_2,$  and  $I_2$ , and four LV DSBFC OP Amps (OP Amp 11, OP Amp 12, OP Amp 21, and OP Amp 22). The power supply voltage of  $V_{DD}$  and  $V_{SS}$  is equal to 1.5 V. The transfer function of this SC LPF circuit is shown in (3).

$$H(z) = (-) \frac{D_1 I_1 + (A_1 G_1 - 2D_1 I_1)z^{-1} + D_1 I_1 z^{-2}}{D_1 B_1 + (A_1 C_1 + A_1 E_1 - 2D_1 B_1)z^{-1} + (D_1 B_1 - A_1 E_1)z^{-2}} \cdot (-) \frac{D_2 I_2 + (A_2 G_2 - 2D_2 I_2)z^{-1} + D_2 I_2 z^{-2}}{D_2 B_2 + (A_2 C_2 + A_2 E_2 - 2D_2 B_2)z^{-1} + (D_2 B_2 - A_2 E_2)z^{-2}} \quad (3)$$

In determining each capacitance of LPF1 ( $A_1, B_1, C_1, D_1, E_1, G_1,$  and  $I_1$ ) and LPF2 ( $A_2, B_2, C_2, D_2, E_2, G_2,$  and  $I_2$ ), the correspondence between the theoretical Butterworth discrete-time transfer function  $H(z)$  and the transfer function of SC LPF circuit is needed. As shown in (1) and (2), each transfer function for the LPF1 and LPF2 is independent of each other. Therefore, the normalization of the coefficients in the LPF1 and LPF2 can be made independently. In Fig. 1, when the coefficients of  $A_1, B_1, D_1, A_2, B_2,$  and  $D_2$  are normalized to 1, other coefficients are determined as follows considering that the transfer function (3) is equal to (1).

$$I_1=K_1=0.10573, G_1=4K_1=0.42292, C_1=1+b_{11}+b_{12}=0.42291$$

$$E_1=1-b_{12}=0.83131, I_2=K_2=0.13976, G_2=4K_2=0.55904$$

$$C_2=1+b_{21}+b_{22}=0.55902, E_2=1-b_{22}=0.45516$$

Here,  $b_{11}=-0.74578, b_{12}=0.16869, b_{21}=-0.98582,$  and  $b_{22}=0.54484$ . When the smallest coefficients of  $I_1=0.10573$  in the LPF1 and  $I_2=0.13976$  in the LPF2 are replaced as a reference capacitance of 0.5 pF, each capacitance in the 4<sup>th</sup>-order SC LPF IC is set in proportion to the above coefficients as shown in Fig. 1.

A sample-hold circuit is also applied in this SC LPF to maintain its input signal for stabilizing. At this time, the s-region function of the transfer function (3) is multiplied by the zero-order hold function (4) due to a sample-hold effect.

$$H_s(j\omega) = \frac{\sin(\omega T_s/2)}{\omega T_s/2} \quad (4)$$

Here,  $T_s$  represents the one cycle period of sampling pulses. Therefore, when the transfer function (1) or (2) is replaced using  $z=e^{j\omega T_s}$ , the magnitude of the transfer function of the 4<sup>th</sup>-order SC LPF considering the sample-hold effect is given by (5).

$$|H(j\omega)| = \frac{\sin(\omega T_s/2)}{\omega T_s/2} \cdot |H_1(j\omega)| \cdot |H_2(j\omega)| \quad (5)$$

Here,  $|H_1(j\omega)|$  and  $|H_2(j\omega)|$  in (5) are the following functions, respectively.

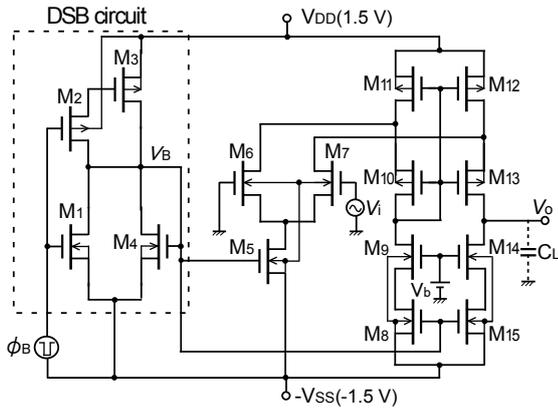


Fig. 3. Configuration of the low-voltage DSBFC OP Amp.

TABLE I  
TYPICAL PERFORMANCES OF 3-V POWER DSBFC OP AMP.  $C_L=1$  pF

Performance parameters	3-V power DSBFC OP Amp
Power supply voltages	$\pm 1.5$ V
Switching frequency $f_s$	14.3 MHz
Open loop gain $A_o$	47.1 dB
Phase margin $\theta$	32.8 degrees
Unity gain frequency $f_u$	603.7 MHz
Slew rate SR ( $C_L=10$ pF)	131 V/ $\mu$ s
Settling time $t_s$	10 ns
Distortion THD ( $f_{in}=10$ kHz, $V_o=0.6$ Vp-p)	0.73%
Power dissipation ( $C_L=5$ pF) at 50 % switching duty ratio	9.3 mW

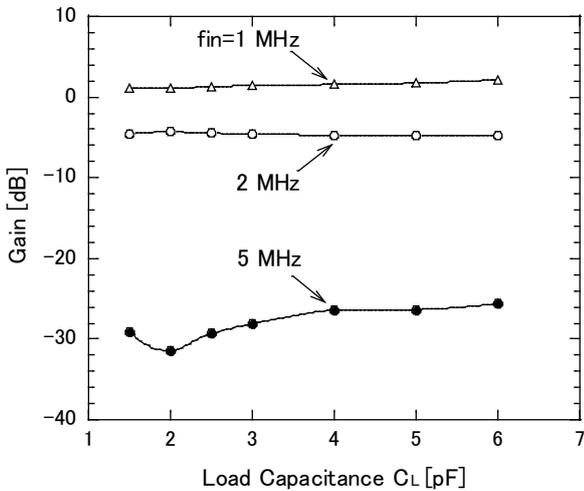
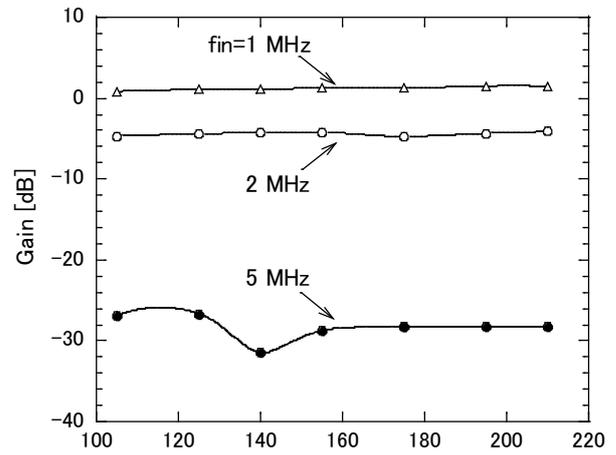


Fig. 4. Gain vs. load capacitance of the LV DSBFC OP Amp.

$$|H_1(j\omega)| = \frac{0.21146(1 + \cos(\omega T_s))}{\sqrt{1.58464 - 1.74317 \cos(\omega T_s) + 0.33738 \cos(2\omega T_s)}} \quad (6)$$

$$|H_2(j\omega)| = \frac{0.27953(1 + \cos(\omega T_s))}{\sqrt{2.26869 - 3.04587 \cos(\omega T_s) + 1.08968 \cos(2\omega T_s)}} \quad (7)$$

In the 4<sup>th</sup>-order SC LPF, a configuration of the LV DSBFC OP Amp enabling low power consumption is shown in Fig. 3. With respect to the LV DSBFC OP Amp, the same CMOS FETs channel width / channel length  $W/L$  as that in the LV DSBFC OP Amp shown in the reference [8] was employed. Typical performances of this OP Amp are shown in Table I. The load capacitance of this OP Amp was designed considering its switching speed and dynamic off swing as



Channel Width of Sampling Switch MOSFETs  $W_{sh}$  [ $\mu$ m]  
Fig. 5. Gain vs. channel width of sampling switch MOSFETs.  $C_{s1}=1$  pF.

follows. Figure 4 shows gain vs. load capacitance of the LV DSBFC OP Amp. The gain of the SC LPF became minimum at a load capacitance of the LV DSBFC OP Amps  $C_L=2$  pF. When  $C_L$  is smaller than 1.5 pF, the gain corresponding to the input signal frequency  $f_{in}=5$  MHz within the stop-band deteriorates due to the mismatch of top and bottom signal levels of dynamic off swing. On the contrary, when  $C_L$  is larger than 2.5 pF, the gain deteriorates due to the slow switching speed of OP Amps. That is,  $C_L$  in the 4<sup>th</sup>-order SC LPF is optimized to 2 pF.

The sample-hold circuit in this SC LPF was designed as follows considering the feed-through phenomenon. Figure 5 shows gain of the 4<sup>th</sup>-order SC LPF in the DSB mode of the LV DSBFC OP Amp vs. channel width  $W_{sh}$  of each of p- and n-MOSFETs in the sampling switch. The gain of the 4<sup>th</sup>-order SC LPF showed a minimum value at a  $W_{sh}$  of nearly 140  $\mu$ m when  $f_{in}$  is equal to 5 MHz within the stop-band, while its gain remains almost unchanged for  $f_{in}$  of 1 and 2 MHz within the passband. When  $W_{sh}$  is larger than 140  $\mu$ m, the feed-through caused by the difference of capacitive coupling between gate and output terminals of the above MOSFETs does not become negligible at the off-state transition of the sampling switch and so the gain corresponding to  $f_{in}=5$  MHz increases. When  $W_{sh}$  is smaller than this value, a driving ability of the sampling switch becomes insufficient, which brings about an increase of the gain. Like this,  $W_{sh}$  of the sampling switch is optimized to 140  $\mu$ m. That is, the sampling switch was designed to  $W/L=140/2.5$  ( $\mu$ m/ $\mu$ m) for each of p- and n-MOSFETs. The feed-through in the sample-hold circuit is also dependent on a holding capacitance. Figure 6 shows gain of the 4<sup>th</sup>-order SC LPF in the DSB mode of the LV DSBFC OP Amp vs. holding capacitance. As the holding capacitance  $C_{s1}$  increases, the gain corresponding to  $f_{in}=5$  MHz in the stop-band deteriorates little by little due to the need of a long transition time for sampling. That is, we can see that a smaller capacitance is desirable as  $C_{s1}$ . So, the  $C_{s1}$  of 1 pF in this 4<sup>th</sup>-order SC LPF was also chosen.

Other CMOS switches were designed to  $W/L=75/2.5$  ( $\mu$ m/ $\mu$ m), which is the same one as that in the 2<sup>nd</sup>-order SC LPF [8]. CMOS switches are turned on and off by non-overlapping two-phase clock pulses  $\phi_1$  and  $\phi_2$ , swinging from -1.5 V to 1.5 V. These sampling and CMOS switches

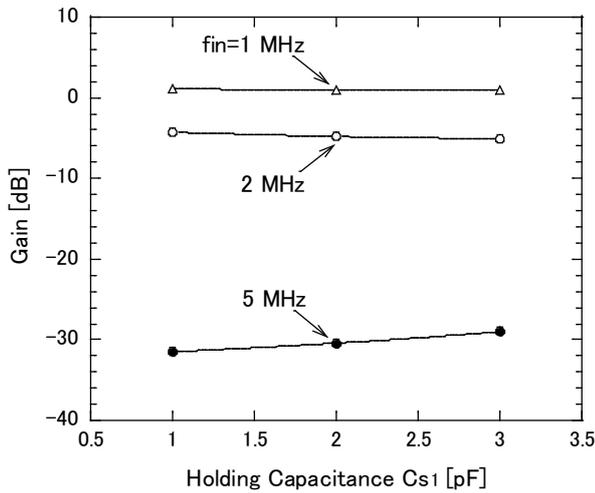


Fig. 6. Gain vs. holding capacitance. W/L of sampling switch MOSFETs=140/2.5 ( $\mu\text{m}/\mu\text{m}$ ).

were designed to have a balanced structure with each equal L and W of p-MOS and n-MOS FETs to suppress a feed-through phenomenon as much as possible. This phenomenon is easy to be caused by a capacitive coupling between gate and output terminals.

Major CMOS process parameters are given as a gate insulating film thickness  $t_{\text{ox}}=50$  nm, a p-MOSFET threshold voltage  $V_{\text{TP}}=-0.6$  V, and an n-MOSFET threshold voltage  $V_{\text{TN}}=0.6$  V.

In this SC LPF, charge transfer operations through clock pulses  $\phi_1$ ,  $\phi_2$ , are performed during the on-state period  $T_o$  of the LV DSBFC OP Amps (when the control pulse  $\phi_B$  is set at  $-1.5$  V). The off-state period  $T_B$  (the remaining period of the one cycle period  $T_s$ ) is separately provided to realize low power consumption for this SC LPF. An input signal  $V_{\text{in}}$  is sampled during the sampling phase of  $\phi_{\text{SH}}$  (10 ns) in the on-state period  $T_o$ . After sampling operation, its corresponding charge is stored on the holding capacitor  $C_{s1}$ . The voltage at the off-state transition of  $\phi_{\text{SH}}$  is transferred to an output terminal  $V_{\text{out}}$ , charging all capacitors, during the clock phase of  $\phi_1$ . During the subsequent clock phase of  $\phi_2$ , each charge of capacitors  $C_1$ ,  $C_2$ ,  $G_1$  and  $G_2$  is discharged and each charge of remaining capacitors is redistributed. During such on-state period of  $T_o$ , the LV DSBFC OP Amps turn on by setting a bias voltage of  $V_B$  at an appropriate level of nearly 0 V and operate normally as operational amplifiers.

Subsequently,  $\phi_B$  becomes 1.5 V at the off-state transition of the OP Amps, while  $\phi_2$  is switched off. During this off period  $T_B$ , the OP Amps turn off and so these do not dissipate power at all. Therefore, when  $T_B$  is set relatively long as compared to the one-cycle period  $T_s$ , the power consumption of the SC LPF is expected to become lower than that observed in ordinary static operation for an SC LPF using conventional OP Amps.

### III. SIMULATION RESULTS

Operation waveforms for an input signal of 1 MHz with an amplitude of 0.3 V and an output load of 2 pF are shown in Fig. 7. In the 4<sup>th</sup>-order SC LPF, the output signal amplitude nearly close to the input signal was also obtained for passband frequency signals. The frequency response of the

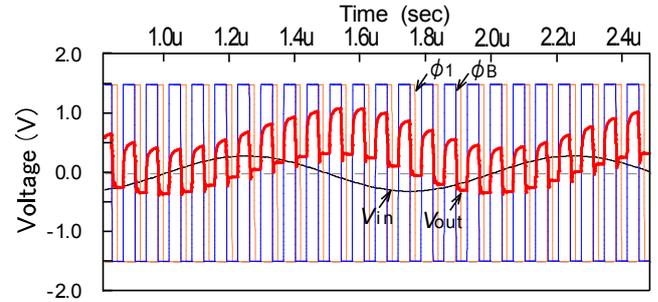


Fig. 7. Simulation waveforms for the 4<sup>th</sup>-order SC LPF.  $V_{\text{in}}=0.3 V_{\text{op}}$ ,  $f_{\text{in}}=1$  MHz,  $C_L=2$  pF.

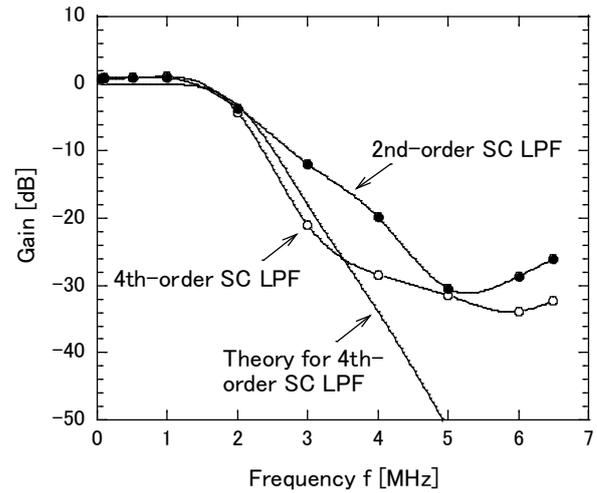


Fig. 8. Frequency response of the 4<sup>th</sup>-order and 2<sup>nd</sup>-order SC LPFs in the DSB mode of the LV DSBFC OP Amps.  $T_B=35$  ns.

4<sup>th</sup>-order SC LPF in the dynamic switching operation of the LV DSBFC OP Amps compared to that of the 2<sup>nd</sup>-order SC LPF is shown in Fig. 8. The roll-off characteristic in near 3-4 MHz was greatly improved compared to that in the 2<sup>nd</sup>-order SC LPF. The response was near the theoretical one from 100 kHz up to near 4 MHz. At 4 MHz within the stop-band, the gain below  $-28$  dB was obtained. In the high frequency range over 5 MHz within the stop-band, although it deteriorated due to a sampling phase effect, the gain below  $-31.5$  dB (a suitable level) was achieved. In this way, a wide stop-band with a high attenuation (a sharp roll-off characteristic) in the high frequency response became possible due to the two-stage biquadratic SC LPF configuration with the filter order of the fourth. Thus, it is clear that the LV DSBFC OP Amp is also applicable to the high-order SC LPF.

Power dissipation vs. OP-Amp switching duty ratio in the 4<sup>th</sup>-order SC LPF with 3-V power LV DSBFC OP Amps compared to that in the 4<sup>th</sup>-order one with conventional 5-V power DSBFC OP Amps is shown in Fig. 9. The power dissipation of the 4<sup>th</sup>-order SC LPF with the LV DSBFC OP Amps decreased in proportion to the off-state period  $T_B$  of the OP Amps. In the dynamic switching operation mode of  $T_B=35$  ns ( $=50\%$  switching duty ratio) and  $\phi_1=\phi_2=15$  ns, the power consumption of this 4<sup>th</sup>-order SC LPF (37.4mW) decreased to 66.8 % as compared to that in the static operation of the LV DSBFC OP Amps (56 mW). This value is twice as large as that in the 2<sup>nd</sup>-order SC LPF with the LV DSBFC OP Amps (18.7 mW) because the 4<sup>th</sup>-order SC LPF consists of a cascade connection of two 2<sup>nd</sup>-order SC LPFs. However, the power consumption of this 4<sup>th</sup>-order SC LPF

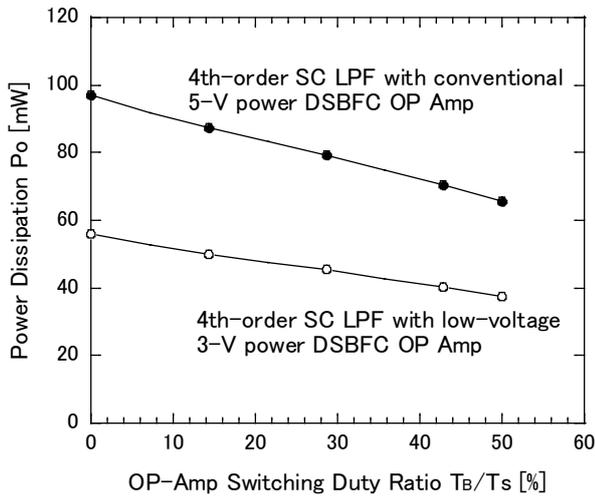


Fig. 9. Power dissipation vs. OP Amp switching duty ratio in the 4<sup>th</sup>-order SC LPFs.  $f_{in}=1$  MHz.

TABLE II  
TYPICAL PERFORMANCES FOR THE 4<sup>TH</sup>-ORDER AND 2<sup>ND</sup>-ORDER SC LPFS  
EMPLOYING THE LV DSBFC OP AMPS ( $V_{DD}=V_{SS}=1.5$  V)

Performance parameters	Simulation results	
	4th-order SC LPF - this work	2nd-order SC LPF
Sampling and switching frequency $f_s$	14.3 MHz	14.3 MHz
Input signal amplitude	0.3 V <sub>0-P</sub>	0.3 V <sub>0-P</sub>
Cutoff frequency $f_c$	2 MHz	2 MHz
Gain at a stop-band over 5 MHz	$\leq -31.5$ dB (Dynamic mode)	$\leq -26.0$ dB (Dynamic mode)
Power consumption	56.0 mW (Static)	28.0 mW (Static)
	37.4 mW (Dynamic: $T_B/T_s=50\%$ )	18.7 mW (Dynamic: $T_B/T_s=50\%$ )

with the LV DSBFC OP Amps at 50 % switching duty ratio was reduced to 56.9 % compared to that in the 4<sup>th</sup>-order SC LPF with conventional 5-V power DSBFC OP Amps (65.7 mW). Such low power characteristic was realized by the low power supply voltages and dynamic switching operation. Thus, even when the DSBFC OP Amps are applied to the two-stage biquadratic circuits of SC LPF, the dynamic operation of these LV DSBFC OP Amps enabling low power consumption as compared to their static operation is also useful for reducing the power consumption of SC LPF. Typical characteristics of the 4<sup>th</sup>-order SC LPF compared with those of the 2<sup>nd</sup>-order SC LPF employing the LV DSBFC OP Amps are listed in Table II.

#### IV. CONCLUSIONS

A low-voltage 4<sup>th</sup>-order Switched-Capacitor Low-Pass Filter (SC LPF) employing 3-V power Low-Voltage Folded-Cascode CMOS OP Amplifiers with a Dynamic Switching Bias circuit (LV DSBFC OP Amps) capable of processing video signals, which enables low power consumption and wide bandwidths operation, was proposed and its performance was evaluated. This SC LPF consists of two-stage biquadratic circuits cascading two 2<sup>nd</sup>-order SC LPFs to achieve the sufficiently sharp roll-off. In this circuit, charging operations through two-phase clock pulses during the on-state period of the OP Amps and non-charging operation during the remaining off-state period of them were separated. A load capacitance of the OP Amps, and a sample-hold circuit consisting of sampling switch and

holding capacitor in this SC LPF, were optimized. Through SPICE simulations, it was shown that the 4<sup>th</sup>-order SC LPF is able to operate at a 14.3 MHz high speed dynamic switching rate, allowing processing video signals. The roll-off response of this 4<sup>th</sup>-order SC LPF was greatly improved compared to that in the 2<sup>nd</sup>-order SC LPF. At over 5 MHz within the stop-band, a suitable level gain below -31.5 dB was achieved. The power consumption of this 4<sup>th</sup>-order SC LPF reduced to 67 % of that observed in the static operation of the OP Amps, and decreased to 56.9 % of that in the 4<sup>th</sup>-order SC LPF with conventional 5-V power DSBFC OP Amps.

Thus, it was confirmed that the SC LPF configuration with the increased filter order of the fourth and the 3-V power low-voltage DSBFC OP Amp is useful for achieving a wide stop-band with a high attenuation and low power consumption. The dynamic charging operations during the on-state period of the OP Amps and non-charging operation of them during their off-state period are also useful for high speed operation, and greatly reducing the power consumption of the SC LPF. This circuit should be useful for the realization of low-power wide-band signal processing ICs. It is also noteworthy that the performance is expected to be improved still more by employing MOSFETs with a minimum shorter channel length than 2.5  $\mu\text{m}$  used in this work.

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