`

A CMOS Under-voltage Lockout Circuit

Mohammad R. Hoque and Simon S. Ang

***Abstract*— A new configuration for a CMOS under voltage lockout (UVLO) circuit is described. This circuit consists of a pre-regulator, a hysteresis control resistor divider and an inverter pair. The UVLO circuit was fabricated using a 0.5 µm CMOS technology operating at a supply voltage of up to 5V, yielding a low quiescent current of 12 µA, an input high threshold voltage of 3.75 V and a hysteresis of 0.55 V.**

Index Terms **– *power good monitor, voltage protection circuit, UVLO.***

I. Introduction

THE rapid growth of portable consumer products has created a competitive landscape for equipment manufacturers. These manufacturers must satisfy the insatiable consumer demand for higher performance, smaller size form factors, and competitive pricing while quickly getting new and exciting products to the market well ahead of the competition. Adding to the design complexity is the convergence of these functions into one product. From the design standpoint, incorporating protection and control features into a single integrated circuit simplifies design, reduces part count, ensures reliability and conformance to industry standards, and also, meets consumer expectations for the latest technologies and features.

An important design consideration is how the system behaves in conditions when the system supply voltage, whether powered by battery or DC source, dips to levels that may cause undesired operations for other critical ICs. A control circuitry that provides under-voltage lockout (UVLO) protection to ensure protection against supply voltages that have not stabilized is helpful [1]. This simple function ensures that the switch is disabled when the input voltage is below the specified threshold. A built-in hysteresis, as the input voltage is increasing, ensures that the device does not turn off intermittently near the threshold voltage. Fig. 1 (a) shows a simple application of the UVLO circuit. As can be seen, the UVLO circuit monitors the battery voltage and changes its modes of operation accordingly. To understand how the circuit works, three different modes of operation can be considered as shown in Fig. 1(b):

M. R. Hoque, Analog Design Engineer, Portable Power Management Group, Texas Instruments Dallas TX 75002 (phone: 214-567-7471, fax: 214-480-6400, email: rashed@ti.com)

S. S. Ang, Professor, Department of Electrical Engineering, University of Arkansas, 3217 Bell Engineering Center, Fayetteville, AR 72701 (phone: 479-575-7683, fax: 479-575-7967; e-mail: siang@uark.edu).

Mode X: When the battery is charging by an external source, but not connected to the load.
Mode Y: When the battery is connected to the load.
Mode Z: When the battery is disconnected from the load.

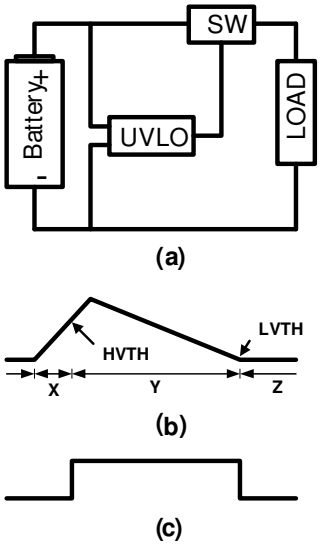

Fig. 1. (a) Application of UVLO (b) Battery voltage (c) UVLO output.

During the time of charging, the voltage at the positive terminal of the battery is rising. When it reaches a certain threshold voltage, the UVLO circuit will send a HI signal to the switch (SW) to connect the battery to the load as shown in Fig. 1(c). This threshold voltage is determined by the UVLO circuit and is known as the HI threshold (HVTH) voltage. The battery voltage will keep rising as long as the charging is progressing. Once the charging is completed, battery voltage starts to drop as its current capacity is being depleted by the load. It is important that the battery is not disconnected form the load when its voltage reaches very close to the HVTH voltage. Disconnecting the load from the battery at HVTH will increase the battery voltage instantaneously that in turn creates instability by switching the load back to the battery. Therefore, UVLO circuit should turn off the load from the battery at a different threshold voltage than the HVTH. The difference between these two thresholds is known as hysteresis of the UVLO circuit. The turn off threshold of the circuit is the difference between the HVTH and the amount of the desired hysteresis, which is known as the LO threshold voltage (LVTH).

When designing UVLO, the quiescent current requirement is

`

an important issue [2]. For example, when the low-battery mode of operation is indicated, a cell phone (or any portable device) automatically powers down after the battery-low indicator has been flashing for some time. If the phone is misplaced in this condition and found a week later, the protection circuitry may over-drain and damage the battery, because of its high quiescent current requirement.

Although UVLO is an important part of many modern electronics, not many of these circuits have been reported [2, 3]. In most of these reported designs, the UVLO circuits require a bandgap reference system to provide the bandgap voltage to set the reference voltage to the UVLO circuits. This paper presents the design of a CMOS on-chip UVLO circuit without the need of a bandgap circuit to operate the UVLO; this feature reduces the quiescent current of the system during the sleep mode.

II. Circuit Description

The complete UVLO circuit is shown in Fig. 2. The left portion of the circuit is a pre-regulator [4] circuit. The output of the regulator (Vreg) is supplied to the inverter pair. The resistor voltage divider controlled by an NMOS switch (M12) is the hysteresis controlling section which generates the input voltage to the first inverter of the inverter pair.

During mode X operation, transistor M12 will be in conduction that bypasses resistor R_A to reduce the effective resistance from node A to GND. Hence, a higher

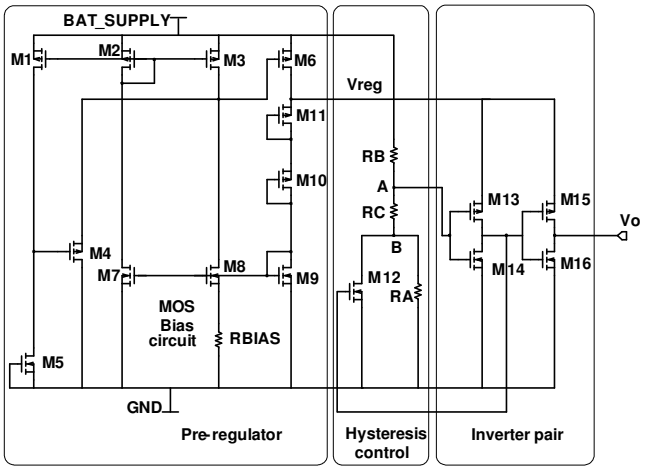

Fig. 2. Complete schematic of CMOS UVLO circuit.

BAT_SUPPLY will be required to turn 'on' transistor M14. This voltage can be considered as the HVTH. Once transistor M14 is in conduction, it switches off M12 and retains the actual resistance from node A to GND. This condition is considered as mode Y operation with the load connected to the battery, i.e., the output of the UVLO is HI as shown in Fig. 1(c). During this instant, a lower BAT_SUPPLY is required to keep transistor M14 in conduction than that during mode X operation. If we consider this voltage as LVTH, the hysteresis voltage will be the difference between these two threshold voltages. The pre-regulator is necessary in this design to properly define these threshold voltages which will be elucidated in more detail in the next section.

III. Design Methodology

This section discusses the analytical design of UVLO circuit using SPICE LEVEL1 model. The circuit is designed for the following specifications which are very common in most commercial ICs [5, 6]:

HVTH = 3.75 V,
Hysteresis = 0.55 V,
Vsupply = up to 5 V,
Quiescent Current ≤ 12 µA.

***Pre-regulator design*:**

Transistors M7, M2, M3, M6 and diode connected MOS transistors M9 through M11 are used to provide negative feedback. Transistors M8 is used as a current source for M3 and provides positive feedback to the output. The positive feedback gain is lower than the negative feedback gain because of the source resistor RBIAS [4]. Three series connected MOS diodes M9-M11 determine the output voltage of the regulator. The lowest operating voltage and output voltage of the regulator circuit should be well below the lower threshold voltage (LVTH) of the UVLO circuit to operate the hysteresis accurately. In this design, the pre-regulator is designed to operate at 2.7 V with an output voltage of 2.6 V. There is no particular restriction of these voltage selections. It depends on the LVTH and output voltage requirement of the UVLO circuit.

The CMOS bias circuit of the regulator, which is independent of the supply voltage and MOSFET threshold voltage, consists of two deliberately mismatched transistors M7 and M8, where M8 is 4 time wider than transistor M7. A resistor R_{BIAS} is connected in series with the source of transistor M8 to determine the bias current through transistors M7 and M8. If the aspect ratio (S8) of transistor M8 is 20 and the bias current is 2.5 µA, then the value of R_{BIAS} can be determined using the following equation [7]:

$$R_{BIAS} = \frac{2}{\sqrt{2\mu_n C_{ox} S_8 I_B}}\left(\sqrt{\frac{S_8}{S_7}} - 1\right) \quad (1)$$

A 2.5 µA bias current has been chosen to design the pre-regulator to satisfy the requirement for a low quiescent current. Using the process parameters supplied by the vendor, the bias resistor, R_{BIAS}, is calculated from equation (1). Since the pre-regulator is driving a pair of inverter, the load current of the regulator is approximately zero. Thus, the current flow through transistor M6 is simply the bias current I_B. Therefore, to meet the output requirement,

$$V_{SD6} \leq 0.1V$$

`

$$\sqrt{\frac{2I_B}{\mu_p C_{ox} S_6}} \le 0.1V \quad (2)$$

The three series-connected MOS diodes determine the Vreg voltage at the output. The current through these diodes is 2.5 µA, determined by transistor M9 which has a similar dimension as transistor M7. To achieve a 2.6 V at the output,

$$V_{DS9} + V_{SD10} + V_{SD11} = 2.6V \quad (3)$$

The drain/source to source/drain voltage of these transistors can be simply calculated from the following equation [9]:

$$| V_{DS} | = \sqrt{\frac{2I_B}{\mu C_{ox} S_{10}}} + | V_t | \quad (4)$$

In the pre-regulator design, no attention has been given to compensate temperature variations. To achieve a constant performance over varying temperature ranges, a temperature compensated regulator can be used [9]. However, a ± 8 % variation of the UVLO threshold is acceptable in most applications [6] as long as the required amount of hysteresis is present.

***Inverter and hysteresis logic design*:**

Inverter plays an important role in determining the threshold voltage of the UVLO circuit. The inverters are designed for a threshold voltage that is half of the Vreg voltage. There are two advantages of such design [6]:

1. The noise margin for both input high and low will be equal.
2. Their values will be maximized.

This requirement can be fulfilled by designing the inverters according to:

$$\frac{\mu_p C_{ox} S_{13}}{\mu_n C_{ox} S_{14}} = 1 \quad (5)$$

A hysteresis phenomenon can be achieved by changing the impedance at node A (input of the inverter) during mode X and mode Y operation. If the aspect ratio of transistor M12 is large enough (~10) and the current flowing through the resistors is low (~3µA), the voltage at node B is approximately 0 V when transistor M12 is in conduction, i.e., in mode X operation. However, increasing the aspect ratio of transistor M12 will introduce a delay to the output of the UVLO due to the gate capacitance of transistor M12. The designer has to make sure that this delay is within the acceptable range of operation. A plot of delay versus output capacitance is presented in the next section. During mode X, the output of the first inverter (M13 & M14) is 'HI' which switches on transistor M12. Therefore, the total resistance from supply to GND is the sum of R_B and R_C. Since the threshold voltage of the inverter is half of Vreg, to achieve an HVTH of 3.75 V, the values of R_B and R_C can be determined as follows,

$$\frac{V_{reg}}{2} = \frac{R_C}{R_B + R_C} HVTH \quad (6)$$

Once the circuit reaches mode Y operation, (i.e., the Vsupply > HVTH), the output of the first inverter (M13 & M14) is LOW, which turns 'off' the switch M12. Hence, the total resistance from the supply to GND becomes $R_A + R_B + R_C$. The resistance R_A determines the hysteresis (i.e., the difference of HVTH and LVTH). For a LVTH of 3.2 V, R_A can be calculated from the following equation.

$$\frac{V_{reg}}{2} = \frac{R_C + R_A}{R_B + R_C + R_A} LVTH \quad (7)$$

One of the important requirements of the UVLO circuit is the low quiescent current for the battery operated devices. Therefore, the pre-regulator including the start-up circuit is designed for a quiescent current of approximately 9 µA. Since the load of the regulator is a CMOS inverter pair, its power consumption is approximately 0 W. The resistor divider draws approximately 2.5 µA from the supply when the battery voltage goes below the LVTH, which is considered LO battery (mode Z operation). Hence, the total quiescent current for the complete UVLO circuit is approximately 11.5 µA at LO battery operation.

IV. Simulation and Measured Results

The UVLO circuit was fabricated using a 0.5-µm n-well CMOS process. Fig. 3 shows the die photo of the fabricated UVLO circuit. The circuit occupies approximately 0.25 mm^2, without any layout optimization. Fig. 4 shows a plot of the output voltage versus input supply voltage. As can be seen, the output of the UVLO is HI when the input supply voltage reaches the HVTH of 3.75 V. The output stays high as long as the supply voltage is above the LVTH of 3.2 V. This yields a hysteresis of 0.55V, similar to our designed value.

The AC power supply sensitivity (PSS) of UVLO output is affected by the PSS of the pre-regulator. Fig. 5 shows a plot of PSS versus frequency when the battery is connected to the load (i.e., mode Y operation). As shown, the PSS is 26 dB up to 3 kHz. Since the function of the UVLO circuit is to connect the battery to the load at the designed voltage, it should meet the PSS requirement of the load. The UVLO PSS performance can be improved by enhancing the PSS of the pre-regulator. Figure 6 shows the simulated output delay versus load capacitance. The load capacitance is the gate capacitance of the switch that connects or disconnects the battery from the load. The load drive capability of the UVLO can be improved by incorporating a buffer at the output of the circuit. The measured power dissipation of the UVLO circuit is 36 µW during mode Z operation, compared to the designed value of 34.5 µW.

`

V. Conclusion

This paper presents a new CMOS UVLO circuit for power management circuit applications. The methodology of designing the UVLO circuit has been described. The fabricated UVLO circuit yielded circuit performance similar to the designed goals.

References

[1] Design, Protection in Power Management for Portable Applications, Aug. 2005 [online] Available: http://neasia.nikkeibp.com/

[2] Li-Ion Battery Protection Circuit Draws Only 4.5 μA, Dec. 1999, [online] Available: http://www.elecdesign.com/

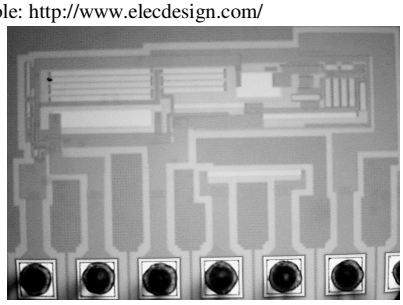

Fig. 3. Die Photograph.

[3] L. Wofford, "UC1860-new IC controls resonant mode power circuits", IEEE Applied Power Electronics Conference and Exposition, Feb. 1988, pp: 299 – 307.

[4] G. A. Rincon-Mora, Voltage References from Diodes to Precision High-Order Bandgap Circuits, p. 103-107, Wiley IEEE Press, 2001.

[5] SC338: Ultra Low Output Voltage Dual Linear FET Controller - Data sheet, Semtech Corporation, Nov. 2004.

[6] ISL6401: Synchronizing Current Mode PWM for Subscriber Line Interface Circuits- Data sheet, Intersil, April 2005.

[7] A. S. Sedra, K. C. Smith, Microelectronic Circuits, Oxford University Press, p. 957, 2004.

[8] P. E. Allen, D. R. Holberg, CMOS Analog Circuit Design, Oxford University Press, p. 125, 2002.

[9] R. J. Widlar, "New Developments in IC Voltage Regulators," IEEE Journal of Solid-State circuits, vol. sc-06, no. 1, Feb. 1971.

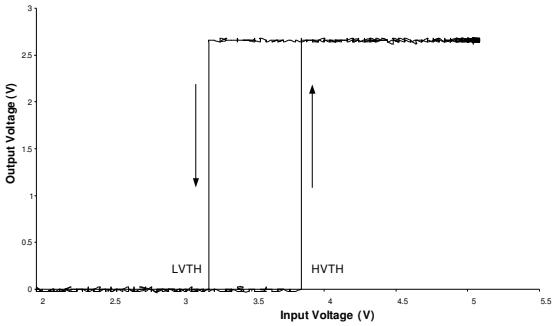

Fig. 4. Measured output of UVLO for variation of supply voltage.

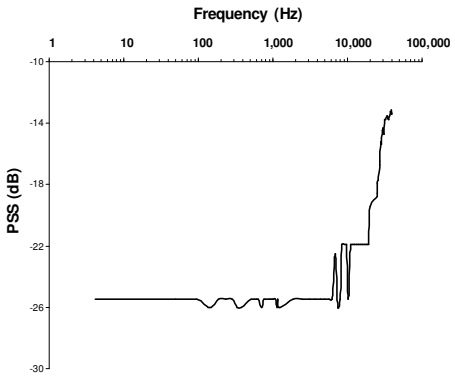

Fig. 5. Measured PSS vs. Frequency for mode Y operation.

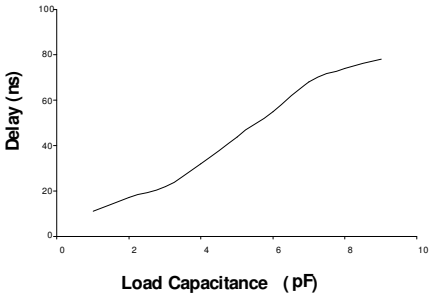

Fig. 6. Simulated output delay versus load capacitance.