On Source Couple Logic (SCL) Layout

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***Abstract*— This paper deals with the extraction of RC parasitic of SCL inverter submicron layouts. As it is known in VLSI design that the RC parasitic of any design is most crucial and affect all performance of the circuit. SCL is promising logic as it is analog friendly and consumes less power in high speed. For that, Different SCL inverters layouts have been investigated for it is effect on output voltage swing, switching noise and the area. The results show an important affect on the SCL output signals. Post-Simulation was carried out on all proposed layouts using HSPICE and using 0.35u MIMOS Berhad PDK. The layout is done using Virtuous from Cadence whereas the extraction done using Mentor Graphic - Caliber Interactive tool.**

Index Terms— Source Couple Logic (SCL), CMOS Layout, RC Parasitic in Layout, Analog Circuit Layout.

I. Introduction

The VLSI technology has been scaled down into submicron level, which allows to layout several million transistors on the chip module. Along that there are quality measures which have to be considered during layout procedure in the physical design of analog VLSI platform. Area and Performance are most crucial issue in any IC layout design. The main target for any VLSI design is to reduce the layout area as much as possible so that we can accommodate more circuits in less area. The performance of layout is key facto to the chip designs success, performance means efficiency of utilizing CMOS designing layers (minimize), efficiency of routing and connect different parts of design (short and direct), and arranging of various parts of the design [1].

As the VLSI circuit composed of several metal layers in a stratified dielectric medium over a silicon substrate, that is create a lot of capacitance effects between different metal layers for such a dense packed multiconductor system, therefore, the area has major effect of overall design efficiency. The layout performance plays an important role to reduce the effect of RC parasitic. The parasitic capacitances and inductances of interconnects are most important aspect in layout design as it is the main contributor to signal delay and it is based on geometrical structure of the layout and aspect ratio of interconnects [2].

The layouts of basic transistor or block of transistors control the amount of area used to layout the circuit, where routing and connecting different parts show the efficiency of the layout. Similarly, matching of transistors to get same characteristics is crucial in VLSI design, and it can be enhanced using layout technique. For this reasons different layouts of differential pair transistors and analog CMOS circuits is suggested by [3] to reduce the area and RC parasitic as well as ensure the matching.

Fingering is one of the layout techniques which used to layout large transistor to multiple transistors that are connected in parallel. There is an advantage with an even number of fingers: the active capacitance is reduced, because the drain region is surrounded with gate poly instead of field. Another reason to use fingering is to optimize the resistance of the gate poly along the width of the transistor. Since the gate poly is driven from one end and gate poly is resistive, there may be reason to have a guideline that states the maximum width of a single finger. Fingering multiple transistors that are connected in series is trickier because the order of connectivity of the devices must be maintained [1].

In this paper, we concerned on Source Couple Logic (SCL) layout since SCL logic style seems to be promising in both reducing power consumption and providing an analog friendly environment where desirable to integrate analog and digital circuitry onto the same die. This integration however faces difficulty in the design of high precision analog circuitry in the presence of digital noise. The low switching noise feature of SCL is obtained at the cost of static power dissipation; a required specification needs special design strategy of SCL gates, while keeping power consumption as low as possible. Moreover, power and delay are the tradeoff parameters in SCL design criteria as mentioned in [4].

In this paper, firstly, we will discuss the topology and operation of the SCL inverter, second section deals with layout of SCL inverter by different arrangements and the result of each, general discussion and overall results will be mentioned in separate section, and finally the conclusion.

II. SCL: Topology and Operation

SCL is a dual rail logic circuit that uses both the variable and its complement (A, $\bar{A}$) as an input pair. The output of a dual rail circuit is also a pair (E, $\bar{E}$) that drives the next gate(s) in the logic cascade. However, dual rail logic interprets the difference (E-$\bar{E}$) as the logic variable instead of just one or the other. When viewed at the level of Boolean algebra, the use of both variables and its complement is superfluous; the result is the same as that found using a single-rail circuit. Moreover, dual rail networks are more complicated to wire [6].

The circuit schematic of SCL inverter gate, shown in Fig. 1, is made up of an NMOS source-coupled pair having transistors working in the saturation or cut off region, that approximates well the behavior of a voltage-controlled current switch. The biasing current (I_{ss}) implemented by using current mirror technique is steered to one of the two output

Manuscript received June 26, 2006. This work was supported by the UKM and the work was done in MIMOS Berhad, Microelectronics & MEMS department.

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branches and converted into a differential output voltage by two PMOS transistor working in the linear region (Active load pull-up resistance). The logic function of the SCL is implemented by the logic block connected between the active load (PMOS) and the current source (I_{ss}). For an inverter/buffer, the logic block is the differential pair constructed by NMOS transistors M1 & M2 [5].

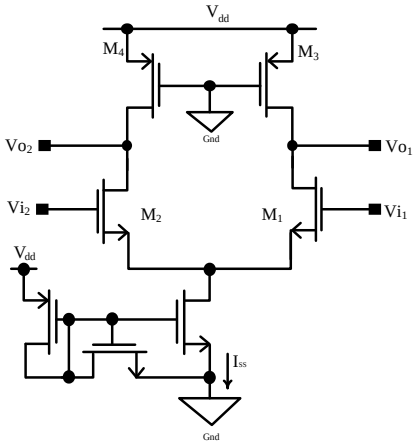

Fig. 1. SCL Inverter

The SCL gate uses PMOS active load, but other types of load, such as physical resistor or a diode-connected NMOS/PMOS can be used. However, resistor's load is not normally chosen since large silicon area needed and its parasitic capacitance can be high. For the second type of load, the output levels will lose the threshold voltage furthermore; the MOS diode load is slower than the PMOS active load for practical bias currents [5].

The operation of the SCL logic is based on the input differential pair circuit. The two inputs control the flow of current through the two branches of the differential pair. For example, if V_{GS} (M2) is higher than V_{GS} (M1), the current I_{D2} exceeds the current I_{D1}. Therefore, the output voltage V_{o2} begins to drop until it reaches steady sate, where the current going through PMOS active load (M4) matches the I_{D2}. In mean time V_{o1} is charged up to V_{dd} through M3.

The output voltage swing V_{swing} is defined as voltage difference between V_{o1} and V_{o2} at steady state. The amount of current passing through the ON branch (M2) controls the delay of the logic gate transition (1→0), while the PMOS active load (M3) controls the charging of the output nodes (0→1 transition) [5].

ΔV is defined as the voltage drop of M3 (M4) due to the drain current equal to I_{ss}, the logic swing of the gate, Vswing, equal $2\Delta V$.

To achieve best performance, all current must pass through the ON branch and the load resistance (PMOS) should be small in order to reduce the RC delay. This guarantees that the voltage is $V_{DD} - I_{ss}.R_D$, where I_{ss} is the current flowing through current source, and R_D is the PMOS equivalent linear resistance [5].

To verify that, simulation is carried out for a SCL inverter for a specific output V_{swing} (~ 1 Volt) with input dual pulses, the aspect ratio of NMOS/PMOS transistor was sited to get desired V_{swing} and according to procedure in [4]. The output V_{swing} and the input dual opposite pulse for SCL inverter circuit netlist is shown in the Fig. 2 . The steering current by current mirror source is 40uA.

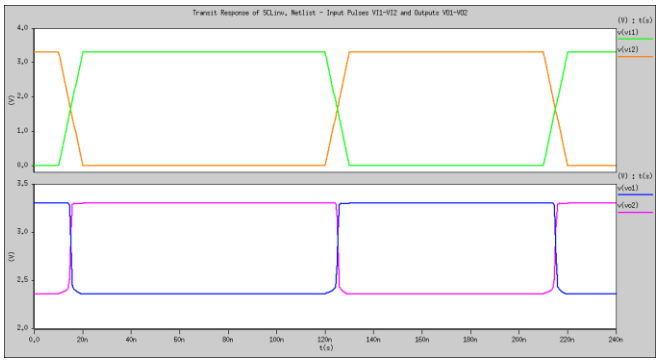

Fig. 2. The Inputs/outputs of SCL inverter netlist

III. SCL Physical Layout

As the design margins decrease steadily, the 'analogue' problems (matching, crosstalk) rises it's effect to the circuits performance. The dominance of parasitics has shifted from the vertical plan (towards GND) to the lateral one (cross) - coupling. The electrical parasitic extraction is the process of estimating or calculating the undesirable by product elements of the physical layout of a circuit. It is utilized to improve the model behavior of a circuit and to highlight the design imperfections and allows the designer to make the circuit more robust. The electrical parasitics are the sum of the electrical characteristics (resistance, inductance and capacitance) of any interconnects (Fig. 3) [6].

Those interconnects have an important contribution through their R and C components on the electrical circuit parameters such as delay, crosstalk or matching, especially in deep submicron technologies and that is why it becomes more important to take these effects into account during the IC simulations [7][8].

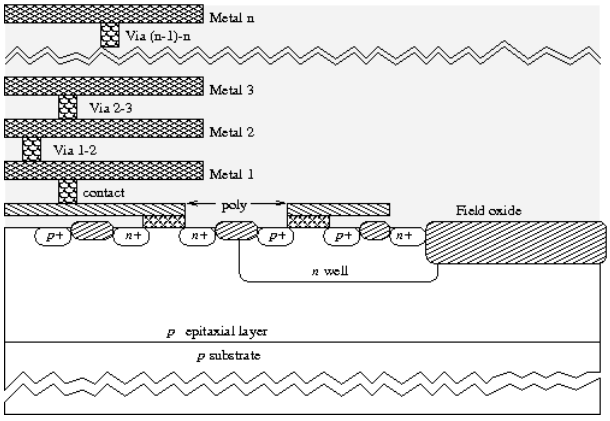

Fig. 3. Interconnection parastics capcitances among CMOS layers.

All mentioned parasitics are dependent on the way of laying out the circuit in the IC design; the way of laying out the circuit is the amount of RC parasitic added, so, therefore affecting all performance of the circuit. In the next sections different techniques of laying SCL inverter will be applied to examine the effect of RC parasitic on the output signals by employing post-simulation with input dual opposite pulses shown in fig. 2, the limits and constrains of all layouts are the design rules of the MIMOS 0.35u PDK.

A. *First Layout: Discrete*

Direct layout is applied and each transistor is laid as discrete component according to layout design rule. Whole W and L of NMOS/PMOS transistors are laid directly. The signal paths among different interconnections terminals are made directly as short as possible with minimum path width. Two metal layers are used M1 and M2 for signal paths. This layout utilizes 14 S/D interconnections. This layout is shown in the Fig. 4.

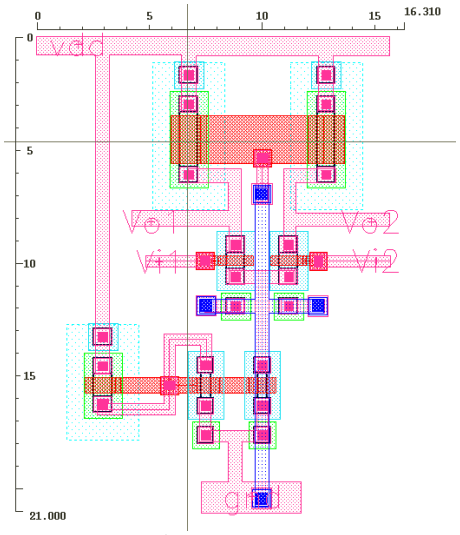

Fig. 4. 1st Layout of SCL Inverter.

B. *Second Layout: Fingering*

Fingering technique is applied to divide the W of NMOS and PMOS on two transistors connected in parallel as shown in the Fig. 5. This layout utilizes 17 S/D interconnections, and two layers M1 and M2. This layout utilizes more area than first one due of fingering.

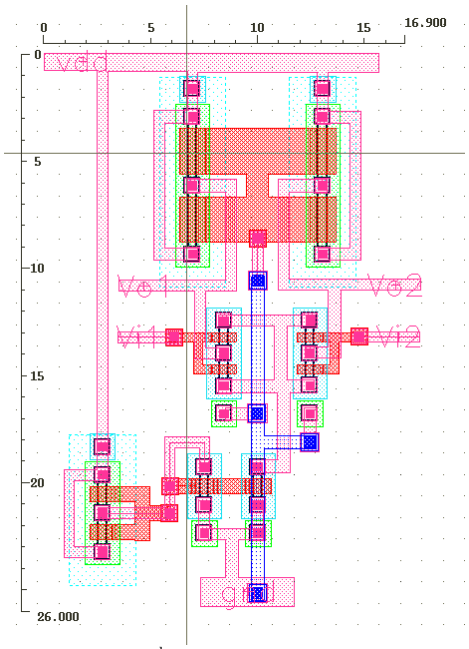

Fig. 5. 2nd Layout of the SCL inverter.

C. *Third Layout: Comb*

In this layout the NMOS and PMOS transistors are laid in a comb way, which reduces the area and drain/source interconnections, also it provides interdigitized and common centroide structure as shown in Fig. 6. This layout utilizes 11 S/D interconnections.

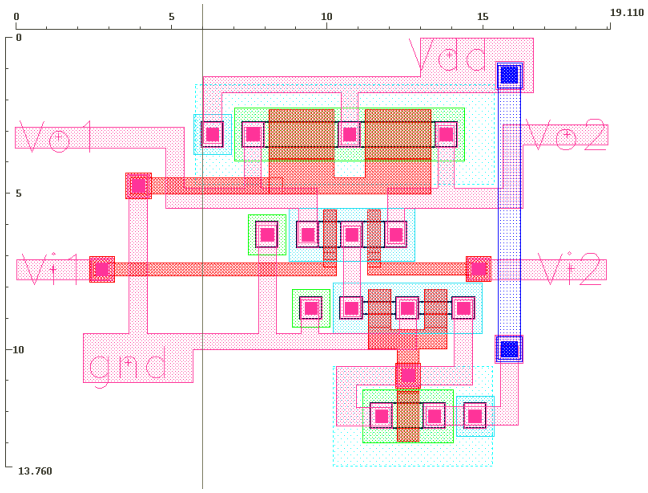

Fig. 6. Comb layout of SCL inverter.

D. *Forth Layout: Fingering and Comb*

Both, fingering and comb techniques are applied in this time as shown in the Fig. 7, and 16 S/D interconnections are used. Comparing with third layout, area is increased.

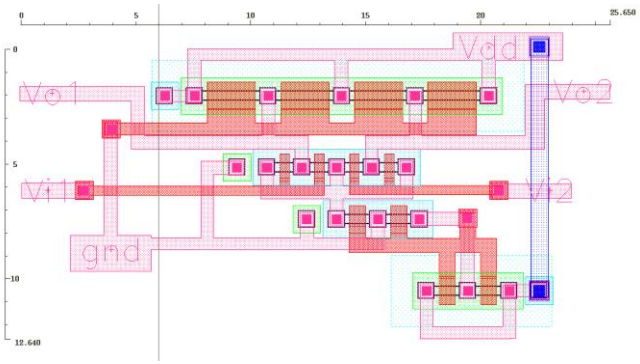

Fig. 7. Fingering and Comb layout of SCL inverter.

IV. Results and Discussion

SCL inverter laid out with four different arrangements to investigate the affect of result RC parasitic on the performance of the SCL inverter. For same inputs, the result shows that the output V_{swing} of the second and forth SCL inverter layout is greater than first and third due of more interconnections of drain and source by using fingering which cause more parasitic resistance. The parasitic capacitance in second layout is more than in forth layout as more S/D interconnections are used, so more areas, which clear from switching noises. Even, the third layout introduces more parasitic capacitance than the first for the same reason. All layouts introduce some amount of resistance due of paths and interconnections which increase the V_{swing} than netlist V_{swing}, Fig. 8, shows the outputs of SCL inverter netlist and it is four layouts for input pulses of 100ns/200ns.

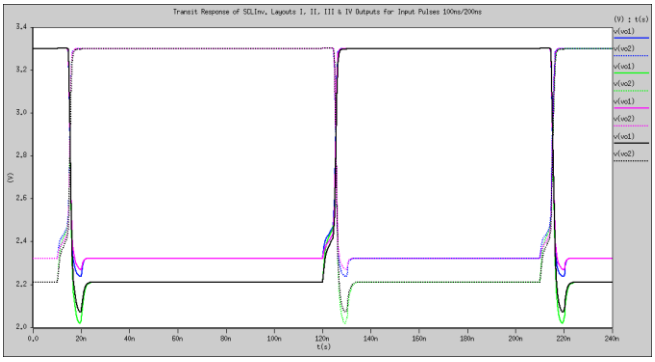

Fig. 8. Outputs of SCL inverter netlist and layouts for 100ns/200ns input pulses.

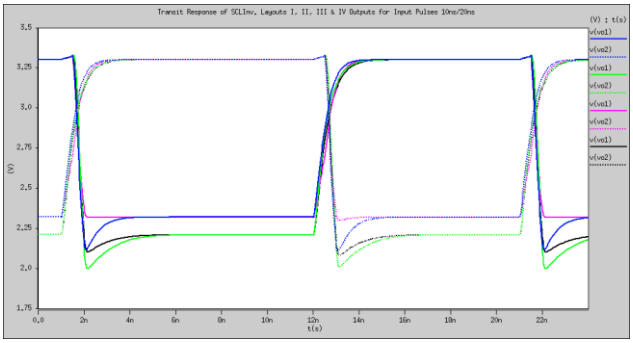

Fig. 9. Outputs of SCL inverter netlist and layouts for 10ns/20ns input pulses.

As the frequency of inputs pulses increases, the shape of output signals get distorted totally since the RC parasitic is a function of signal frequency and the signal delay become superfluous (Fig. 9).

V. Conclusion

The layouts introduce RC parasitic capacitance by signal paths and the way of transistor layout. The different ways of laying out the SCL inverter shows important effect on the performance and signal delay. The post-simulation shows that, the V_{swing} and switching noise are affected by the layout technique; also the total area of the circuit can be reduced significantly. The outputs of four different layouts of SCL show the effect of parasitics on signal delay and output resistance. The introduced parasitics by layouts are increased by increasing of inputs signal frequency. All post-simulation was carried out by using HSPICE, where the layout is done using Virtuoso - Cadence and the extraction done by using Mentor Graphic - Caliber Interactive tool on MIMOS 0.35u PDK.

Acknowledgment

We would like to thank MIMOS Berhad for all its support and offering all work facilities. Also, we don't forget to thank mixed analog signal group (AMS) in Microelectronics & MEMS department at MIMOS for all their help and support.

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