

# Design Technique of an Integrated Gate Driver

Mohammad R. Hoque and Simon S. Ang

**Abstract**— Gate driver circuits are required in power switching converters to switch either their internal or external power MOSFETs. This paper presents a design procedure by optimizing the number of pre-driver inverters and their size ratios to minimize the signal delay of an integrated gate driver circuit for switching converters. The gate driver circuit was implemented in a 1.5 $\mu\text{m}$  CMOS process and tested successfully in a hysteretic synchronous buck switching converter.

**Index Terms** – gate driver, switching regulator, DC-DC converter.

## I. INTRODUCTION

NEXT generation microprocessors need low voltage, fast-response and high-power-density power supplies. It is widely recognized that switching converter is suitable for this application. Switching converter requires a gate driver circuitry to control the external or internal power MOSFETs to deliver the required power to the output. The speed of this gate driver circuitry is extremely important for a high-frequency switching converter. Low propagation delay in the gate driver circuit improves the loop response, and hence, provides a better startup and transient response. Moreover, low propagation delay has the advantage of using smaller magnetic components in high frequency converters. This paper presents a technique to minimize the delay due to the power MOSFETs driver circuitry, hence, optimizing the design for high frequency control [1-3].

## II. BASIC ARCHITECTURE

Basic gate driver circuit consists of a pull up and a pull down circuitries as shown in Figure 1. The “OUT” pin is connected to the gate of an internal or an external power MOSFET which supplies power to the load by switching actions. For a large power MOSFETs, gate capacitances can be as high as a couple of nano farad (nF). To drive such a large gate capacitance, anti-cross conduction circuitry is required in the driver circuit to prevent shoot-through of the power supply from the pull up circuitry to the pull down circuitry.

In the gate driver circuit, there are two sources of signal delay.

M. R. Hoque, Analog Design Engineer, Portable Power Management Group, Texas Instruments 12500 TI Blvd Dallas TX 75243 (phone: 214-567-7471, fax: 214-480-6400, email: [rashed@ti.com](mailto:rashed@ti.com)).

S. S. Ang, Professor, Department of Electrical Engineering, University of Arkansas, 3217 Bell Engineering Center, Fayetteville, AR 72701 (phone: 479-575-7683, fax: 479-575-7967; e-mail: [siang@uark.edu](mailto:siang@uark.edu)).

Delay due to anti-cross conduction circuitry is much smaller compared to the pre-driver delay, since minimum size devices are usually used in the shoot-through protection circuit. Pre-driver usually uses a string of inverter gates where the preceding gate is a couple of times narrower than the subsequent gate. The total number of inverters in the string and their size ratio are the critical design parameter to minimize the signal delay in the pre-driver. This paper presents a design technique of the pre-driver for minimum signal delay by selecting the right number of gates and their proper size ratios. This design technique can be applied to improve the control of the switching converter at high frequency operation [4-6].

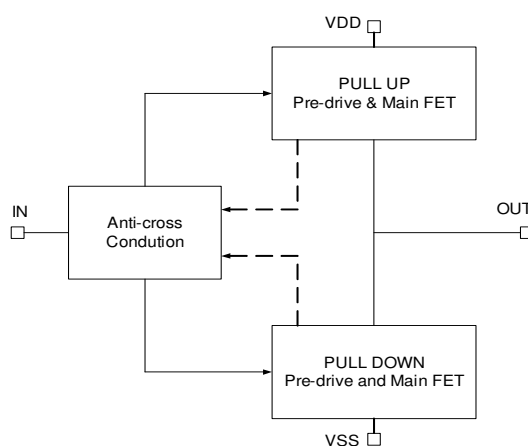


Figure 1. Basic architecture of the driver circuit.

## III. DESIGN FOR MINIMUM PROPAGATION DELAY

The main MOSFET in the pull-up and pull-down circuitries is designed based on the current requirement to charge and discharge the gate capacitance of the external or internal power MOSFETs. For example, if the gate capacitance of the power MOSFET is  $C$ , then the peak current required to charge the gate voltage to the Miller Plateau ( $V_{gs} \sim 2.5\text{V}$ ) is

$$I_{peak} = C \cdot \frac{dv}{dt} \quad (1)$$

where  $dt$  is the rise time of the gate voltage which can be from 20ns to 200ns depending on the maximum switching frequency of the controller.

Once  $I_{peak}$  is determined, the width/length (W/L) ratio of the main drive MOSFET can be estimated for a gate-to-source voltage of 2.5V. As a rule of thumb, designers use the size (W/L

ratio) of the pre-drive stages that is ten times smaller than the main driver for minimum propagation delay, but this is not always true. In this paper, we present a technique to precisely estimate the size ratios and number of stages of the pre-driver.

Figure 2 shows the schematic of the driver circuit with the anti-cross conduction circuit consisting of the NAND 1, NAND 2 and INVERTER 1. Terminal X is connected to the control signal while terminal D is connected to the gate of an internal or an external power MOSFET. The MOSFETs, MN and MP, are the main drive MOSFETs. The size of MN and MP may be different based on process parameters and the required source and sink currents to the gate of power MOSFET connected to point D. For equal source and sink currents, the gate capacitance of MP is usually three times larger than that of MN due to the mobility differences of their conducting carriers. The inverter strings connected between AB and CD are the pre-driver circuit to pull up or to pull down the MP and MN MOSFETs.

Our design goal is to reduce the propagation delay in the driver circuit. As discussed, the main source of signal delay in

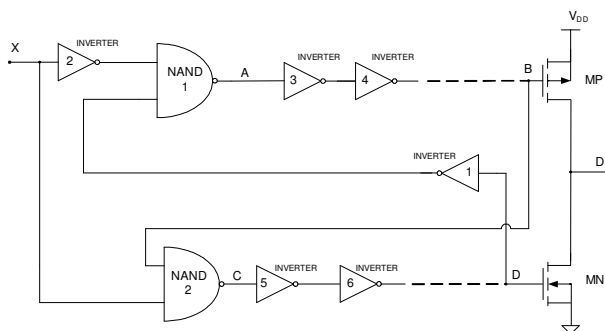


Figure 2. Schematic of the driver with anti-cross conduction circuit.

the driver is the pre-driver circuitry. The delay can be minimized by properly designing the inverter string in the pre-driver. As mentioned earlier, the delay is dependent on the number of inverters in the string and their size ratios. To determine the proper size ratios and the number of inverters in the string, the capacitances at nodes A, B, C and D are first to be estimated. Capacitance at node A has the minimum gate capacitance as the first inverter in the inverting string usually has the minimum size. For example, in a typical 1.5μm CMOS process, the minimum inverter gate capacitance is about 0.0025pF; therefore, CA = 0.0025pF. Capacitance at node B depends on the size of MP. The size of MP depends on I<sub>peak</sub>. From equation (1), with a dt = 100ns and dv = 2.5V, I<sub>peak</sub> = 25mA, where the gate capacitance of the external MOSFET is 1nF in this example.

To supply I<sub>peak</sub> = 25mA, the W/L ratio of MP in Figure 1 is approximately 1200 which imposes capacitance at node B, CB = 4pF. The relationship between the propagation delay and the number of stages of inverter in the pre-driver circuit can be calculated from (2).

$$Delay = N \cdot \left(1 + \sqrt[N]{H}\right) \quad (2)$$

where N is the number of stages and H is the ratio of gate capacitance of B and A nodes.

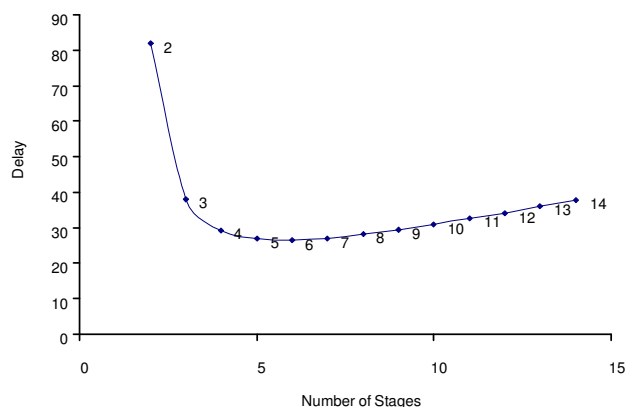


Figure 3. Relationship between number of stages and propagation delay.

Figure 3 presents the relationship between number of inverter stages and signal propagation delays. The vertical scale ‘Delay’ is a relative number. From Figure 3, it can be shown that the propagation delay is minimum for a 5 or 6 stages inverter string in the pre-driver circuit. The size ratio of the inverters in the string is approximately  $\sqrt[5]{(4p/0.0025p)} \approx 4$  times larger than the previous inverter stage. The inverter stages and their size ratio for the signal path from C to D can be determined in a similar manner.

#### IV. DESIGN FOR TEST

The integrated gate driver circuit designed in the previous section was implemented in a hysteretic synchronous buck converter as shown in Figure 4. Power MOSFETs, M1 and M2, are IRF7311, available in a single SO-8 package. The gate capacitances of M1 and M2 are approximately 1nF [7]. The Rf-Cf network superimposes a ramp signal to the sensed output voltage at the input of the hysteretic controller. For proper values of these components, the amplitude of the ramp signal is greater than the output voltage ripple, and thus, the switching frequency becomes independent of the output filter characteristics [2]. Detail description of the operation of hysteretic synchronous buck converter can be found from literatures [3]. The controller of the hysteretic synchronous buck converter was laid out along with the driver circuitry on the same chip.

The die photograph of the chip is shown in Figure 5 where the white boxes marked the different circuit sections of the controller. The high side driver is the driver for M1 MOSFET while the low side driver is the driver for M2 MOSFET. A level shifter is required to switch the high side MOSFET with a voltage higher than the input voltage. The current limit circuit is to protect the power MOSFETs from damage due to over-current. The total chip area, including the input/output

(I/O) bond pads, is approximately  $3.8 \text{ mm}^2$ .

### V. ELECTRICAL MEASUREMENT RESULTS

Figure 6 shows the gate drive voltages, feedback voltage and reference voltage to measure the propagation delay of the hysteretic buck switching converter. When the feedback voltage (purple) goes below the reference voltage (yellow), the gate drive voltage of the M2 MOSFET (blue) goes low. Due to the delay in the control loop, there is a 120ns delay of switching the MOSFET M2 off. This switching delay is due to the signal propagation delay through the hysteretic comparator and driver circuitry. According to our design, the delay in the driver circuit is approximately 100ns with the delays in the hysteretic comparator and anti-cross conduction circuit ignored.

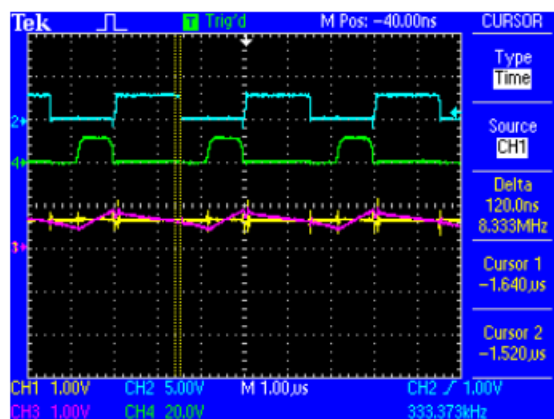


Figure 6. Measurement of delay in the driver.

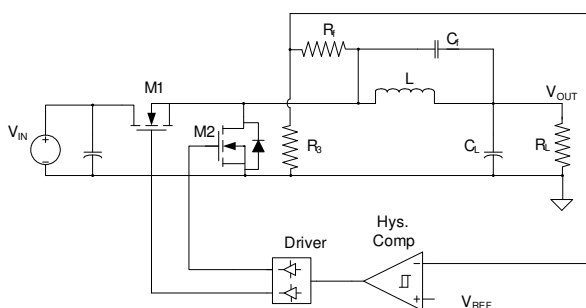


Figure 4. Test Bench for the driver circuit.

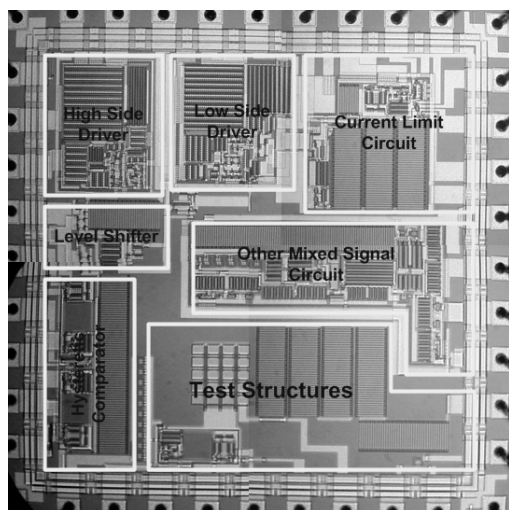


Figure 5. Die photo of the buck controller with driver.

### VI. CONCLUSION

In this paper, a design technique is presented to minimize the propagation delay in the pre-driver. The driver circuit was laid out and fabricated using a  $1.5\mu\text{m}$  CMOS process. The design was tested as a part of a hysteretic buck converter. A driver circuit was designed for 100ns where the delay in the comparator and anti-cross conduction circuit had been ignored. A delay of 120ns was measured and this met the design goal very well.

### REFERENCES

- [1] Z. Yang, S. Ye, Y.-F. Liu, "A New Resonant Gate Drive Circuit for Synchronous Buck Converter", IEEE Transactions on Power Electronics, Vol. 22, Issue 4, July 2007 pp:1311 – 1320.
- [2] D. Haifei, A. Q. Huang, A. Feuerbacher, M. Yan, "Design of a monolithic 2 MHz fast transient voltage regulator chip", IEEE Digital Object Identifier conference 2004, pp. 383– 386.
- [3] W. Gu, I. Batarseh, 'Interleaved synchronous buck regulator with hysteretic voltage control' Proc. IEEE PESC, 2001, pp. 1512–1516.
- [4] K. H. Chen, C. Chien, C.-H. Hsu, L.-R. Huang, "Optimum power-saving method for power MOSFET width of DC/DC converters", Circuits, Devices & Systems, IET Vol. 1, Issue. 1, February 2007 pp: 57-62.
- [5] K. Cho, "Delay calculation capturing crosstalk effects due to coupling capacitors"; Electronics Letters Vol. 41, Issue 8, April 2005 pp:458 - 460
- [6] K. H. Abed, K.Y. Wong, M. K. Kazimierczuk, "Implementation of novel low-power driver for integrated buck converter", IEEE Digital Object Identifier conference 2005, pp. 1757 – 1760.
- [7] "IRF7331 N-Channel Power MOSFET", International Rectifier Datasheet. Aug. 2001.