A 1.57-GHz Low-Power Low-Phase-Noise Quadrature LC-VCO

Quan Pan, Zhiping Wen, Weimin Li

***Abstract*—A 1.57-GHz low-power low-phase-noise quadrature LC-VCO is presented. This paper adopts current source sharing and higher L/C, L/R ratio techniques to achieve power and phase noise optimization. Verified by 0.35-um CMOS process, the VCO features a much lower power consumption of 6.4mW and a low phase noise performance of -140dBc/Hz@3MHz, with a wide tuning range of 14%.**

***Index Terms*—power optimization, phase noise, radio frequency, tuning range, quadrature VCO.**

I. Introduction

In recent years, the rapid growth of wireless communication system has led to an unprecedented demand of high-performance transceivers[1]. After years' development, zero-IF or low-IF transceiver architectures have become the most promising ones offering high performance, high integration and low cost. Therefore, as one of the key components in the high-performance transceivers, the fully integrated quadrature VCO is critical to improve the overall performance. A lot of research effort has been invested in the design of fully integrated low-power low-phase-noise quadrature LC-VCOs.

This work describes a fully integrated quadrature LC-VCO with very low power and very low phase noise performance. This paper is organized into five sections. Section Ⅱ describes systematic LC-VCO concepts of low power and low phase noise. Section Ⅲ explains the details of VCO design. Section Ⅳ presents the details of simulation results and comparison with other prior works, followed by the conclusion in Section Ⅴ.

II. Concepts about powe and phase noise of LC-VCO

Fig. 1 shows a symbolized model for the general LC-VCO. A general LC-VCO mainly consists of three parts: inductor L, voltage-controlled capacitor C (i.e., varactors) and an active element –R. The L and C compose a resonance tank which resonates at the central frequency ω_c constantly under the ideal condition:

$$\omega_c = \frac{1}{\sqrt{LC}} \qquad (1)$$

Unfortunately in the real world, inductor L and capacitor C unavoidably have parasitic resistors, denoted with $R_{L,series}$ and $R_{C,series}$, respectively. In Fig. 1, for simplicity, $R_{L,series}$ and $R_{C,series}$ have been combined into $R_{series} = R_{L,series} + R_{C,series}$, which is dominated by $R_{L,series}$.

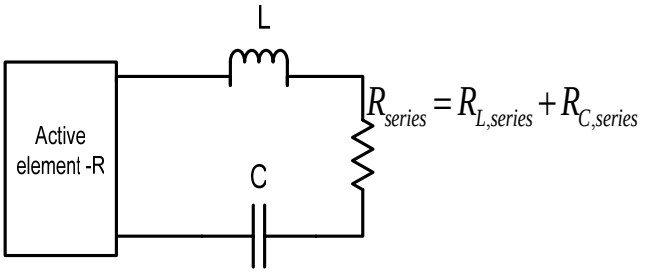

Fig.1 LC-VCO model

So the resonance tank will lose energy on R_{series}, in order to keep this tank resonant at frequency ω_c constantly, an active element –R is designed to compensate the energy loss on parasitic resistors of inductor L and voltage-controlled capacitor C.

As power and phase noise performance are the two most important parameters in VCO design [2], the rest of the section will scrutinize the energy conservation theorem and Leeson's empirical phase-noise expression. These expressions are unconditionally valid for a large signal oscillator [5].

As in Fig.1 LC-VCO model, the total energy transfers back and forth between the inductor L and capacitor C, with a constant sum. As a consequence, the peak energy stored in either the capacitor or inductor is equal to the total energy stored in the LC-tank at any given time, which could be expressed as follows[3][5]:

$$E_{tot} = \frac{1}{2} C I_{peak}^2 R_{series}^{\ 2} = \frac{1}{2} V_{peak}^2 C = \frac{1}{2} I_{peak}^2 L \qquad (2)$$

Manuscript received July 30, 2008.

Quan Pan is with Beijing Microelectronics Tech. Institute (BMTI), Beijing, P.R. China. He is now on the RF group; (e-mail:show@ustc.edu).

Zhiping Wen is with Beijing Microelectronics Tech. Institute (BMTI), Beijing, P.R. China; (e-mail:wzp@catec.casc).

Weimin Li is with Beijing Microelectronics Tech. Institute (BMTI), Beijing, P.R. China; (e-mail:lwm@catec.casc).

Where I_{peak} is the peak amplitude current through the inductor and V_{peak} is the peak amplitude voltage across the capacitor.

So the average power dissipated can be expressed as

$$P_{avg} = \frac{1}{2} R_{series} I_{peak}^2 = \frac{R_{series} C}{2L} V_{peak}^2 \qquad (3)$$

Or with (1)

$$P_{avg} = \frac{R_{series} C^2 \omega_c^2}{2} V_{peak}^2 = \frac{R_{series}}{2L^2 \omega_c^2} V_{peak}^2 \qquad (4)$$

Some useful conclusions could be drawn from equation (4) for low power design of LC-VCO.

1) In order to decrease power consumption, we should reduce R_{series} as much as possible. Furthermore, a smaller R_{series} would also improve phase noise drastically. So in this work we really take good care of the layout of inductor L.
2) As ω_c is constant, a larger inductance would decrease power consumption as well from (4), but this will reduce the tuning range of VCO. Designers should compromise between tuning range and power consumption according to the requirement of transceivers.

As for phase noise conception, Leeson offered a useful phase noise model in [4] [5].

$$L\{\Delta\omega\} = 10\log[\frac{2FkT}{P_{sig}}\{1+(\frac{\omega_0}{2Q\Delta\omega})^2(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|})] \qquad (5)$$

Where P_{sig} is the signal power; Q is the quality factor of resonance tank; factor F accounts for the increased noise in the $1/(\Delta\omega)^2$ region due to the active element –R; $\{1+(\frac{\omega_0}{2Q\Delta\omega})^2$ accounts for the nose floor of output buffer or measurement equipments; $(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|})$ accounts for noise in the $1/(\Delta\omega)^3$ region.

Some useful conclusions could also be drawn from equation (5) for the low phase noise design of LC-VCO.

1) Increasing the signal power P_{sig} can improve phase noise performance. Since P_{sig} is proportional to V_{peak}^2, the larger P_{sig}, the larger amplitude of output voltage, so the lower phase noise. But this parameter should compromise with low-power design consideration.
2) Since increasing quality factor Q can improve phase noise performance quadratically, the most effective way to improve phase noise is to use an LC-resonance tank with a higher Q. A higher Q means a lower resistance of $R_{L.series}$ and a higher inductance of L, which relates with layout of inductor closely.

Paper [5] also points out that higher L/C and L/R ratios can reject phase deviation strongly, improving the phase noise performance accordingly. So in this paper high L/C is guaranteed as long as the tuning range is enough for the transceivers. Higher L/R could be obtained by increase the number of turns N in the inductor, for L is proportional to N^2 while R is proportional to N, so L/R is proportional to N. The optimal number of turns should be achieved in simulation.

So to sum up, in order to achieve both low power and low phase noise, we should reduce $R_{L.series}$ and $R_{C,series}$ as much as possible improving Q of the resonance tank. Also, increasing the inductance of L is useful as long as the tuning range is sufficient for transceivers. And from another perspective, we should try to obtain a higher V_{peak} with the limited power consumption.

III. CIRCUITS DESIGN OF QUADRATURE LC-VCO

A. Structure

Three design options are available to generate quadrature signals:

1) VCO at double frequency followed by divider (may also include buffer, if necessary).
2) Polyphase I-Q VCO scheme.
3) Two cross coupled VCOs.

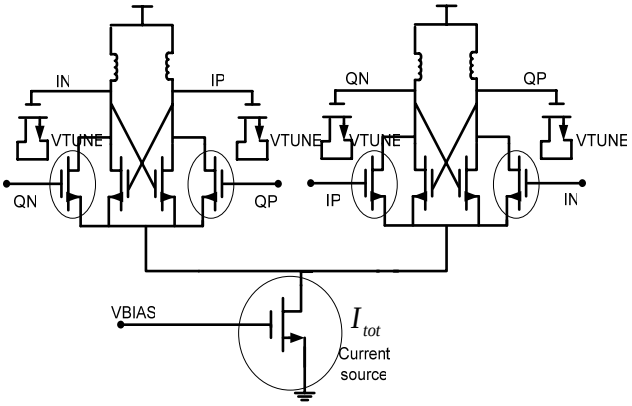

Fig.2 quadrature LC-VCO in this work with current source sharing technique

The first option has the smallest area, because a smaller on-chip inductor is used at double frequency (the smaller inductor, the smaller area) and the divider area is negligible. However, the divider, which is designed to operate at the doubled frequency, consumes too much power.

The second option consumes a lot of power by poly-phase filters and buffers, deteriorating the noise performance of the VCO. Furthermore, this topology requires a lot of die area.

The third option comprises two identical VCOs, which couple together to produce quadrature outputs. This option consumes less power compared with the previous two.

In this work, the topology of two cross coupled VCOs is preferred.

B. Current source sharing and huge MOS capacitors

While most of other paper works make use of separate current sources for the two identical VCOs, this work determines to share one current source for both I and Q VCOs, yielding higher output voltage swing with the same total bias current, which improves power and phase noise performance accordingly. This is because the peak current passing through each core MOSFET during its opening time can be as large as I_{tot} (which means all current flow through this core MOSFET, and the currents flowing through other core MOSFETs are negligible), while in separate current source VCOs, the peak current flowing through the core MOSFET can only be $I_{tot}/2$. Higher peak current means higher voltage swing, which also means lower phase noise performance. So this topology succeeds in achieving the same phase noise with a much lower source current compared with other separate current source VCOs.

In order to filter out the ripples on the gate of the bias-transistors, a huge MOS-transistor capacitor is connected between the gate and ground.

Also, since one common problem of VCO is the start-up difficulty, additional backup current source circuits are designed in parallel with current source connecting to the Band-gap output of the whole chip.

C. LC-Tank

16.05-nH inductors fabricated by the top thick metal are used in this work, yielding a Q of 8 and turns of 7. To assure the reduction of parasitic resistance, a ground active-shield is designed. Lower parasitic resistance and higher number of turns mean Higher Q and higher L/R ratio, which totally improve the overall phase noise performance [5].

Because of high $C_{\max}/C_{\min}$ ratio and low cost for process, NMOS transistors are used as varactors providing the voltage-controlled capacitance. The minimal gate length of 0.35um is preferred for maximal varactor Q and noise performance[3]. In order to reduce $R_{C,series}$, which would increase the Q of resonance tank, multi-finger folded NMOS varactors are adopted shown in Fig.3 .

D. Active element –R

Active elements are used to generate negative resistance, compensating the parasitic resistance loss of inductor L and NMOS varactors. Due to simulation optimization of power and phase noise, coupling MOSFETs denoted in Fig.2 with four circles are sized at 20% of the main core MOSFETs.

IV. Simulation Results

To verify concepts and results obtained in Section Ⅱ and Section Ⅲ, this work has implemented the quadrature LC-VCO in 0.35um CMOS process. Inductors are implemented by the top thick metal layer with a ground active-shield to reduce parasitic resistance loss of metal and substrate, which is very critical for the overall performance. This work has inductors of 16.05-nH with a Q of 8 and turns of 7 at 1.57GHz operation frequency.

Fig. 3 shows the symmetric layout of this quadrature LC-VCO. Fig.4 shows the voltage outputs of quadrature LC-VCO.

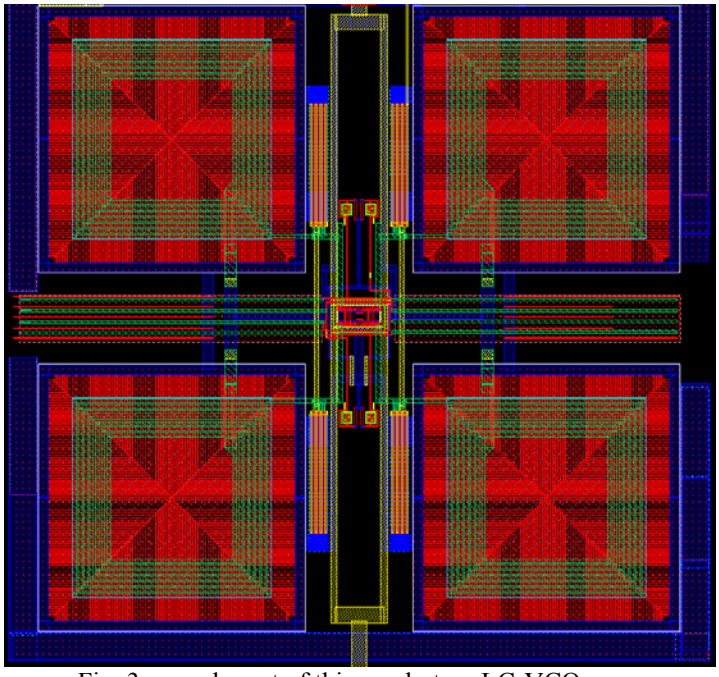

Fig. 3 core layout of this quadrature LC-VCO

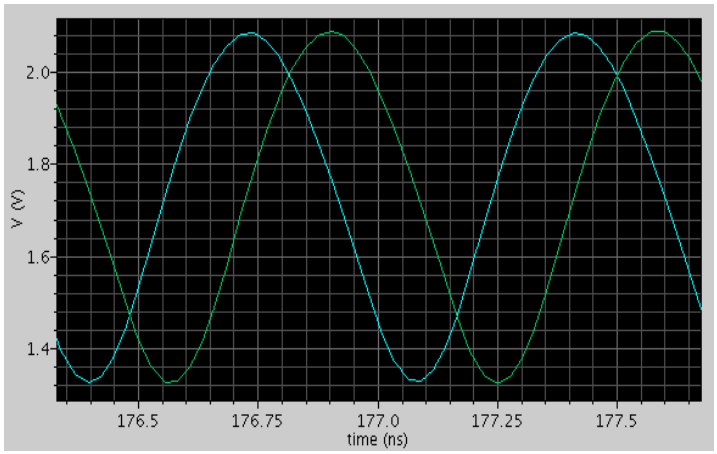

Fig.4 voltage output of quadrature LC-VCO

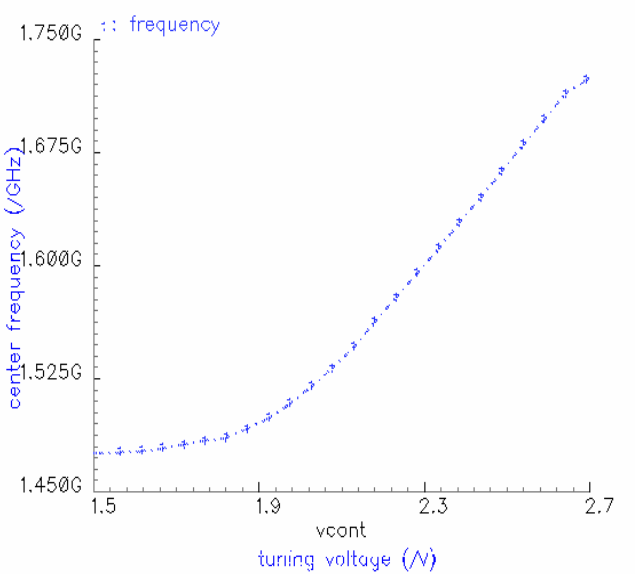

Fig.5 tuning range of this quadrature LC-VCO

The tuning characteristic of this LC-VCO is presented in Fig. 5.

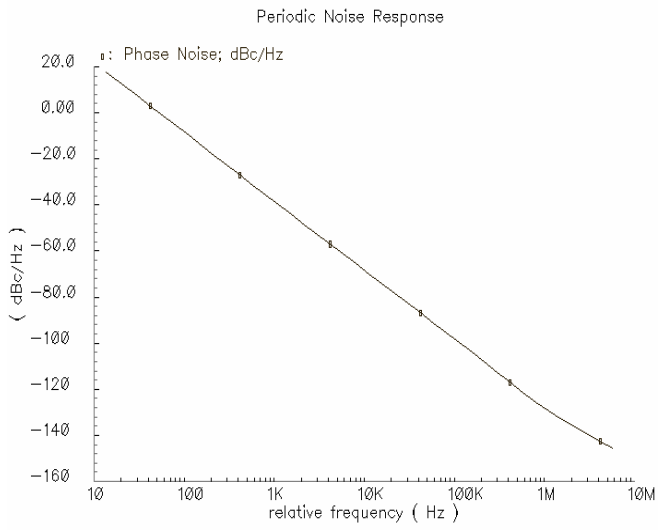

Fig.6 phase noise of this quadrature LC-VCO

The phase noise performance is presented in Fig.6.

TABLE Ⅰ
LC-VCO RESULTS SUMMARY

Process	0.35-um CMOS
Centre Frequency	1.57GHz
Tuning Range	220MHz(14%)
Phase Noise	-140.618dBc/Hz@3MHz
Power Consumption	6.4mW
Area	730um*700um (Not include pad.)

Table Ⅰ summarizes the key parameters of this quadrature LC-VCO, which are used to compare with some prior works in table Ⅱ.

TABLE Ⅱ
COMPARISON OF THE PERFORMANCE WITH PRIOR WORKS

	Process (um)	Freq. (GHz)	Power (mW)	Phase Noise (dBc/Hz)
[5]	0.25	1.8	20	-143@3MHz
[6]	0.25	1.8	24	-132@3MHz
[7]	0.25	1.57	30	-147@3MHz
[8]	0.35	1.8	50	-140@3MHz
[9]	0.35	2	20.8	-140@3MHz
This work	**0.35**	**1.57**	**6.4**	**-140@3MHz**

V. Conclusion

A fully integrated CMOS quadrature LC-VCO at 1.57-GHz implemented by a 0.35-um CMOS process is presented. Through current source sharing and higher L/C, L/R ratio techniques, using multi-finger folded NMOS-varactors, a much lower power consumption of 6.4mW and a low phase noise performance of -140dBc/Hz@3MHz are obtained, with a wide tuning range of 14%. This VCO can meet the demands of high-performance zero-IF or low-IF transceivers.

Acknowledgment

The authors would like to thank the RF groups in Beijing Microelectronics Tech. Institute (BMTI) for their support in team-work for the whole chip.

References

[1] Ting-Ping liu and Eric Westerwick, "5-GHz CMOS radio transceiver front-end chipset," IEEE J.Solid-State Circuits, vol.35, no.12, Dec. 2000.
[2] A. Hajimiri and T.H. Lee, "A general theory of phase noise in electrical oscillator," IEEE J.Solid-State Circuits, vol.33, pp. 179-194, Feb. 1998.
[3] Thomas H. Lee, The design of CMOS radio-frequency integrated circuits, second edition,Cambridge University, 2004.
[4] D.B. Leeson, "A simple model of feedback oscillator noise spectrum," Proc. IEEE, pp.329-330, Feb. 1966.
[5] M. Tiebout, "Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS," IEEE J.Solid-State Circuits, vol.36, pp. 1018-1024, July 2001.
[6] B.De Muer, N.Itoh, and M.S.Steyaert, " Low supply voltage fully integrated CMOS VCO with three terminals spiral inductor," in Proc.25th European Solid-State Circuits Conf., Duisburg, Germany, Sept. 1999,pp. 207-209.
[7] P.Vandreani and M. Steyaert, "A 1.57-GHz fully integrated very low-phase –noise quadrature VCO," IEEE J.Solid-State Circuits, vol.37,pp. 653-656, May 2002.
[8] P. Andreani, A. Bonfanti, L.Romano and C. Samori, "Analysis and design of a 1.8-GHz MOS LC quadrature VCO," IEEE J.Solid-State Circuits, vol.37, no.12, pp. 1737-1747, Dec 2002.
[9] P. Andreani and X. Wang, "On the phase-noise and phase-error performances of multi-phase LC CMOS VCOs," IEEE J.Solid-State Circuits, vol.3, no. 11, pp. 1833-1843, Nov 2004.