An Approach for Analyzing and Evaluating Semiconductor Design Projects

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Abstract—**Performance Management is the key factor to successfully persist in the semiconductor market. In this paper an approach for analyzing and evaluating semiconductor design projects is presented. The design process is transformed into a task graph to better analyze and optimize its dependencies. Optimization objectives can be time as well as costs. Key Performance Indicators (KPIs) are defined and classified into the main areas *finance*, *resources*, *process* and *technical output* to appraise the project.**

Keywords: performance management, Key Performance Indicators, chip design, task graph, sensitivity

1 Introduction

The semiconductor industry is characterized by fast technological changes, small time-to-market windows and a prodigious growth rate of 8 to 10 % p. a. in the long term [1]. Despite the current economic crisis, a compound annual growth rate of 6.1 % for the forecast period, 2008-2011 is projected [2]. CMOS semiconductor technology still permits the fabrication of much more diminutive structures. Improving the design process and its productivity is of central importance for closing the increasing design gap which exists between the ability in manufacturing chips and the capability to design them [3]. However, the semiconductor design process still knows no technically mature metrics to compare and evaluate performance and productivity. Although it is fairly difficult to conceive the many factors affecting design productivity, such measurements are the key to improve the process and thus persist and gain market share. Hence, meaningful Key Performance Indicators (KPIs) embedded in an all-embracing Performance Management System need to be developed.

"You cannot improve what you cannot measure" [4] is probably the decisive axiom for defining KPIs for semiconductor design projects. For this purpose, an analysis of the design flow with its dependencies is inevitable. Furthermore, the most important parameters to calculate the KPIs have to be identified.

Section 2 gives an overview of the main facts and modules of the Performance Management System. Section 3 and Section 4 describe further details of the system and the analysis of the design process. The derived ideas and a conclusion are given in the last section.

2 Performance Measurement

In order to measure and thus improve the design process, an all-embracing Performance Management System for semiconductor design projects is built up. The Chip Design Performance Management System (CDPMS) enables a multidimensional view on all perspectives and processes of a company and helps managers to make the right decisions [5].

In Fig. 1 an overview of the CDPMS is shown. The Data Entry Module allows an easy entry of the required information of the chip design process. The data needed is organized into the categories *input*, *process* and *output*. The parameters and metrics required to calculate the KPIs are stored in the database. In the Project Appraisal Module, the KPIs are classified into the four main areas *finance*, *resources*, *process* and *technical output*. On top stands a High Level Key Performance Indicator (HL-KPI) which expresses a main statement of the productivity dependent on the requirements and application of the design project. The traffic lights are part of a warning system, which indicates actual/target differences of each KPI [5]. Furthermore, the sensitivity of the KPI to main parameters is expressed in the total differential δ_{KPI}. Further details are explained in the following sections.

3 Data Entry

Before evaluating the project, information about the process and resources used need to be acquired. The chip design process consists of a series of activities which transform design artifacts into different states of abstraction.

Data about the costs of resources, the (planned) market price and other project requirements are collected in the category *input*. The information which is available after finishing the process, e. g. technical parameter, personnel

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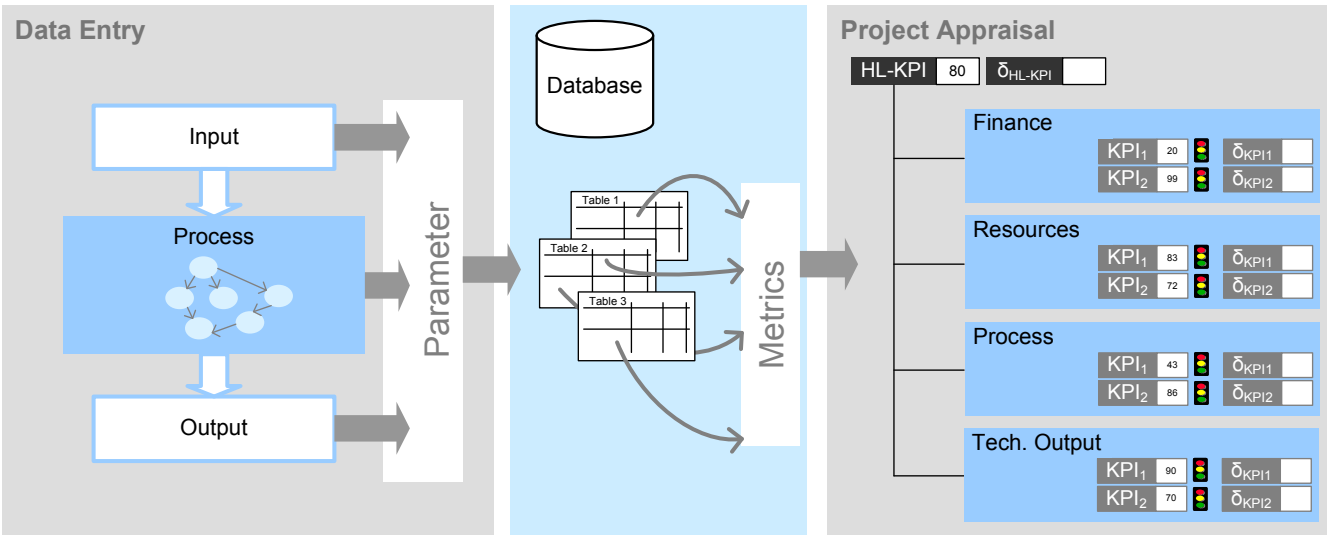

Fig. 1: Overview of the CDPMS

effort, is classified into *output*. The data to be entered are determined by the defined KPIs. The category *process* acquires the required data about the hierarchy and available states of the design artifact as well as the common design flow in order to generate a task graph.

The advantages of the task graph are the clarification of the existing dependencies between the activities as well as a clear and transparent representation of the process. Some questions which can be answered are the following:

- How is the workload of my resources?
- How is the design flow affecting the costs?
- How is the minimal project duration/maximal workload?
- How can the process be optimized with respect to costs and time?

In the first step, the task graph is generated from the information about the design artifact (DA) and the design flow. The nodes represent the activities of the design process executed on specific DAs including iterations. The edges of the task graph represent the dependencies of the specific activities, that means which activity has to be executed before the other. To generate the task graph, the DA hierarchy and the common activities' sequence of the company need to be known. Furthermore, the available states of the DAs need to be considered. If the DA can be reused from another project the activity sequence can be started from that point on.

The example in Fig. 2 shows the task graph generated from the DA hierarchy and the common activities' sequence. The hierarchy comprises two DAs 1 and 2, each with two submodules DA 1.1 and DA 1.2 as well as DA 2.1 and DA 2.2. The activities' sequence in the digital design process is quite steady. In Fig. 2, two front-end activities are mentioned to illustrate the resulting task graph. The generic activities *Coding in Hardware Description Language (HDL-C)* and *Synthesis (Syn)* are applied to the specific DAs. The flow starts with the coding of the top module, then the coding on lower level follows. The submodules need to be synthesized separately before they are integrated to the higher DA. In the example, there is no reuse, thus all the DAs need to be developed. If the available state of a DA is e. g. a synthesized netlist, the preceding activities can be omitted. Solely, activities to adapt the reuse blocks need to be considered. The causal order of the activities executing DAs determines the edges in the task graph.

The second step after generating the first task graph is to optimize the process depending on the objectives.

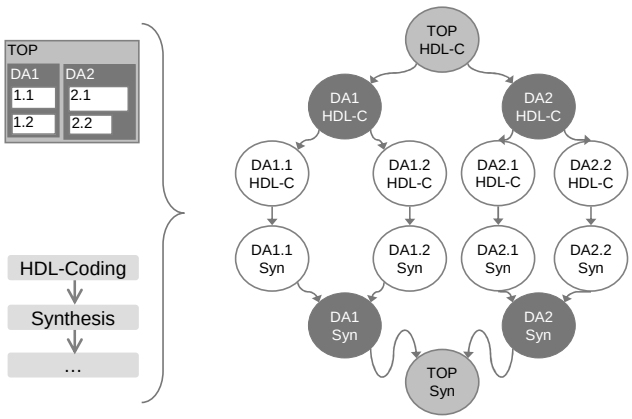

Fig. 2: Step 1 - Generating the task graph

The following three scenarios are possible:

1. Optimization of time, resources are variable
2. Optimization of workload, time is variable, minimum of resources is fixed
3. Optimization of workload, resources are variable, time is fixed

To optimize the process using the task graph, we assume that the duration of the activity executed on a specific DA is known. Furthermore, the type and the minimum amount of resources needed to execute the activity (e. g. designer: 2 HDL-Coder, license: 2 synthesis licenses) has to be specified. We assume that the resources are used during the whole time of the activity's duration.

The amount of resources can be either variable or fixed. Either the project manager can calculate with indefinite resources to optimize other objectives (e. g. time) or there is a fixed amount designated for the project and the workload need to be optimized. However, the fixed amount of resources cannot be less than the maximum of the resources needed for an activity.

Scenario 1

In Scenario 1 the main objective is to minimize the project duration (pd). Early market entry is a key factor to remain competitive. To achieve a minimal project duration, the resources required need to be available in a convenient time. Every time a starting activity needs new resources, they are provided. The maximal amount of the same resource type used at the same point in time determines the maximal amount of resources needed.

The critical path of the task graph constitutes the minimal project duration. In Fig 3, the duration T ($[T] = days$) and the number of designers d needed for each activity of the anterior task graph example is noted. The critical path is marked by bold arrows. The minimal project duration for the frond-end activities is 31 days.

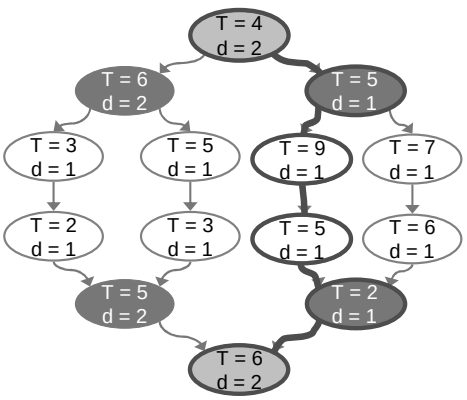

Fig. 3: Critical path of the task graph

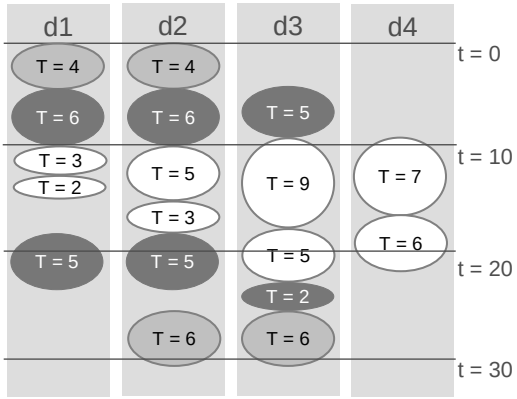

Fig. 4: Allocation of activities in Scenario 1

The description of the process and its dependencies in a task graph shows exactly the activities which can be executed in parallel and which activities follow others. On the basis of this information, the planning and allocation of activities to resources can be made.

The activities can be distributed among any resources of the design process (e. g. designers, computers, licenses) depending on the resource type to be optimized. Fig. 4 shows the allocation of activities to designers of the task graph. The allocation is based on the principle "first come first serve". To execute the process in minimal time, four designers are required. Time for organizational meetings is not considered. In this case, the average workload (aw) of the designers with respect to the total project duration is 71,77 %.

Scenario 2

Scenario 2 is aimed at optimizing the workload of a fixed amount of resources, assuming that a fixed pool of resources is given for the execution of the project.

The example in Fig. 5 shows the allocation to two designers. The activities are executed sequentially considering the dependencies. In this scenario, the project duration is 45 days and the average workload of the designers is 98,89 %.

Scenario 3

In the case of a restricted project duration in order to reach a specific time-to-market window, the workload of variable resources can be optimized. Fig. 6 shows the allocation of activities to the designers in Scenario 3. The

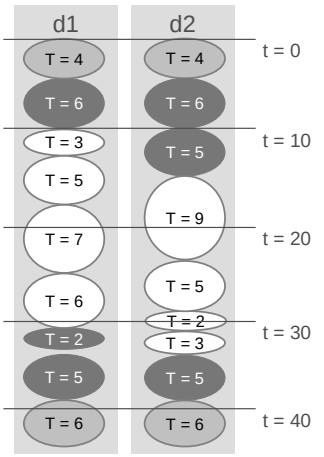

Fig. 5: Allocation of activities in Scenario 2

objective is to use as few resources as possible to execute the process in the given time t_{fix} and to optimize their workload.

Is the fixed time 34 $days \leq t_{fix} < 45$ $days$, three designers are needed. The project duration of this Scenario 3 for the task graph is 34 days and the average workload of the designers is 87,25 %.

A summary of the results of all scenarios is given in Table 1. After optimizing the design process itself, the next step is to provide appropriate KPIs to evaluate the chip design project.

4 Project Appraisal

In order to define Key Performance Indicators, the main goals of the company and the project itself have to be clear. In the first place, a company wants to maximize the profit. For this reason, the main goals are the minimization of the research and development effort and the project duration as well as the maximization of reuse, quality of the products and the success rate of the projects. In the following, main questions resulting from

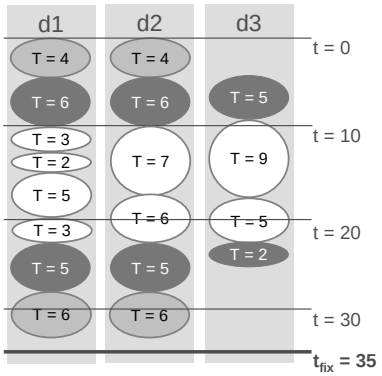

Fig. 6: Allocation of activities in Scenario 3

Table 1: Overview of the scenarios

Sc.	Optimization	d	pd/*days*	aw/%
1	time, res. var.	4	31	71,77
2	workload, res. fix	2	45	98,89
3	workload, res. var.	3	34	87,25

the goals are classified into the four main areas *finance*, *resources*, *process* and *technical output* in order to define relevant KPIs and thus evaluate the design project.

Finance

This area implies the costs and the profit of the design project. Main questions are:

- What are the total development costs of the project and the cost breakdown?
- How high is the personnel effort in the project?
- How high is the financial profit of the project?
- What is the immaterial benefit of the project?

Resources

Some of the questions concerning the resources were already presented in Section 3.

- What is the optimal resource allocation?
- What is the workload of the resources?
- What is the frequency of use of the resources?
- How is the employee loyality/turnover rate?

Process

This area implies questions about the scheduling and optimization of the process.

- Is the planned project duration realistic? Does the end of project reaches the time-to-market window?
- How is the fulfillment of the milestones?
- How can the process be optimized concerning time and costs?

Technical Output

All technical parameters are classified into this area. The questions refer to the quality and completion of the DA.

- Does the design result comply with the specification?
- Is the quality sufficient?
- What is the remaining time to completion?

The next step is to derive Key Performance Indicators from the main questions to evaluate the design project. The following example demonstrates the procedure in calculating the project duration.

A lot of factors influence the duration of a project. The number of designers deployed in the project (d), the point in time of a change of specification (t_{SC}) and the ratio of reuse (a_R) rank among the most important factors.

The project duration as a function of the number of designers (pd_d) is shown in Fig. 7. Increasing the number of designers leads to a decreasing project duration. Nevertheless, the more designers are deployed, the less time is saved because of the limited parallelization of activities. The reference point of the function ($pd_d = 1$) is the execution of the project with only one designer ($d = 1$). The equation of the project duration is

$$pd_d(d) = 0,9 \cdot 1/d + 0,1.$$

Fig. 8 illustrates the project duration as a function of the point in time of a change of specification (pd_{tSC}). The size and difficulty of the change lengthen the project duration [6]. t_{SC} is stated in percent of elapsed time. Provided that the specification change occurs before a certain point A the process is able to accommodate the change without any delay in completion and thus the project duration does not change. In the example in Fig. 8 point A is 0.33.

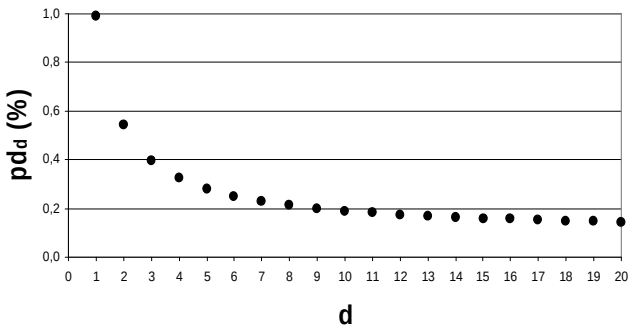

Fig. 7: Project duration pd as a function of number of designers

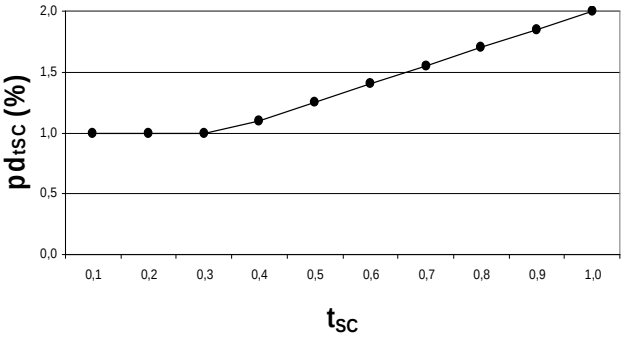

Fig. 8: Project duration pd as a function of point in time of change of specification

Assuming that the project P and the modified project P' in isolation take the same time ($pd = pd' = 1$) a specification change at the end of the project would imply two independent projects executed successively in the worst case. The function pd_{tSC} is

$$pd_{tSC}(t_{SC}) = \begin{cases} 1 & 0 \leq t_{SC} < A \\ \frac{1}{1-A} \cdot t_{SC} + (\frac{1-2A}{1-A}) & A \leq t_{SC} < 1 \end{cases}.$$

The project duration as a function of the ratio of reuse (pd_{a_R}) is sketched in Fig. 9. a_R is stated in percent. The reference point ($pd_{a_R} = 1$) is the project execution without the reuse of intellectual property ($a_R = 0$). The equation for pd_{a_R} is deduced from the total development costs C_{tot}

$$C_{tot} = F \cdot d \cdot pd.$$

F is a cost factor which includes all costs of the project per designer and per month, e. g. salaries, license costs, hardware costs, training costs and organizational costs. F and the number of designers deployed d are independent of the reuse ratio. Only the project duration pd depends on the ratio of reuse a_R. Hence, the total development costs with reuse (C_{totR}) and without reuse (C_{totOR}) are:

$$C_{totR} = F \cdot d \cdot pd_R$$

and

$$C_{totOR} = F \cdot d \cdot pd_{OR}.$$

Furthermore, C_{totR} can be calculated by

$$C_{totR} = C_{totOR} - a_R \cdot C_{totOR} + a_{ov} \cdot a_R \cdot C_{totOR}.$$

The development costs of the reused blocks can be subtracted. However, some adaptations have to be made in order to integrate the intellectual property into the new design environment. The costs incurred thereby depend on the adaption rate a_{ov}. In the example in Fig. 9 a rate of $a_{ov} = 0.2$ is assumed.

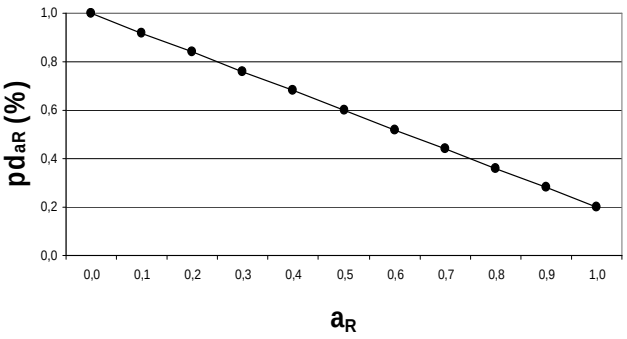

Fig. 9: Project duration pd as a function of ratio of reuse

The saving by reuse S_R is calculated by

$$S_R = 1 - \frac{C_{totR}}{C_{totOR}} = 1 - (1 - a_R \cdot (1 - a_{ov})) = a_R \cdot (1 - a_{ov})$$

and equals

$$S_R = 1 - \frac{pd_R}{pd_{OR}}.$$

Hence, the project duration as a function of the ratio of reuse is

$$pd_{a_R}(a_R) = \frac{pd_R}{pd_{OR}} = 1 - a_R \cdot (1 - a_{ov}).$$

To get the project duration subject to the three parameters, the independent equations are linked by multiplication:

$$pd(d, t_{SC}, a_R) = pd_d \cdot pd_{tSC} \cdot pd_{aR}$$

In the reference point $(d = 1, 0 \leq t_{SC} < A, a_R = 0)$ the project duration is $pd = 1$.

However, not only the absolute value of the equation gives the information a company needs. To know what kind of risks and chances are in the variance of a parameter and which parameter causes the biggest impact on the KPI the total differential in a point P is calculated by

$$\begin{aligned} \delta pd = & \left.\frac{\partial pd_d}{\partial d}\right|_P \cdot pd_{tSC} \cdot pd_{aR} \cdot \delta d \\ & + \left.\frac{\partial pd_{tSC}}{\partial t_{SC}}\right|_P \cdot pd_d \cdot pd_{aR} \cdot \delta t_{SC} \\ & + \left.\frac{\partial pd_{aR}}{\partial a_R}\right|_P \cdot pd_d \cdot pd_{tSC} \cdot \delta a_R. \end{aligned}$$

In this certain point P the sensitivity of each parameter is scaled by the values of the other parameters. For example, in point $P_1 = (d = 2, t_{SC} = 0.67, a_R = 0.13)$ the total differential of the project duration is

$$\delta pd = -0.30\ \delta d + 0.74\ \delta t_{SC} - 0.66\ \delta a_R.$$

Increasing the ratio of reuse has the greatest impact on decreasing the project duration. Specification changes should be as early as possible in the project.

5 Conclusions and Outlook

In this paper an approach of analyzing and evaluating chip design processes is presented. The design process with its dependencies is described as a task graph for optimization. Three scenarios with different objectives are used to allocate the activities to the resources. To evaluate the project, main questions are pointed out to develop Key Performance Indicators in the areas *finance*, *resources*, *process* and *technical output*. The calculation of the sensitivities and the total differential give information about the parameter with the greatest impact on the KPI.

Further work will be based on optimization algorithms and resource allocation. Besides, the important parameters for each KPI are studied and the equations for the KPIs will be developed.

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