Design and Implementation of a CMOS Posicast Pre-Shaper For Vibration Reduction of Op-Amps

M. Rasoulzadeh, M. B. Ghaznavi-Ghoushchi

***Abstract*—Posicast-based control is a widely used method in vibration reduction of lightly damped oscillatory systems especially in mechanical fields. In this paper, a fully CMOS Pulse pre-shaper for realization of Posicast command is proposed. Our design is based on delay-and-add approach for the incoming pulses. The delay is done via a modified Schmitt Trigger-like circuit. The adder is implemented by a simple non-binary analog adder terminated by a passive element. Our proposed design has the flexibility in configuration of time delay and amplitude of the desired pulse-like shapes. The delay is controlled via the delay unit and the pre-shaped pulse amplitudes are controlled by analog adder unit. The overall system has 18 MOS transistors, one small capacitor and one resistor. To verify the effectiveness of recommended method, it is experienced on the real CMOS Op-Amps. HSPICE simulation results on 0.25u technology show a significant reduction on overshoot and settling time of the under test Op-Amp. The mentioned reduction is more than 95% in overshoot and more than 60% in settling time of system.**

***Keywords*- Op-Amp; Posicast; Pre-Shaper; Vibration**

I. INTRODUCTION

The characteristics of an amplifier circuit using of an Op-Amp can be modified by the application of negative feedback. The resulting amplification can be alerted, its stability improved, the magnitude of undesired signals reduced, the bandwidth and operating speed increased, and nonlinearities reduced [1]. However, the benefits of using feedback are accompanied by two drawbacks. First the gain of the circuit is reduces in almost direct proportion to the other benefits obtained. This can be solved by adding extra amplifier stages with a consequent increase in hardware cost. The second potential problem associated with the use of feedback is the possibility of oscillation to occur in the circuit [2].

In Op-Amps, the mentioned oscillatory manner, could be determined by overshoot percent and settling time of the step response of the system.

Two main concepts of control systems are speed and stability that can be assigned in time-domain by settling time and the overshoot percent, respectively [3].

Manuscript received July 25, 2009.
M. Rasoulzadeh is with the Electrical Engineering Department, Shahed University, Tehran, Iran. (e-mail: mansourr61@yahoo.com)
M. B. Ghaznavi-Ghoushchi is with the Electrical Engineering Department, Shahed University, Tehran, Iran. (e-mail: ghaznavi@shahed.ac.ir)

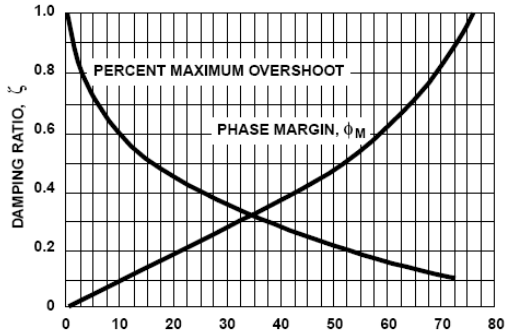

Figure 1. Percent overshoot and phase margin as a function of damping ratio [4]

In frequency-domain, phase margin is used to determine system stability which has reversed relation with the overshoot percent in time-domain. The relationship of overshoot percent and phase margin with damping ratio ζ is presented in Figure 1. So, the reduction of overshoot leads to increasing the phase margin and more stability.

Classical Posicast is a feed-forward control method for lightly damped systems which reshapes the reference input to eliminate the oscillatory response that is characteristic of lightly damped systems.

Posicast control originally introduced in the late 1950s [5], [6] and further studied in the early 1960s [7], [8]. Some of applications of Posicast are as follows: A Posicast-based control method is presented for both buck and boost converters in [9]. In [10] a three step modulation signal shaping compensator is designed and proposed to improve the LC resonant damping in a PWM CSR system. Using Posicast-based controller in DC-DC converters to eliminate the overshoot on their step response is presented in [11]. In [12]-[14] some other applications of Posicast are presented.

In this paper, a CMOS pulse shaper circuits is designed to shape the input step pulse to a modified pulse with specific characteristics that can be used as Posicast pulse. Then, the Posicast pulse is applied on an Op-Amp to show the effect of Posicast pulse in oscillation reduction of step response of Op-Amp. The simulation results show a meaningful improvement in both overshoot percent and settling time of the Op-Amp.

The reminder of this paper is organized in the following manner. In section 2, Posicast control theory and concepts are described. The specifications of a desired Posicast pre-shaper for our especial work, is mentioned in section 3. Also, the design process of the proposed pre-shaper circuit is

presented in this section. Section 4 includes applying the Posicast pulse which is generated with proposed pre-shaper, on an Op-Amp and simulating the results. Finally, section 5 concludes the paper.

II. Posicast Control, Theory and Concepts

Consider a system with a lightly damped step response as presented in Figure 2(a)-dashed.

The overshoot in the response can be described by two parameters. First, the time to the first peak is one half the period of under-damped response (T_d). Second, the peak value is described by $1+\delta$ where δ is the normalized overshoot, which ranges from zero to one.

Posicast divides the step input command into two parts, as presented in Figure 2(b). The amplitude of first part is scaled so that the first peak of the response precisely reaches the desired final value. The amplitude of the second part of the Posicast input is equal to the amplitude of original step input and has specific delay to precisely cancel the remaining oscillatory response, thus causing the system response to stay at the desired value [15]. The classical Posicast can be modeled using just the two parameters δ and T_d. The resulting system output is shown in Figure 2(a)-solid.

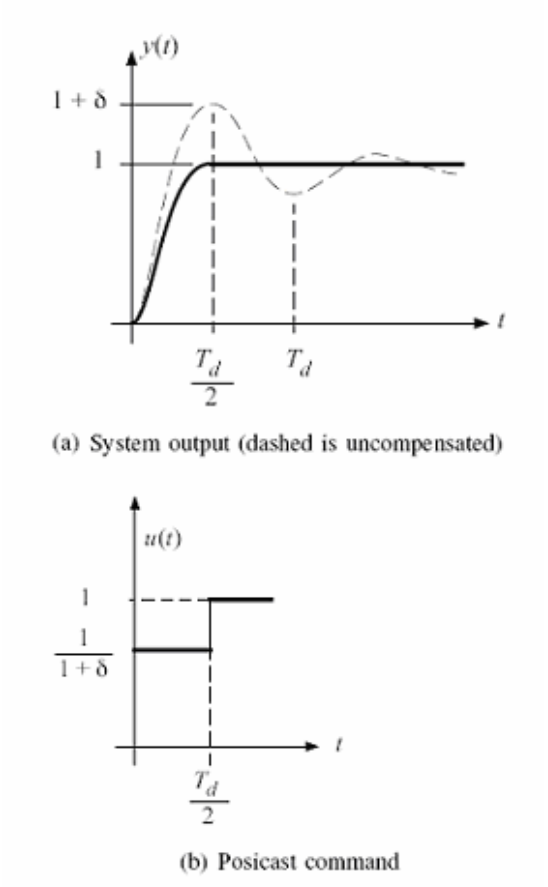

Figure 2. (a) Step response (dashed), Posicast response (solid) (b) Posicast pulse [15]

III. CMOS Posicast Pre-shaper

In this work, the target system for applying Posicast pulse is the Op-Amp circuit and regarding that the Op-Amps are experiencing both positive and negative edges in its input, the pre-shaper should shape the input step pulse in both positive and negative edges. The input and modified pulses are shown in Figure 3. Note that, the Posicast pulse in both positive and negative edges has a low voltage level, a high voltage level, a middle voltage level, and a specific timing between them.

The block diagram of proposed pre-shaper is presented in Figure 4. As seen, the step pulse is delayed by a "delay circuit" and the resulting pulse is added with the original step pulse using an "adder circuit". At the following, the internal structures of the delay circuit and adder circuit are described.

The delay circuit is a fully CMOS structure (Figure 5) which based on the modified design of delay circuit in patent [16]. The original delay circuit gives the needed delay to input pulse but does not make the sharp edges for output pulse. This problem is solved in modified design by adding a buffer in output. As seen in Figure 5, the delay circuit is composed of four consecutive inverter stages.

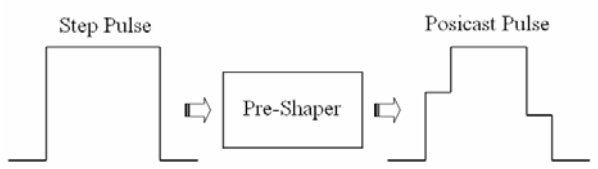

Figure 3. Shaping step pulse to Posicast pulse

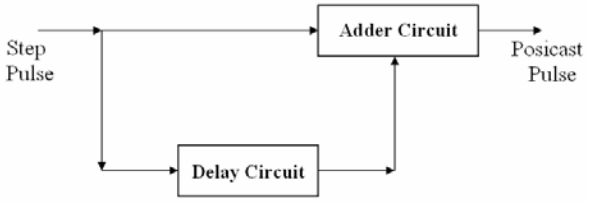

Figure 4. Block diagram of pre-shaper

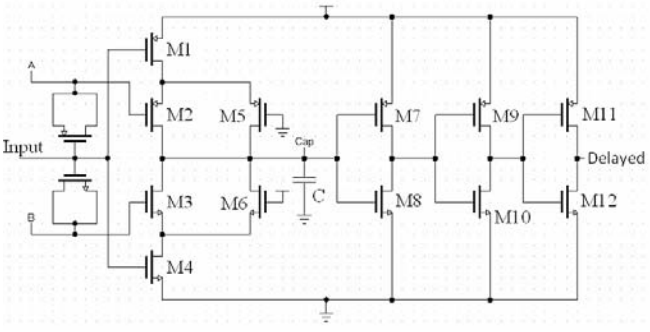

Figure 5. Proposed delay circuit with modification and improvement on patent in [16]

The first and second inverters and the capacitance C between them make the main delay and the third and fourth inverters make sharp edges for output pulse. The value of C has a direct relation with the overall delay of the circuit and the main delay generated by the capacitance. Also, the delay of circuit can be controlled by voltage terminals A and B. the delay of positive and negative edges of input pulse can be adjusted separately and accurately by changing the sizing of transistors M7 and M5, respectively. This leads to a accurate delay with independent tuning for positive and negative edges. The simulation result of delay circuit (Figure 5) for a step input pulse is shown in Figure 7(a and b).

There are several methods to add the input and delayed pulse to create the Posicast pulse. For example an Op-Amp in non-inverting topology can do that. But, a real Op-Amp has some non-idealities which will affect the adding operation and the result will be undesired. In this work, a simple CMOS circuit is proposed to add the input step pulse and delayed pulse.

The schematic of designed adder circuit is presented on Figure 6. The current passing from resistor R (which is connected to voltage source (VDD) via three different paths) makes the output voltage. The transistors act as switches that are controlled by the input and delayed pulses. So, when both inputs are low level, all transistors are off and all paths are cut. Therefore the output voltage is in lowest level (zero in this example). When only one of inputs is high level, the resistor is connected to VDD via corresponding path and the output voltage is the middle level of Posicast pulse for positive or negative edge. Finally, when both inputs are high level, the resistor is connected to VDD via all three paths and in this situation the output voltage will be the highest level of Posicast pulse.

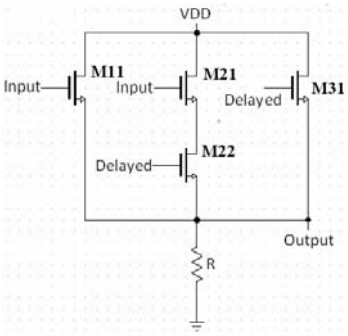

Figure 6. Proposed adder circuit

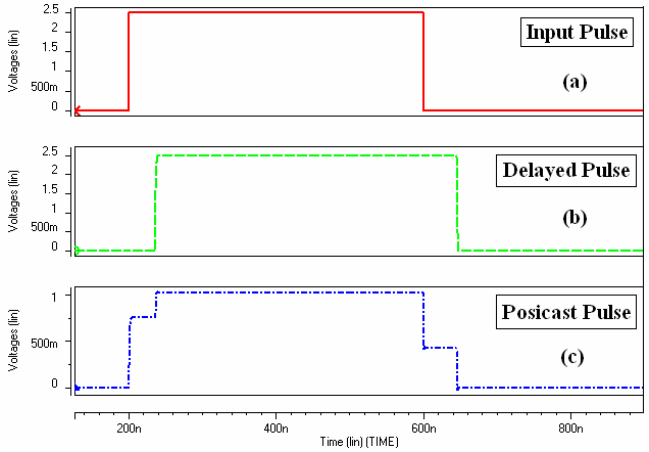

Figure 7. Adding input step pulse and delayed pulse to generate Posicast pulse

For realization of the adder circuit's operation method, the simulation result of adding step pulse and delayed pulse by adder circuit (Figure 6) is shown in Figure 7(c). Using of proposed adder circuit has several advantages. First, it is a so simple circuit with suitable operation. Second, it has a flexible design which allows the user to adjust the middle and high voltage level of Posicast pulse separately by changing the sizing of transistors of each path. The other feature of designed adder circuit is that changing the low voltage level of Posicast pulse from zero to a non-zero value is possible with adding a always-connected path from resistor R to VDD. Also, the mentioned non-zero value will be adjustable by changing the related transistor's sizing.

IV. Applying Posicast Pulse on Op-Amp

The schematic of a two-stage Op-Amp is presented in Figure 8. The step response of Op-Amp (Figure 9) has undesired vibrations in both positive and negative edges. The overshoot and settling time of positive edge is 25% and 205ns, respectively. Also, the negative edge response, has 24% overshoot with 253ns settling time. To cancel the oscillation, a posicast pulse is generated by proposed pre-shaper and is applied on Op-Amp. The Posicast pulse and the Op-Amp's response to Posicast pulse, is shown in Figure 10. One can see that, the oscillation is significantly decreased in both positive and negative edges. The overshoot of positive edges is decreased from 25% to 1% and the overshoot of negative edge is reached from 24% to 1%. Also, settling time of positive and negative edges is decreased from 205ns and 253ns to 34ns and 99ns respectively. These results realize the effectiveness of Posicast control in vibration reduction of under test Op-Amp.

For better comparison, the numerical results of simulating the step response and Posicast response of Op-Amp are presented in Table 1.

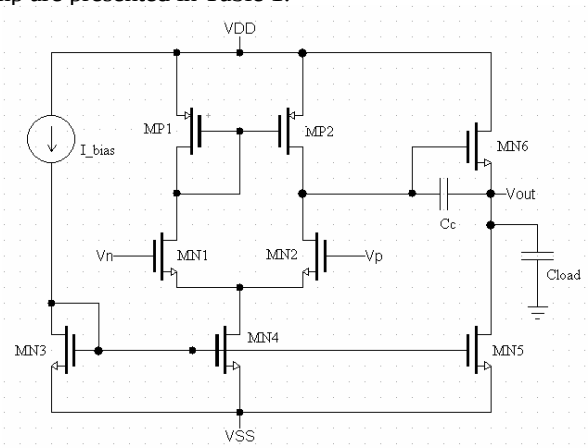

Figure 8. Schematic of a two-stage Op-Amp

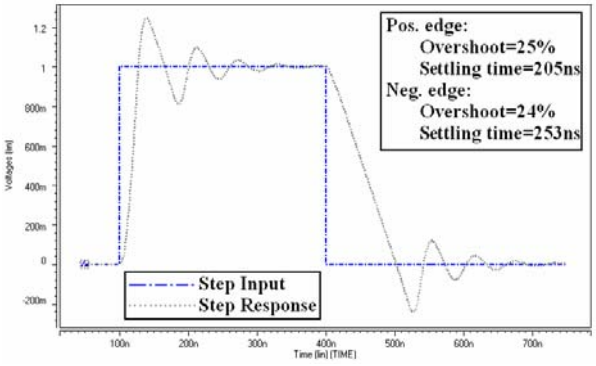

Figure 9. Step response of Op-Amp in Figure 8

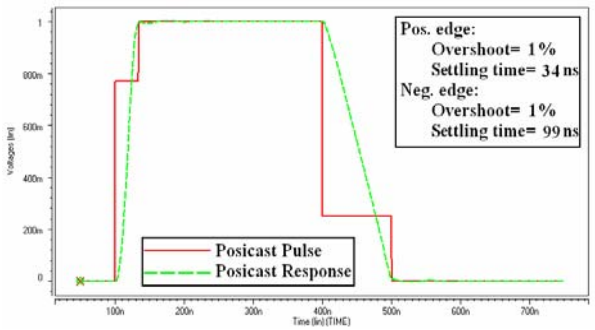

Figure 10. Posicast response of Op-Amp in Figure 8

TABLE I. SIMULATION RESULTS

Input Type		Overshoot	Improve	Settling time	Improve
Step	*Pos. edge*	25 %	-	205 ns	-
	Neg. edge	24 %	-	253 ns	-
Posicast	*Pos. edge*	1 %	96.0 %	34 ns	83.4%
	Neg. edge	1 %	95.8 %	99 ns	60.8 %

V. CONCLUSION

In this paper, electronic realization of Posicast control system is implemented to reduce vibration in Op-Amps. The effectiveness of using Posicast method on Op-Amps has been presented in [17][18].

A CMOS pre-shaper circuit is designed to shape the input step pulse into a desired Posicast pulse. The implemented pre-shaper circuit has several freedoms of action to regulate the voltage levels and timings of Posicast pulse.

The HSPICE simulations of applying the generated Posicast pulse on an Op-Amp show a meaningful reduction in both overshoot and settling time of under test system. The overshoot is reduced in positive edge from 25% to 1% and in negative edge from 24% to 1 % that shows more than 95% improvement. Also, the settling time is decreased from 205ns and 253ns to 34ns and 99ns in positive and negative edges respectively. Obviously, decreasing the overshoot and the settling time leads to more stability and speed of system.

REFERENCES

[1] Arpad Barna, Dan I. Porat, “Operational Amplifiers”, Whily Inter-Science, Second Edition, 1971.

[2] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G.Meyer, “Analysis and Design of Analog Integrated Circuits”, John wiley & Sons Inc., Foutrh Edition, 2001.

[3] Richard C. Dorf, Robert H. Bishop, “Modern Control Systems”, Addison-Wesley, Seventh Edition, 1995.

[4] “Feedback, Op Amps and Compensation”, Intersil Corporation, www.intersil.com/data/an/an9415.pdf.

[5] O. J. M. Smith, “Posicast control of damped oscillatory systems,” Proc. IRE, vol. 45, no. 9, pp. 1249–1255, Sep. 1957.

[6] Feedback *Control Systems*. New York: McGraw-Hill, 1958.

[7] G. Cook, “An application of half-cycle Posicast,” IEEE Trans. Autom. Control, vol. AC-11, no. 3, pp. 556–559, Jul. 1966.

[8] “Control of flexible structures via Posicast,” in Proc. Southeast. Symp. Syst. Theory, Knoxville, TN, Apr. 7–8, 1986, pp. 31–35.

[9] Q. Feng, R. M. Nelms, and J. Y. Hung, "The application of Posicast control to dc-dc converters," Proceedings of 35th Intersociety Energy Conversion Engineering Conference, Washington, DC, July 2002.

[10] Y. W. Li, B. Wu, N. Zargari, J. Wiseman, and D. Xu, “An effective method to suppress resonance in input LC filter of a PWM currentsource rectifier,” 5th CES/IEEE Int. Power Electr. And Motion Contr. Conf., vol. 2, Shanghai, China, Aug. 2006, p. 6.

[11] Qi Feng, R. M. Nelms, John Y. Hung, “Posicast-Based Digital Control of the Buck Converter”, IEEE Transaction on Industrial Electronics, Vol. 53, No. 3, Jun 2006

[12] J. Y. Hung, “Feedback control with Posicast,” IEEE Trans. Indust. Electr., vol. 50, no. 1, Feb. 2003, pp. 94-99.

[13] Akihiko Sugiki, Katsuhisa Furuta, “Posicast Control Design for Parameter-Uncertain Plants”, 45th IEEE Conference on Decision and Control, December 13-15, 2006, Manchester Grand Hyatt Hotel, San Diego, CA, USA

[14] P. C. Loh, C. J. Gajanayake, D. M. Vilathgamuwa, and F. Blaabjerg, “Evaluation of resonant damping techniques for Z-source current-type inverter,” 21st Annual IEEE Applied Power Electr. Conf. and Expos., Mar. 19-23, 2006, p. 7.

[15] J. Y. Hung, “Posicast Control Past and Present,” IEEE Multidisciplinary Eng. Educ., Vol. 2, No. 1, Mar 2007

[16] Shinji Hattori, Sharp K. Kaisha, “CMOS Pulse Delay Circuit”, United States Patent, Patent Number: 5459424, 1995.

[17] M. Rasoulzadeh, M.B. Ghaznavi-Ghoushchi, “A Novel Method for Oscillation Cancelling of CMOS Op-Amps Using Posicast”, Proceedings of The International Conference of Computing in Engineering, Science and Informatics (ICC2009), April 2-4, 2009, California, USA, Paper ID 100-51.

[18] M. Rasoulzadeh, MB. Ghaznavi-Ghoushchi, “Oscillation Controlled Electronic Systems Design Using Posicast-Based Pulse Pre-Shaping”, Submitted to the IEEE International Multitopic Conference 2009 (INMIC-2009), December 14-15, 2009, Islamabad, Pakistan.