

Design of a Divider Circuit for Complex Binary Numbers

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Abstract—Complex numbers play a very important role in various applications of electrical and computer engineering. These days, arithmetic operations dealing with these numbers rely on a “divide-and-conquer” technique wherein a complex number is broken into its real and imaginary parts and then, after representing each part in binary number system, operation is carried out on each part as if part of the real arithmetic. In an effort to reduce the number of arithmetic operations within the realm of complex arithmetic, binary number system with base $(-1+j)$, called complex binary number system (CBNS), has been proposed in the literature. This number system allows a complex number to be represented as single-unit instead of two separate units as in the traditional base-2 binary number system. Arithmetic circuits to perform addition, subtraction, multiplication, shift-left, and shift-right operations on complex numbers represented in CBNS have been previously presented in the literature. In this paper, we have presented the design procedure for a divider circuit involving CBNS.

Index Terms—Arithmetic circuits, complex binary number system, complex number, division.

I. INTRODUCTION

Complex numbers play a very important role in engineering applications such as digital signal processing and image processing. Thus design of an efficient approach to handle complex arithmetic will result in better performance in such applications. These days, arithmetic operations dealing with complex numbers involve, to a large extent, application of a “divide-and-conquer” technique, whereby a complex number is broken up into its real and imaginary parts and then operations are carried out on each part as if it were part of the real-arithmetic. Finally, the overall result of the complex operation is obtained by accumulation of the individual results. Efforts in defining binary numbers with bases other than 2, which facilitate one-unit representation of complex numbers, include work by Knuth [1], Penney [2], and Stepanenko [3]. Jamil [4] has presented a detailed analysis of $(-1+j)$ -base complex binary number system and elaborated

on how addition, subtraction, multiplication, and division of two such complex binary numbers can be accomplished. Designs of adder circuit [5], subtractor circuit [6], and multiplier circuit [7] have been previously presented in the literature. In this paper, we have outlined the procedure for the design of a nibble-size CBNS divider circuit.

This paper is organized as follows: In Section II, we present a brief introduction to $(-1+j)$ -base complex binary number system. This is followed, in Section III, by the description of division algorithm for CBNS. The truth table for the CBNS divider circuit is presented in Section IV and, in Section V, we have listed the minterms for the outputs of the divider circuit. Finally, summary and conclusion are given in Section VI, which is followed by Acknowledgment and References.

II. $(-1+j)$ -BASE COMPLEX BINARY NUMBER SYSTEM

The value of an n -bit binary number with base $(-1+j)$ can be written in the form of a power series as follows: $a_{n-1}(-1+j)^{n-1} + a_{n-2}(-1+j)^{n-2} + \dots + a_1(-1+j)^1 + a_0(-1+j)^0$ where the coefficients $a_{n-1}, a_{n-2}, \dots, a_1, a_0$ are binary (either 0 or 1). Using the algorithms presented in [4], we are able to represent a given complex number in CBNS format, e.g. $2010+j2010 = 1110100000001110100010001000_{base(-1+j)}$

III. DIVISION ALGORITHM FOR CBNS

The division algorithm is based on determining the reciprocal of the divisor (denominator) and then multiplying it with the dividend (numerator) according to the multiplication algorithm of CBNS [4]. The multiplication of two complex binary numbers is similar to multiplying two ordinary base-2 binary numbers, the only difference being in adding the intermediate results of multiplication wherein we follow the following rules for CBNS addition: $0+0=0$; $0+1=1$; $1+0=1$; $1+1=1100$ (note that $2_{10} = 1100_{base(-1+j)}$). The zero rule ($11+111=0$) plays an important role in reducing the number of summands resulting from intermediate multiplications.

Thus $(a+jb) \div (c+jd) = (a+jb)(c+jd)^{-1} = (a+jb)z$ where $z = w^{-1}$ and $w = c+jd$. We start with our initial approximation of z setting $z_0 = (-1+j)^k$ where k is obtained from the representation of w such that

$$w = \sum_{i=-\infty}^k a_i (-1+j)^{-i}$$

in which $a_k \equiv 1$ and $a_i \equiv 0$ for $i > k$. The successive approximations are then obtained by $z_{i+1} = z_i(2 - wz_i)$. If the values of z do not converge, we correct our initial

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approximation to $z_0 = j(-1+j)^{-k}$ which will definitely converge[8]. Having calculated the value of z , we just multiply it with $(a+jb)$ to obtain the result of division. In the following examples, for the sake of clarity, decimal numbers have been used to explain the converging process of the division algorithm.

Let $(a + jb) = 1 + j2$, and $w = 1 + j3$. Our calculations for approximation of $z = w^{-1}$ then begin as follows[4]:

$$1 + j3 = 1010_{base(-1+j)} = 1.(-1 + j)^3 + 0.(-1+j)^2 + 1.(-1 + j)^1 + 0.(-1+j)^0 \Rightarrow k = 3. \text{ Therefore,}$$

$$z_0 = (-1+j)^{-3} = 0.25 - j0.25 \quad z_1 = 0.125 - j0.375$$

$$z_2 = 0.09375 - j0.28125 \quad z_3 = 0.09960 - j0.2988$$

$$z_4 = 0.0999 - j0.2999 \quad z_5 = 0.1 - j0.3 \text{ (converging)}$$

Now, $0.1 - j0.3 = 0.001111001011110010111100..._{base(-1+j)}$

So $(1+j2) \div (1+j3) = (1+j2) \times (1+j3)^{-1}$

$$= 1110101_{base(-1+j)} \times 0.001111001011110010111100..._{base(-1+j)}$$

$$= 1.1111001011110010111100..._{base(-1+j)} = 0.7 - j0.1$$

As another example, let $w = -28 - j15$, then

$$-28 - j15 = 11011010011_{base(-1+j)}$$

$$= 1.(-1+j)^{10} + 1.(-1+j)^9 + 0.(-1+j)^8 + 1.(-1+j)^7 + 1.(-1+j)^6 +$$

$$0.(-1+j)^5 + 1.(-1+j)^4 + 0.(-1+j)^3 + 0.(-1+j)^2 + 1.(-1+j)^1 + 1.(-1+j)^0$$

$$\Rightarrow k = 10. \text{ We begin by choosing } z_0 = (-1+j)^{-10} = j0.03125 \text{ and}$$

find after nine iterations that it is not converging. So we correct our initial approximation to $z_0 = j(-1+j)^{-10} = -0.03125$

and find after five iterations that it converges to $z_5 = -0.02 + j0.014$. The converging value of z_5 can then be represented in CBNS and the result of division obtained as in previous example.

IV. TRUTH TABLE FOR CBNS DIVIDER CIRCUIT

The first step in designing any digital circuit is to obtain its truth table. For the divider circuit, we have assumed nibble size operands: 4-bit size dividend or numerator (operand A = $a_3a_2a_1a_0$ in the truth table) and 4-bit size divisor or denominator (operand B = $b_3b_2b_1b_0$ in the truth table). The division algorithm was programmed in MATLAB and the result of division is listed in the column labeled "R" in the truth table. Since the result of division operation contained small fractions for some sets of operands, we decided to round the result (RR column in the truth table) by converging numbers less than 0.5 to 0 and numbers greater than or equal to 0.5 to 1. This step was necessary in order to avoid representing fractional numbers in CBNS. Obviously, this procedure has produced some degree of error in the final result and, therefore, the resulting circuit can best be described as an approximate divider circuit. The rounded result (RR) was then represented in CBNS. The complete truth table for the approximate divider circuit is given in Table I.

V. BOOLEAN EXPRESSIONS FOR DIVIDER OUTPUTS

As can be seen for CBNS representation of the result obtained from division operation (Table I), we have a 10-bit output which has been labeled as $R_9R_8R_7R_6R_5R_4R_3R_2R_1R_0$. The Boolean expression for each output is a function of $(a_3, a_2, a_1, a_0, b_3, b_2, b_1, b_0)$ and consists of minterms listed in Table II.

VI. SUMMARY AND CONCLUSION

We have outlined the division algorithm for CBNS and presented a complete truth table of a nibble-size divider

circuit. From the truth table, we have obtained Boolean expressions in sum-of-minterms form for the outputs of this circuit. This circuit can now be implemented in the hardware and, in combination with adder, subtractor and multiplier circuits presented earlier in scientific literature, can assist in the design and implementation of an arithmetic unit for CBNS.

Table II. Minterms corresponding to Divider Outputs

Divider Output	Corresponding Minterms
R ₉	183
R ₈	158, 163, 190
R ₇	83, 94, 166, 182, 210, 242
R ₆	86, 149, 172, 188, 199, 212, 215
R ₅	30, 50, 92, 100, 103, 131, 146, 147, 178, 179, 200, 206, 211, 216, 222, 223, 227, 250
R ₄	37, 52, 55, 67, 74, 82, 104, 110, 111, 115, 134, 135, 148, 150, 151, 164, 167, 180, 214, 230, 246, 247
R ₃	35, 62, 70, 71, 84, 87, 118, 129, 140, 141, 142, 145, 156, 157, 159, 161, 168, 169, 174, 175, 177, 189, 191, 193, 209, 213, 220, 225, 236, 241, 252, 254
R ₂	18, 19, 36, 38, 39, 54, 65, 72, 76, 77, 78, 79, 81, 88, 89, 90, 91, 93, 95, 97, 101, 108, 113, 124, 126, 130, 162, 194, 195, 202, 218, 219, 226, 243
R ₁	20, 22, 23, 33, 40, 44, 46, 47, 49, 60, 66, 98, 99, 114, 132, 133, 154, 165, 173, 181, 196, 197, 198, 228, 229, 231, 244, 245
R ₀	17, 28, 34, 51, 68, 69, 85, 102, 116, 119, 136, 137, 138, 139, 143, 152, 153, 155, 170, 171, 184, 185, 186, 187, 204, 205, 207, 217, 221, 232, 238, 239, 248, 249, 251, 253, 255

ACKNOWLEDGMENT

We gratefully acknowledge the financial support provided by Sultan Qaboos University (Oman) for CBNS project through various internal research grants.

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Table I. Truth Table for a Nibble-Size Divider Circuit for Complex Binary Numbers
(NaN: Not a Number; Inf: Infinity)

Minterm	Operand A				Operand B				Actual Result (R)	Rounded Result (RR)	Rounded Result in CBNS R ₉ R ₈ R ₇ R ₆ R ₅ R ₄ R ₃ R ₂ R ₁ R ₀
	a ₃	a ₂	a ₁	a ₀	b ₃	b ₂	b ₁	b ₀			
0	0	0	0	0	0	0	0	0	NaN	NaN	NaN
1	0	0	0	0	0	0	0	1	0	0	000000000
2	0	0	0	0	0	0	1	0	0	0	000000000
3	0	0	0	0	0	0	1	1	0	0	000000000
4	0	0	0	0	0	1	0	0	0	0	000000000
5	0	0	0	0	0	1	0	1	0	0	000000000
6	0	0	0	0	0	1	1	0	0	0	000000000
7	0	0	0	0	0	1	1	1	0	0	000000000
8	0	0	0	0	1	0	0	0	0	0	000000000
9	0	0	0	0	1	0	0	1	0	0	000000000
10	0	0	0	0	1	0	1	0	0	0	000000000
11	0	0	0	0	1	0	1	1	0	0	000000000
12	0	0	0	0	1	1	0	0	0	0	000000000
13	0	0	0	0	1	1	0	1	0	0	000000000
14	0	0	0	0	1	1	1	0	0	0	000000000
15	0	0	0	0	1	1	1	1	0	0	000000000
16	0	0	0	1	0	0	0	0	Inf	Inf	NaN
17	0	0	0	1	0	0	0	1	1	1	000000001
18	0	0	0	1	0	0	1	0	-0.5000 - 0.5000i	-1.0000 - 1.0000i	000000110
19	0	0	0	1	0	0	1	1	0 - 1.0000i	0 - 1.0000i	000000111
20	0	0	0	1	0	1	0	0	0 + 0.5000i	0 + 1.0000i	000000111
21	0	0	0	1	0	1	0	1	0.2000 + 0.4000i	0	000000000
22	0	0	0	1	0	1	1	0	-0.5000 + 0.5000i	-1.0000 + 1.0000i	000000010
23	0	0	0	1	0	1	1	1	0 + 1.0000i	0 + 1.0000i	000000011
24	0	0	0	1	1	0	0	0	0.2500 - 0.2500i	0	000000000
25	0	0	0	1	1	0	0	1	0.2308 - 0.1538i	0	000000000
26	0	0	0	1	1	0	1	0	0.1000 - 0.3000i	0	000000000
27	0	0	0	1	1	0	1	1	0.1538 - 0.2308i	0	000000000
28	0	0	0	1	1	1	0	0	0.5	1	000000001
29	0	0	0	1	1	1	0	1	0.3333	0	000000000
30	0	0	0	1	1	1	1	0	0.5000 - 0.5000i	1.0000 - 1.0000i	000111010
31	0	0	0	1	1	1	1	1	0.4000 - 0.2000i	0	000000000
32	0	0	1	0	0	0	0	0	-Inf + Inf	-Inf + Inf	NaN
33	0	0	1	0	0	0	0	1	-1.0000 + 1.0000i	-1.0000 + 1.0000i	000000010
34	0	0	1	0	0	0	1	0	1	1	000000001
35	0	0	1	0	0	0	1	1	1.0000 + 1.0000i	1.0000 + 1.0000i	000001110
36	0	0	1	0	0	1	0	0	-0.5000 - 0.5000i	-1.0000 - 1.0000i	000000110
37	0	0	1	0	0	1	0	1	-0.6000 - 0.2000i	-1	000011101
38	0	0	1	0	0	1	1	0	0 - 1.0000i	0 - 1.0000i	000000111
39	0	0	1	0	0	1	1	1	-1.0000 - 1.0000i	-1.0000 - 1.0000i	000000110
40	0	0	1	0	1	0	0	0	0 + 0.5000i	0 + 1.0000i	000000011
41	0	0	1	0	1	0	0	1	-0.0769 + 0.3846i	0	000000000
42	0	0	1	0	1	0	1	0	0.2000 + 0.4000i	0	000000000
43	0	0	1	0	1	0	1	1	0.0769 + 0.3846i	0	000000000
44	0	0	1	0	1	1	0	0	-0.5000 + 0.5000i	-1.0000 + 1.0000i	000000010
45	0	0	1	0	1	1	0	1	-0.3333 + 0.3333i	0	000000000
46	0	0	1	0	1	1	1	0	0 + 1.0000i	0 + 1.0000i	000000011
47	0	0	1	0	1	1	1	1	-0.2000 + 0.6000i	0 + 1.0000i	000000011
48	0	0	1	1	0	0	0	0	NaN + Inf	NaN + Inf	NaN
49	0	0	1	1	0	0	0	1	0 + 1.0000i	0 + 1.0000i	000000011
50	0	0	1	1	0	0	1	0	0.5000 - 0.5000i	1.0000 - 1.0000i	000111010
51	0	0	1	1	0	0	1	1	1	1	000000001
52	0	0	1	1	0	1	0	0	-0.5	-1	000011101
53	0	0	1	1	0	1	0	1	-0.4000 + 0.2000i	0	000000000
54	0	0	1	1	0	1	1	0	-0.5000 - 0.5000i	-1.0000 - 1.0000i	000000110
55	0	0	1	1	0	1	1	1	-1	-1	000011101
56	0	0	1	1	1	0	0	0	0.2500 + 0.2500i	0	000000000
57	0	0	1	1	1	0	0	1	0.1538 + 0.2308i	0	000000000
58	0	0	1	1	1	0	1	0	0.3000 + 0.1000i	0	000000000
59	0	0	1	1	1	0	1	1	0.2308 + 0.1538i	0	000000000
60	0	0	1	1	1	1	0	0	0 + 0.5000i	0 + 1.0000i	000000011
61	0	0	1	1	1	1	0	1	0 + 0.3333i	0	000000000
62	0	0	1	1	1	1	1	0	0.5000 + 0.5000i	1.0000 + 1.0000i	000001110
63	0	0	1	1	1	1	1	1	0.2000 + 0.4000i	0	000000000

Table I. Truth Table for a Nibble-Size Divider Circuit for Complex Binary Numbers (*continued*)
(NaN: Not a Number; Inf: Infinity)

Minterm	Operand A				Operand B				Actual Result (R)	Rounded Result (RR)	Rounded Result in CBNS R ₉ R ₈ R ₇ R ₆ R ₅ R ₄ R ₃ R ₂ R ₁ R ₀
	a ₃	a ₂	a ₁	a ₀	b ₃	b ₂	b ₁	b ₀			
64	0	1	0	0	0	0	0	0	NaN - Inf	NaN - Inf	NaN
65	0	1	0	0	0	0	0	1	0 - 2.0000i	0 - 2.0000i	000000100
66	0	1	0	0	0	0	1	0	-1.0000 + 1.0000i	-1.0000 + 1.0000i	000000010
67	0	1	0	0	0	0	1	1	-2	-2	000001100
68	0	1	0	0	0	1	0	0	1	1	000000001
69	0	1	0	0	0	1	0	1	0.8000 - 0.4000i	1	000000001
70	0	1	0	0	0	1	1	0	1.0000 + 1.0000i	1.0000 + 1.0000i	000001110
71	0	1	0	0	0	1	1	1	2	2	000001100
72	0	1	0	0	1	0	0	0	-0.5000 - 0.5000i	-1.0000 - 1.0000i	000000110
73	0	1	0	0	1	0	0	1	-0.3077 - 0.4615i	0	000000000
74	0	1	0	0	1	0	1	0	-0.6000 - 0.2000i	-1	000001101
75	0	1	0	0	1	0	1	1	-0.4615 - 0.3077i	0	000000000
76	0	1	0	0	1	1	0	0	0 - 1.0000i	0 - 1.0000i	000000011
77	0	1	0	0	1	1	0	1	0 - 0.6667i	0 - 1.0000i	000000011
78	0	1	0	0	1	1	1	0	-1.0000 - 1.0000i	-1.0000 - 1.0000i	000000010
79	0	1	0	0	1	1	1	1	-0.4000 - 0.8000i	0 - 1.0000i	000000011
80	0	1	0	1	0	0	0	0	Inf - Inf	Inf - Inf	NaN
81	0	1	0	1	0	0	0	1	1.0000 - 2.0000i	1.0000 - 2.0000i	000000010
82	0	1	0	1	0	0	1	0	-1.5000 + 0.5000i	-2.0000 + 1.0000i	000001111
83	0	1	0	1	0	0	1	1	-2.0000 - 1.0000i	-2.0000 - 1.0000i	001110101
84	0	1	0	1	0	1	0	0	1.0000 + 0.5000i	1.0000 + 1.0000i	000000110
85	0	1	0	1	0	1	0	1	1	1	000000001
86	0	1	0	1	0	1	1	0	0.5000 + 1.5000i	1.0000 + 2.0000i	000111010
87	0	1	0	1	0	1	1	1	2.0000 + 1.0000i	2.0000 + 1.0000i	000000111
88	0	1	0	1	1	0	0	0	-0.2500 - 0.7500i	0 - 1.0000i	000000011
89	0	1	0	1	1	0	0	1	-0.0769 - 0.6154i	0 - 1.0000i	000000011
90	0	1	0	1	1	0	1	0	-0.5000 - 0.5000i	-1.0000 - 1.0000i	000000010
91	0	1	0	1	1	0	1	1	-0.3077 - 0.5385i	0 - 1.0000i	000000011
92	0	1	0	1	1	1	0	0	0.5000 - 1.0000i	1.0000 - 1.0000i	000011010
93	0	1	0	1	1	1	0	1	0.3333 - 0.6667i	0 - 1.0000i	000000011
94	0	1	0	1	1	1	1	0	-0.5000 - 1.5000i	-1.0000 - 2.0000i	001110100
95	0	1	0	1	1	1	1	1	0 - 1.0000i	0 - 1.0000i	000000011
96	0	1	1	0	0	0	0	0	-Inf - Inf	-Inf - Inf	NaN
97	0	1	1	0	0	0	0	1	-1.0000 - 1.0000i	-1.0000 - 1.0000i	000000010
98	0	1	1	0	0	0	1	0	0 + 1.0000i	0 + 1.0000i	000000001
99	0	1	1	0	0	0	1	1	-1.0000 + 1.0000i	-1.0000 + 1.0000i	000000010
100	0	1	1	0	0	1	0	0	0.5000 - 0.5000i	1.0000 - 1.0000i	000011010
101	0	1	1	0	0	1	0	1	0.2000 - 0.6000i	0 - 1.0000i	000000011
102	0	1	1	0	0	1	1	0	1	1	000000001
103	0	1	1	0	0	1	1	1	1.0000 - 1.0000i	1.0000 - 1.0000i	000011010
104	0	1	1	0	1	0	0	0	-0.5	-1	000001101
105	0	1	1	0	1	0	0	1	-0.3846 - 0.0769i	0	000000000
106	0	1	1	0	1	0	1	0	-0.4000 + 0.2000i	0	000000000
107	0	1	1	0	1	0	1	1	-0.3846 + 0.0769i	0	000000000
108	0	1	1	0	1	1	0	0	-0.5000 - 0.5000i	-1.0000 - 1.0000i	000000010
109	0	1	1	0	1	1	0	1	-0.3333 - 0.3333i	0	000000000
110	0	1	1	0	1	1	1	0	-1	-1	000001101
111	0	1	1	0	1	1	1	1	-0.6000 - 0.2000i	-1	000001101
112	0	1	1	1	0	0	0	0	NaN - Inf	NaN - Inf	NaN
113	0	1	1	1	0	0	0	1	0 - 1.0000i	0 - 1.0000i	000000011
114	0	1	1	1	0	0	1	0	-0.5000 + 0.5000i	-1.0000 + 1.0000i	000000010
115	0	1	1	1	0	0	1	1	-1	-1	000001101
116	0	1	1	1	0	1	0	0	0.5	1	000000001
117	0	1	1	1	0	1	0	1	0.4000 - 0.2000i	0	000000000
118	0	1	1	1	0	1	1	0	0.5000 + 0.5000i	1.0000 + 1.0000i	000000110
119	0	1	1	1	0	1	1	1	1	1	000000001
120	0	1	1	1	1	0	0	0	-0.2500 - 0.2500i	0	000000000
121	0	1	1	1	1	0	0	1	-0.1538 - 0.2308i	0	000000000
122	0	1	1	1	1	0	1	0	-0.3000 - 0.1000i	0	000000000
123	0	1	1	1	1	0	1	1	-0.2308 - 0.1538i	0	000000000
124	0	1	1	1	1	1	0	0	0 - 0.5000i	0 - 1.0000i	000000011
125	0	1	1	1	1	1	0	1	0 - 0.3333i	0	000000000
126	0	1	1	1	1	1	1	0	-0.5000 - 0.5000i	-1.0000 - 1.0000i	000000010
127	0	1	1	1	1	1	1	1	-0.2000 - 0.4000i	0	000000000

Table I. Truth Table for a Nibble-Size Divider Circuit for Complex Binary Numbers (*continued*)
(NaN: Not a Number; Inf: Infinity)

Minterm	Operand A				Operand B				Actual Result (R)	Rounded Result (RR)	Rounded Result in CBNS R ₉ R ₈ R ₇ R ₆ R ₅ R ₄ R ₃ R ₂ R ₁ R ₀
	a ₃	a ₂	a ₁	a ₀	b ₃	b ₂	b ₁	b ₀			
128	1	0	0	0	0	0	0	0	Inf + Inf	Inf + Inf	NaN
129	1	0	0	0	0	0	0	1	2.0000 + 2.0000i	2.0000 + 2.0000i	0000001000
130	1	0	0	0	0	0	1	0	0 - 2.0000i	0 - 2.0000i	0000000100
131	1	0	0	0	0	0	1	1	2.0000 - 2.0000i	2.0000 - 2.0000i	0000111000
132	1	0	0	0	0	1	0	0	-1.0000 + 1.0000i	-1.0000 + 1.0000i	0000000010
133	1	0	0	0	0	1	0	1	-0.4000 + 1.2000i	0 + 1.0000i	0000000011
134	1	0	0	0	0	1	1	0	-2	-2	0000011100
135	1	0	0	0	0	1	1	1	-2.0000 + 2.0000i	-2.0000 + 2.0000i	0000011000
136	1	0	0	0	1	0	0	0	1	1	0000000001
137	1	0	0	0	1	0	0	1	0.7692 + 0.1538i	1	0000000001
138	1	0	0	0	1	0	1	0	0.8000 - 0.4000i	1	0000000001
139	1	0	0	0	1	0	1	1	0.7692 - 0.1538i	1	0000000001
140	1	0	0	0	1	1	0	0	1.0000 + 1.0000i	1.0000 + 1.0000i	0000001110
141	1	0	0	0	1	1	0	1	0.6667 + 0.6667i	1.0000 + 1.0000i	0000001110
142	1	0	0	0	1	1	1	0	2	2	0000001100
143	1	0	0	0	1	1	1	1	1.2000 + 0.4000i	1	0000000001
144	1	0	0	1	0	0	0	0	Inf + Inf	Inf + Inf	NaN
145	1	0	0	1	0	0	0	1	3.0000 + 2.0000i	3.0000 + 2.0000i	0000001001
146	1	0	0	1	0	0	1	0	-0.5000 - 2.5000i	-1.0000 - 3.0000i	0000110010
147	1	0	0	1	0	0	1	1	2.0000 - 3.0000i	2.0000 - 3.0000i	0000111111
148	1	0	0	1	0	1	0	0	-1.0000 + 1.5000i	-1.0000 + 2.0000i	0000011001
149	1	0	0	1	0	1	0	1	-0.2000 + 1.6000i	0 + 2.0000i	0001110100
150	1	0	0	1	0	1	1	0	-2.5000 + 0.5000i	-3.0000 + 1.0000i	0000011110
151	1	0	0	1	0	1	1	1	-2.0000 + 3.0000i	-2.0000 + 3.0000i	0000011011
152	1	0	0	1	1	0	0	0	1.2500 - 0.2500i	1	0000000001
153	1	0	0	1	1	0	0	1	1	1	0000000001
154	1	0	0	1	1	0	1	0	0.9000 - 0.7000i	1.0000 - 1.0000i	0000000010
155	1	0	0	1	1	0	1	1	0.9231 - 0.3846i	1	0000000001
156	1	0	0	1	1	1	0	0	1.5000 + 1.0000i	2.0000 + 1.0000i	0000001111
157	1	0	0	1	1	1	0	1	1.0000 + 0.6667i	1.0000 + 1.0000i	0000001110
158	1	0	0	1	1	1	1	0	2.5000 - 0.5000i	3.0000 - 1.0000i	0111010110
159	1	0	0	1	1	1	1	1	1.6000 + 0.2000i	2	0000001100
160	1	0	1	0	0	0	0	0	Inf + Inf	Inf + Inf	NaN
161	1	0	1	0	0	0	0	1	1.0000 + 3.0000i	1.0000 + 3.0000i	0000001010
162	1	0	1	0	0	0	1	0	1.0000 - 2.0000i	1.0000 - 2.0000i	0000000101
163	1	0	1	0	0	0	1	1	3.0000 - 1.0000i	3.0000 - 1.0000i	0111010110
164	1	0	1	0	0	1	0	0	-1.5000 + 0.5000i	-2.0000 + 1.0000i	0000011111
165	1	0	1	0	0	1	0	1	-1.0000 + 1.0000i	-1.0000 + 1.0000i	0000000010
166	1	0	1	0	0	1	1	0	-2.0000 - 1.0000i	-2.0000 - 1.0000i	0011101011
167	1	0	1	0	0	1	1	1	-3.0000 + 1.0000i	-3.0000 + 1.0000i	0000011110
168	1	0	1	0	1	0	0	0	1.0000 + 0.5000i	1.0000 + 1.0000i	0000001110
169	1	0	1	0	1	0	0	1	0.6923 + 0.5385i	1.0000 + 1.0000i	0000001110
170	1	0	1	0	1	0	1	0	1	1	0000000001
171	1	0	1	0	1	0	1	1	0.8462 + 0.2308i	1	0000000001
172	1	0	1	0	1	1	0	0	0.5000 + 1.5000i	1.0000 + 2.0000i	0001110101
173	1	0	1	0	1	1	0	1	0.3333 + 1.0000i	0 + 1.0000i	0000000011
174	1	0	1	0	1	1	1	0	2.0000 + 1.0000i	2.0000 + 1.0000i	0000001111
175	1	0	1	0	1	1	1	1	1.0000 + 1.0000i	1.0000 + 1.0000i	0000001110
176	1	0	1	1	0	0	0	0	Inf + Inf	Inf + Inf	NaN
177	1	0	1	1	0	0	0	1	2.0000 + 3.0000i	2.0000 + 3.0000i	0000001011
178	1	0	1	1	0	0	1	0	0.5000 - 2.5000i	1.0000 - 3.0000i	0000111110
179	1	0	1	1	0	0	1	1	3.0000 - 2.0000i	3.0000 - 2.0000i	0000111001
180	1	0	1	1	0	1	0	0	-1.5000 + 1.0000i	-2.0000 + 1.0000i	0000011111
181	1	0	1	1	0	1	0	1	-0.8000 + 1.4000i	-1.0000 + 1.0000i	0000000010
182	1	0	1	1	0	1	1	0	-2.5000 - 0.5000i	-3.0000 - 1.0000i	0011101010
183	1	0	1	1	0	1	1	1	-3.0000 + 2.0000i	-3.0000 + 2.0000i	1110100101
184	1	0	1	1	1	0	0	0	1.2500 + 0.2500i	1	0000000001
185	1	0	1	1	1	0	0	1	0.9231 + 0.3846i	1	0000000001
186	1	0	1	1	1	0	1	0	1.1000 - 0.3000i	1	0000000001
187	1	0	1	1	1	0	1	1	1	1	0000000001
188	1	0	1	1	1	1	0	0	1.0000 + 1.5000i	1.0000 + 2.0000i	0001110101
189	1	0	1	1	1	1	0	1	0.6667 + 1.0000i	1.0000 + 1.0000i	0000001110
190	1	0	1	1	1	1	1	0	2.5000 + 0.5000i	3.0000 + 1.0000i	0111010010
191	1	0	1	1	1	1	1	1	1.4000 + 0.8000i	1.0000 + 1.0000i	0000001110

Table I. Truth Table for a Nibble-Size Divider Circuit for Complex Binary Numbers (*continued*)
(NaN: Not a Number; Inf: Infinity)

Minterm	Operand A				Operand B				Actual Result (R)	Rounded Result (RR)	Rounded Result in CBNS $R_9R_8R_7R_6R_5R_4R_3R_2R_1R_0$
	a_3	a_2	a_1	a_0	b_3	b_2	b_1	b_0			
192	1	1	0	0	0	0	0	0	Inf	Inf	NaN
193	1	1	0	0	0	0	0	1	2	2	000001100
194	1	1	0	0	0	0	1	0	-1.0000 - 1.0000i	-1.0000 - 1.0000i	000000110
195	1	1	0	0	0	0	1	1	0 - 2.0000i	0 - 2.0000i	000000100
196	1	1	0	0	0	1	0	0	0 + 1.0000i	0 + 1.0000i	000000011
197	1	1	0	0	0	1	0	1	0.4000 + 0.8000i	0 + 1.0000i	000000011
198	1	1	0	0	0	1	1	0	-1.0000 + 1.0000i	-1.0000 + 1.0000i	000000010
199	1	1	0	0	0	1	1	1	0 + 2.0000i	0 + 2.0000i	0001110100
200	1	1	0	0	1	0	0	0	0.5000 - 0.5000i	1.0000 - 1.0000i	0000111010
201	1	1	0	0	1	0	0	1	0.4615 - 0.3077i	0	000000000
202	1	1	0	0	1	0	1	0	0.2000 - 0.6000i	0 - 1.0000i	000000011
203	1	1	0	0	1	0	1	1	0.3077 - 0.4615i	0	000000000
204	1	1	0	0	1	1	0	0	1	1	000000001
205	1	1	0	0	1	1	0	1	0.6667	1	000000001
206	1	1	0	0	1	1	1	0	1.0000 - 1.0000i	1.0000 - 1.0000i	0000111010
207	1	1	0	0	1	1	1	1	0.8000 - 0.4000i	1	000000001
208	1	1	0	1	0	0	0	0	Inf	Inf	NaN
209	1	1	0	1	0	0	0	1	3	3	000001101
210	1	1	0	1	0	0	1	0	-1.5000 - 1.5000i	-2.0000 - 2.0000i	0011101000
211	1	1	0	1	0	0	1	1	0 - 3.0000i	0 - 3.0000i	0000110011
212	1	1	0	1	0	1	0	0	0 + 1.5000i	0 + 2.0000i	0001110100
213	1	1	0	1	0	1	0	1	0.6000 + 1.2000i	1.0000 + 1.0000i	0000001110
214	1	1	0	1	0	1	1	0	-1.5000 + 1.5000i	-2.0000 + 2.0000i	0000011000
215	1	1	0	1	0	1	1	1	0 + 3.0000i	0 + 3.0000i	0001110111
216	1	1	0	1	1	0	0	0	0.7500 - 0.7500i	1.0000 - 1.0000i	0000111010
217	1	1	0	1	1	0	0	1	0.6923 - 0.4615i	1	000000001
218	1	1	0	1	1	0	1	0	0.3000 - 0.9000i	0 - 1.0000i	000000011
219	1	1	0	1	1	0	1	1	0.4615 - 0.6923i	0 - 1.0000i	000000011
220	1	1	0	1	1	1	0	0	1.5	2	000001100
221	1	1	0	1	1	1	0	1	1	1	000000001
222	1	1	0	1	1	1	1	0	1.5000 - 1.5000i	2.0000 - 2.0000i	0000111000
223	1	1	0	1	1	1	1	1	1.2000 - 0.6000i	1.0000 - 1.0000i	0000111010
224	1	1	1	0	0	0	0	0	Inf + Inf	Inf + Inf	NaN
225	1	1	1	0	0	0	0	1	1.0000 + 1.0000i	1.0000 + 1.0000i	0000001110
226	1	1	1	0	0	0	1	0	0 - 1.0000i	0 - 1.0000i	000000011
227	1	1	1	0	0	0	1	1	1.0000 - 1.0000i	1.0000 - 1.0000i	0000111010
228	1	1	1	0	0	1	0	0	-0.5000 + 0.5000i	-1.0000 + 1.0000i	000000010
229	1	1	1	0	0	1	0	1	-0.2000 + 0.6000i	0 + 1.0000i	000000011
230	1	1	1	0	0	1	1	0	-1	-1	000011101
231	1	1	1	0	0	1	1	1	-1.0000 + 1.0000i	-1.0000 + 1.0000i	000000010
232	1	1	1	0	1	0	0	0	0.5	1	000000001
233	1	1	1	0	1	0	0	1	0.3846 + 0.0769i	0	000000000
234	1	1	1	0	1	0	1	0	0.4000 - 0.2000i	0	000000000
235	1	1	1	0	1	0	1	1	0.3846 - 0.0769i	0	000000000
236	1	1	1	0	1	1	0	0	0.5000 + 0.5000i	1.0000 + 1.0000i	0000011110
237	1	1	1	0	1	1	0	1	0.3333 + 0.3333i	0	000000000
238	1	1	1	0	1	1	1	0	1	1	000000001
239	1	1	1	0	1	1	1	1	0.6000 + 0.2000i	1	000000001
240	1	1	1	1	0	0	0	0	Inf + Inf	Inf + Inf	NaN
241	1	1	1	1	0	0	0	1	2.0000 + 1.0000i	2.0000 + 1.0000i	000001111
242	1	1	1	1	0	0	1	0	-0.5000 - 1.5000i	-1.0000 - 2.0000i	0011101001
243	1	1	1	1	0	0	1	1	1.0000 - 2.0000i	1.0000 - 2.0000i	000000101
244	1	1	1	1	0	1	0	0	-0.5000 + 1.0000i	-1.0000 + 1.0000i	000000010
245	1	1	1	1	0	1	0	1	0 + 1.0000i	0 + 1.0000i	000000011
246	1	1	1	1	0	1	1	0	-1.5000 + 0.5000i	-2.0000 + 1.0000i	000011111
247	1	1	1	1	0	1	1	1	-1.0000 + 2.0000i	-1.0000 + 2.0000i	000011001
248	1	1	1	1	1	0	0	0	0.7500 - 0.2500i	1	000000001
249	1	1	1	1	1	0	0	1	0.6154 - 0.0769i	1	000000001
250	1	1	1	1	1	0	1	0	0.5000 - 0.5000i	1.0000 - 1.0000i	0000111010
251	1	1	1	1	1	0	1	1	0.5385 - 0.3077i	1	000000001
252	1	1	1	1	1	1	0	0	1.0000 + 0.5000i	1.0000 + 1.0000i	000001110
253	1	1	1	1	1	1	0	1	0.6667 + 0.3333i	1	000000001
254	1	1	1	1	1	1	1	0	1.5000 - 0.5000i	2.0000 - 1.0000i	000001111
255	1	1	1	1	1	1	1	1	1	1	000000001