Investigation of Gate Underlap Design on Linearity of Operational Transconductance Amplifier (OTA)

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Abstract*—The significance of optimization of gate–source/drain extension region (also known as underlap design) in double gate (DG) silicon-on-insulator (SOI) FETs to improve the linearity performance of a low power folded cascode operational transconductance amplifier (OTA) is described. Based on a new figure-of-merit (*FoM*) involving A_V, linearity, f_T and dc power consumption P_{DC}, the paper presents guideline for optimum design for underlap spacer *s* and film thickness T_{si} to maximize the performance of OTA. It has been shown that *FoM* exhibited by an underlap DG MOSFET OTA gives significantly higher value (≅ 9) compared to a conventional single gate bulk MOSFET OTA. This is due to a combination of both higher f_T, and higher gain A_V for the same *linearity* at low power consumption of 360μW. With gate length scaling, *FoM* continues to improve, primarily due to higher value of f_T. A scaled bulk MOSFET OTA exhibits similar but much smaller enhancement in trend for *FoM

Index Terms—Double Gate, Operational Transconductance Amplifier, Analog Performance, Low power, Non-Linearity, Underlap Design.

I. Introduction

Modern wireless communication systems require high performance analog front-end and analog filters circuits to cater for the need of higher speed, large bandwidth and high linearity [1]. When it comes to analog filter implementation with electronic tenability, operational transconductance amplifiers (OTAs) have been proven to be the most widely used candidate [2]. It is widely accepted that double gate (DG) MOSFETs are promising candidates for realization of analog filters used in modern wireless systems, where device must be very precise [3]. Such devices with source/drain extension (SDE) region engineering have been used in the design of OTA and their advantages for linear mode of operation for low power analog applications have been advocated [4]. But non-linearity study for such OTA circuit has not been carried out, which is essential to realize emerging wireless systems. This paper extends the work presented in [4] by incorporating non-linearity study as described in section II. By using mixed mode simulation [5], the effect of underlap channel design on voltage gain A_V, unity gain bandwidth f_T and *linearity* of OTA circuit shown in Figure 1 has been evaluated. Table 1 gives the summary of aspect ratio (W/L) of various transistors used in OTA design shown in Figure 1. Device design is analyzed in terms of the spacer *s* and film thickness T_{si} that are the key design parameter for OTA circuit based on underlap channel devices.

Based on a new figure-of-merit (*FoM*) as discussed in section II, the performance of a DG MOSFET OTA is compared with that realized with a single gate bulk MOSFET technology. Our results demonstrate that an OTA designed with underlap DG MOSFETs exhibits superior performance as compared to those realized in single gate bulk MOSFET devices. A design criterion to select underlap region parameters is proposed for achieving optimal *FoM* value of OTA.

II. Figure-of-merit (FoM)

In order to compare the different implementations of OTAs, a new figure-of-merit (*FoM*) involving A_V, *linearity*, f_T and dc power consumption P_{DC} has been proposed, which can be defined as:

$$FoM = \frac{Linearity \times A_v \times f_T}{P_{DC}} \quad (1)$$

When differential pair is used in the design of OTA, even-order harmonics are significantly suppressed but odd-order harmonics; especially 3rd harmonics are still significant unwanted harmonic [6]. Taking this fact into account, linearity in this work has been defined as given (2).

Table 1: OTA Parameters

V_{DD}	0.6V	V_{SS}	-0.6V
M_1-M_2	176	M_{11}	20
M_3-M_4	60	M_{12}	120
M_5-M_6	4.5	M_{13}-M_{14}	35/4
M_7-M_8	120	M_{15}	35/4
M_9-M_{10}	27	M_{16}-M_{17}	88

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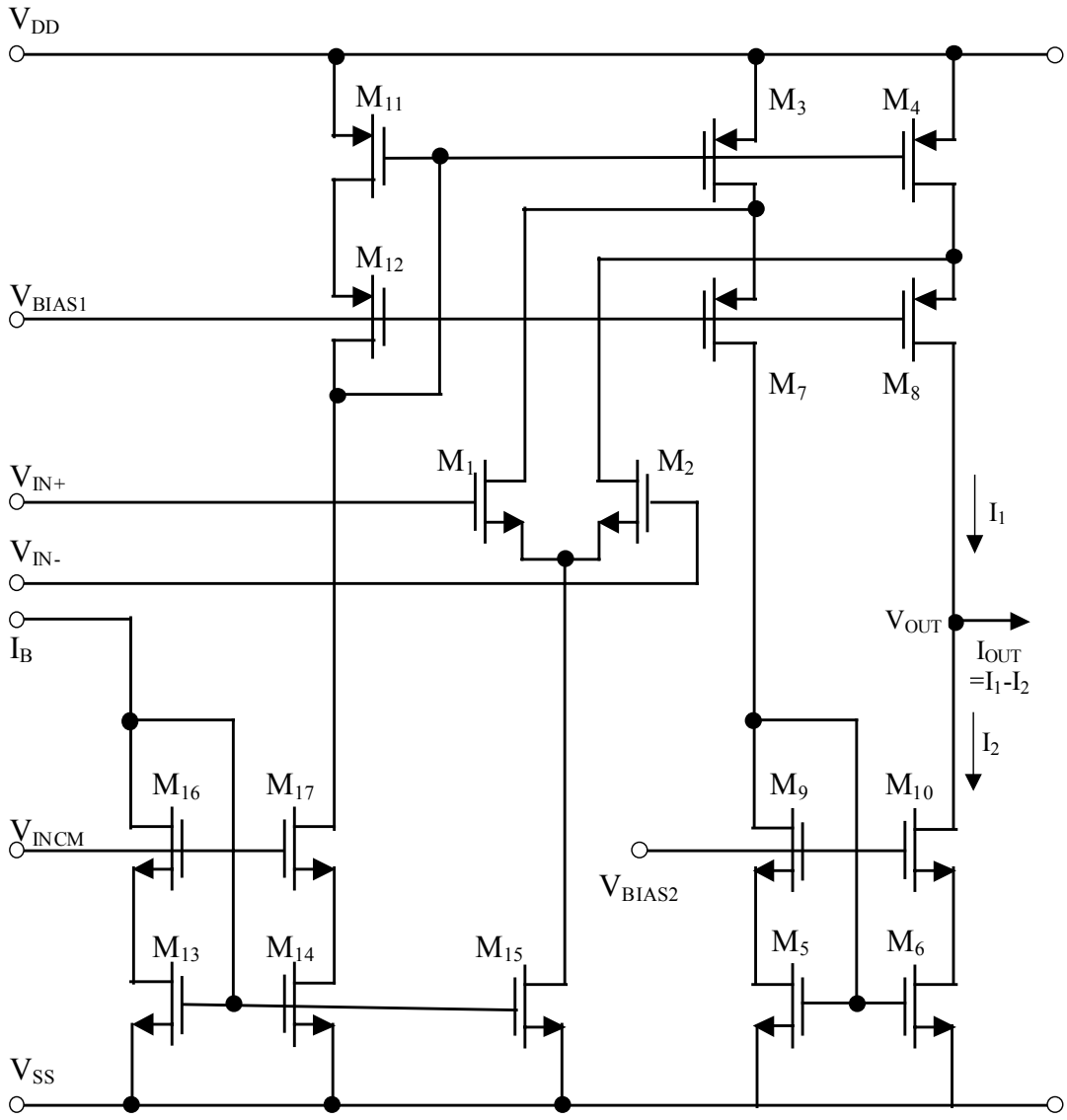

Figure 1. Circuit diagram of the folded cascoded operational transconductance amplifier (OTA) [3]. Devices M_1 and M_2 form the nMOS differential pair with M_3 and M_4 as current sources. M_5 and M_6 are current mirror devices and M_7–M_{10} represents cascode devices. The voltage at V_{INCM} is connected externally to ground and provides a low-voltage, cascode gate bias for M_{16}–M_{17}. When the OTA inputs V_{IN+} and V_{IN-} are at a common-mode voltage equal to ground, the bias current in the M_{15} input pair current source is replicated from the current source in the M_{13} bias reference because both devices have equal drain–source voltages. The voltage at V_{BIAS1} provides a low-voltage, cascode gate voltage for M_7, M_8 and M_{12}, while the voltage at V_{BIAS2} provides the same for M_9 and M_{10}. V_{BIAS1} connects to an external pMOS, diode-connected device connected to V_{DD}, whereas V_{BIAS2} connects to an external nMOS, diode-connected device connected to V_{SS}

$$Linearity = \frac{P_{fund}}{P_{3rd\_order\_harmonic}} \quad (2)$$

Where $P_{3rd\_order\_harmonic}$ is the third-order harmonic power and P_{fund} is fundamental power. This measure of linearity is easier to evaluate at specific power level than more commonly used third-order intercept IP_3 [7]. Non-linear effects are traditionally investigated by evaluating higher order derivatives of transconductance g_m with respect to gate voltage, under dc mode of operation [8] [9]. But such a technique ignores the non-linearity contribution from parasitic resistance and capacitance and underestimates the overall circuit non-linearity, especially when the frequency of operation is high [10]. Therefore, in this work Mixed mode simulation [5], which combines the merits of device and circuit simulation, is used to simulate the linearity of OTA circuit shown in Figure 1. In this approach the basic physical structure of each double gate SOI transistor comprising gate oxide, thin silicon, buried oxide and source/drain doping profile is precisely modelled in the conventional manner, while parasitic effects of contact resistance R_{CON}, gate resistance R_G and overlap capacitance C_{OVL} are added as external lumped elements as shown in Figure 2. Calculation of these parasitic elements has been carried using technique describe in [11] [12]. Mixedmode simulation [5] avoids the requirement for a detailed SPICE model, and therefore, a very useful predictive tool for nano-scale technologies when an accurate SPICE model is not available. For linearity calculation in (2), the time-domain waveform of output voltage V_{OUT} in Figure 1 under single tone 1 GHz differential excitation of $20mV_{p\text{-}p}$ amplitude was simulated. Linearity was determined by transforming voltage time-domain waveforms into frequency domain using Fast Fourier Transform and then determining the required power ratio.

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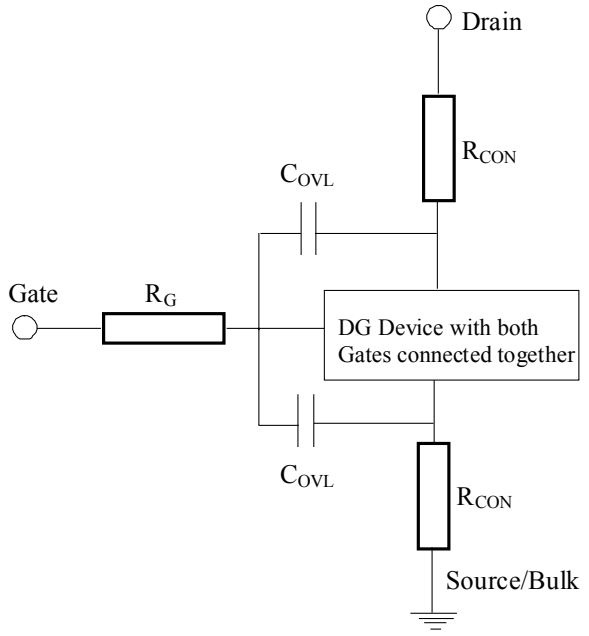

Figure 2. Schematic diagram for mixed mode simulation, where intrinsic device is discretised using ATLAS and extrinsic parasitics R_G , R_{CON} and C_{OVL} are added as lumped elements.

III. Simulation

The OTA circuit shown in Figure 1 is based on midgap gate DG FETs on undoped silicon (Figure 3(a)), where each device is defined by specific geometric parameters, gate length (L_G), oxide thickness (T_{OX}), silicon film thickness (T_{si}) and spacer length (s). Source/drain (S/D) region was modelled by a gate underlap with a Gaussian S/D profile with lateral straggle σ, across a spacer s defined by the distance from the start of the profile to the edge of the gate, as shown in Figure 3(b). The lateral straggle σ, is directly related to spacer length s and d the inverse source/drain doping gradient in nm/decade evaluated at the gate edge, by $\sigma = \sqrt{2sd/\ln(10)}$ [13][14]. In underlap design, S/D profiles are designed with s/σ >1.8, such that the extension region doping does not significantly extend beyond the gate edge. Indeed in the limit if $s/\sigma = 3$ (as in Figure 3 (b)), the channel region directly under the gate is free from dopants [14], so the effective channel length (L_{EFF}), defined by depletion layer edges in source and drain) exceeds the gate length (L_G). Comparative simulations in this paper, examining the effectiveness of gate underlap, have therefore been carried out using abrupt junction with gate length equal to L_{EFF}.

The film thickness (T_{si}) and spacer s were varied from $0.5L_G$ to $1.25L_G$, $0.5L_G$ to $1.25L_G$, respectively to determine their optimum value in order to maximize *FoM* in (2). The simulations have been performed with established physical models, but neglect quantum effects, as they will be negligible in weak inversion when silicon film thickness exceeds 10nm.

IV. Results and Discussion

A. How to maximize Figure-of-Merits?

In order to maximize *FoM* in (1) for the OTA circuit shown in Figure 1, the optimal device structure for specific gate length and oxide thickness is to be designed. The sensitivity

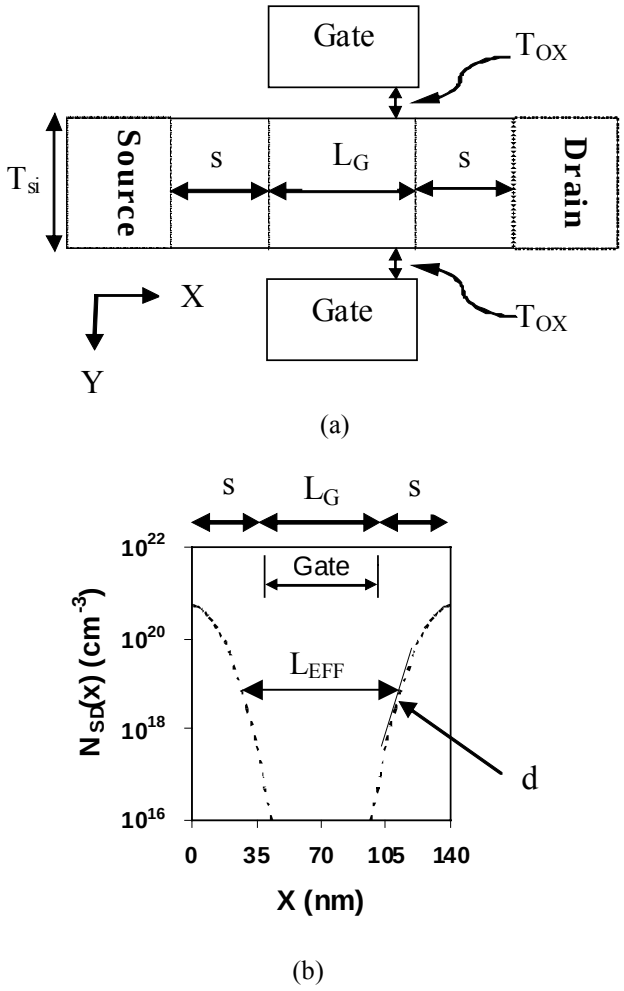

Figure 3 (a) DG structure (b) Lateral doping profile along the channel with L_G = 60nm ; s/σ=3.

of the device physical parameters spacer variation s and film thickness T_{si} at L_G = 60 nm have been investigated to maximize *FoM*. Figure 4 and Figure 5 show the plot of optimal *FoM* at 360μW dc power consumption under single-tone excitation f_1 = 1 GHz as a function of spacer s and film thickness T_{si}. With increase in spacer width ((Figure 4(b)), *FoM* increase until $s \leq L_G$, whereas $T_{si} = 0.75L_G$ (Figure 5(b)) is required in order to maximize *FoM* of OTA.

For comparison with bulk technology, BSIM4 [15] is used and *FoM* is calculated using Advanced Design System (ADS) [16]. It can be seen from Figure 4(b) and Figure 5(b) that the gate underlap concept applied to an OTA gives significant performance improvement ((≅ 9) compared to a comparable bulk OTA *FoM* = 33.7 GHz×μW^{-1}. This results from a two and half fold higher f_T, three and half fold higher gain A_V and almost similar *linearity* value of 10 in underlap DG at same dc power consumption of 360μW. However, in comparing simulation with limited available experimental data for voltage gain *Av* [17], specifically from a 0.18 μm bulk technology with almost half effective gate length L_{EFF} ≅90nm of SDE DG, it can be concluded SOI offers significant potential for performance enhancement.

B. Effect of gate length

Figure 6 show the enhancement in *FoM* arising from use of gate underlap is most effective at lower bias current, a particularly significant observation for future technologies. In

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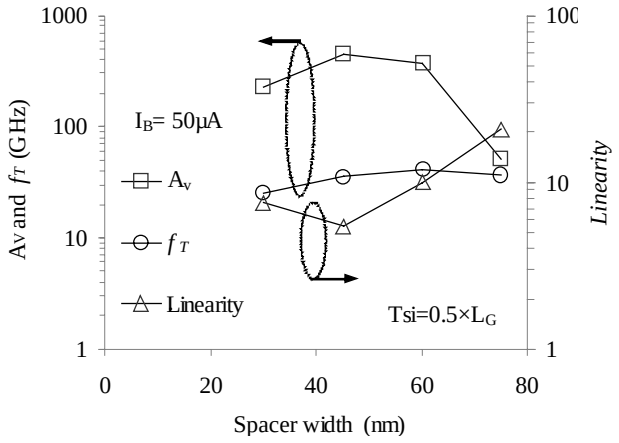
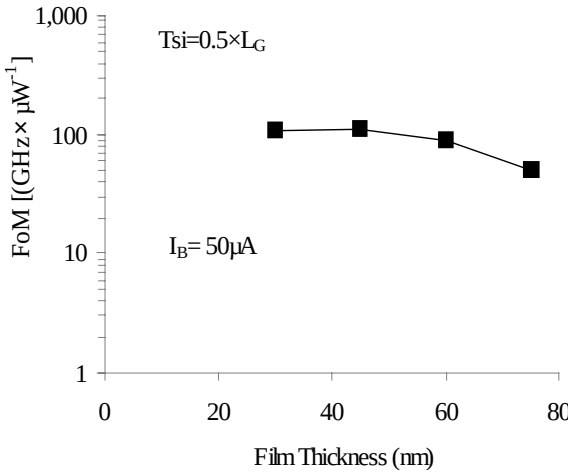
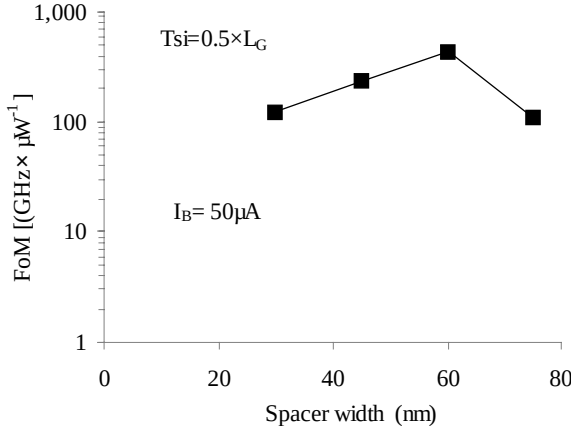


(a)



(b)

Figure 5. OTA performance variation with film thickness T_{SI} (a) A_V, f_T and linearity (b) FoM



(b)

Figure 4. OTA performance variation with spacer width (a) A_V, f_T and linearity (b) *FoM*

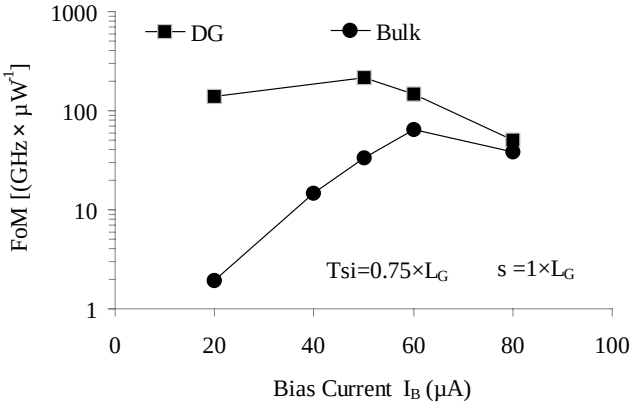


Figure 6. Comparison of underlap DG FoM (L_G=60nm) with bulk OTA simulated using BSIM4 (L_{EFF}=90nm)with variation in bias current I_B.

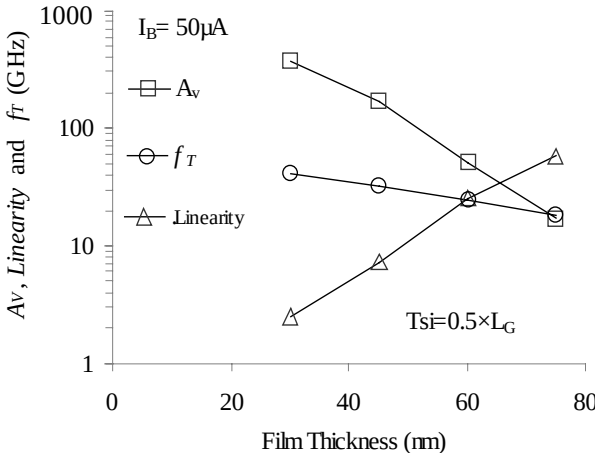


Figure 5(a)

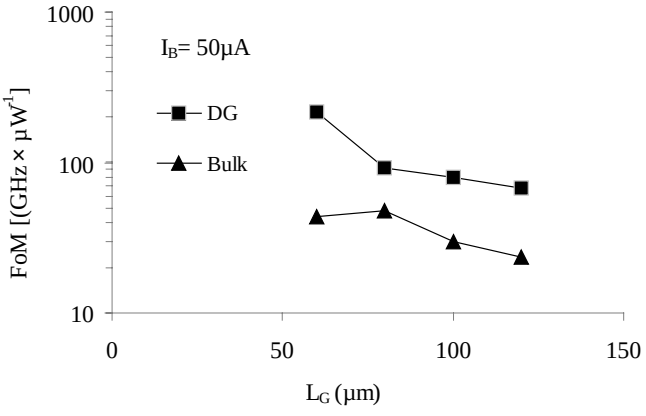


Figure 7. Comparison of underlap DG FoM with bulk OTA simulated using BSIM4 with variation in gate length L_G

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associated scaling of T_{ox} , an underlap device, $s=L_G$ and $Tsi=0.75L_G$ enhances FoM , primarily due to increase in f_T. Any enhancement arising from scaling a conventional bulk device is much less significant at shorter gate lengths.

III. Conclusions

Valuable design insights to optimize the performance of an OTA implemented with gate underlap DGSOI transistors have been provided. The superior performance of an OTA based on optimal DG MOSFET arises from a combination of enhanced voltage gain, linearity, and bandwidth especially at low power. An underlap DG OTA biased at 50 µA exhibits higher values of both voltage gain and f_T , alleviating the gain–bandwidth trade-off associated with analog circuit design. The resultant enhancement in overall FoM is almost an order of magnitude when compared to a conventional single gate MOSFET OTA.

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