Modeling of a Double-Layer Capacitor with Individual Branch Response

Md. Shafiul Islam, Md. Belayat Hossain*, Md. Nahid Hossain, Saadia Binte Alam and Md. Enamul Hoque Chowdhury

Abstract— **The double-layer capacitor (DLC) is a low voltage device exhibiting an extremely high capacitance value in comparison with other capacitor technologies of similar physical size. It's also a promising device for certain power electronic application as energy storage. In this work, a three RC branch equivalent circuit is used to characterize its terminal behavior and the equivalent circuits result are simulated using PSIM to provide the power electronics engineers a model for the terminal behavior of the DLC. Voltage dependent capacitor and schematic implementation of the double layer capacitor model using PSIM is also presented here. The simulated equivalent circuit response of a carbon-based DLC for power applications is found to be similar with the experimental results.**

Index Terms— **Double-layer capacitor, Energy storage system, Three RC branch equivalent circuit, Terminal behavior.**

I. Introduction

Double-layer capacitor can be used for energy storage and peak power control in order to increase the efficiency and the life cycle of a system. Potential applications are seen at the moment in short time uninterrupted power supplies (UPS) and peak load shaving in combination with batteries [1]. The power density of these capacitors is higher than that of batteries, and the energy density is 10 to 20 times higher than that of electrolytic capacitors for power applications. Smaller DLC's have been known for several years, but double-layer capacitors for power applications are just emerging.

This paper concentrates on Carbon-Based Double-Layer Capacitors (DLC's) suitable for power applications, which although expensive, are becoming now commercially available. These capacitors are low voltage devices with a rated voltage of 2.3 V and are available with capacitance values of 470 F, 900 F and 1500 F [2-3]. Higher voltages can be achieved by connecting many cells in series like in batteries. To study possible applications, a terminal model describing the behavior of the DLC is required. A three RC branch equivalent [4] is simulated to describe the terminal behavior of a DLC since the simulated model follows more precisely the measured terminal behavior of the DLC. Physical reasoning supports the structure of the equivalent model. Voltage dependent capacitor implementation using PSIM [5] is shown in this paper because in the simulation software there is no voltage variable capacitor available. Finally schematic implementation of the equivalent circuit model with charge-discharge control circuitry is presented here.

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II. DLC Equivalent Circuit

The purpose of the equivalent circuit is to provide a model of the terminal behavior of the DLC in power electronics circuits. The DLC consists of activated carbon particles that act as Polarizable electrodes [1]. These particles strongly packed are immersed in an electrolytic solution forming a double-layer charge distribution along the contact surface between carbon and electrolyte. Three major aspects of the physics of the double-layer charge distribution have an influence in the structure of the equivalent circuit model and these are as follows.

First, based on the electrochemistry of the interface between two materials in different phases, the double-layer charge distribution of differential sections of the interface is modeled as an *RC* circuit where resistance is for the resistivity of the carbon particles and the capacitor is due to the capacitance between carbon and electrolyte [6].

Second, based on the theory of the interfacial tension in the double-layer, the capacitance of the double-layer charge distribution depends on the potential difference across the material.

Third, the double-layer charge distribution shows certain self discharge.

The choice of three branches is the least number, if good accuracy is wanted for the specified time range of 30 min. Each of the three branches has a distinct time constant differing from the others in more than an order of magnitude which will result in an easily measurable model. The first or immediate branch, with the elements R_i, C_{io} and the voltage-dependent capacitor C_{i1} (in F/V), dominates the immediate behavior of the DLC in the time range of seconds in response to a charge action. The second or delayed branch, with parameters R_d and C_d dominates the terminal behavior in the range of minutes. Finally, the third or long-term branch,

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with parameters R_l and C_l determines the behavior for times longer than 10 min [3].

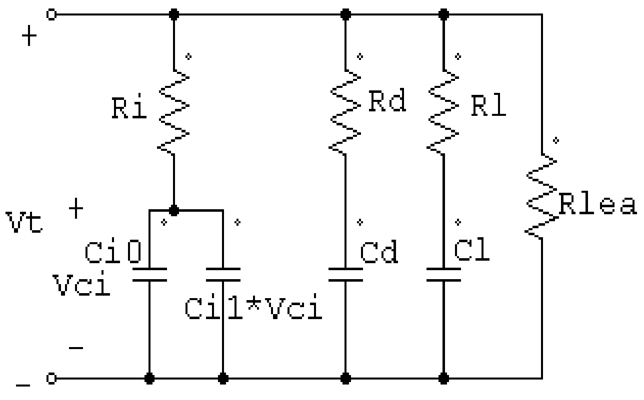

Fig.1. Equivalent Circuit Model for DLC

A leakage resistor, parallel to the terminals, is added to represent the self discharge property. The proposed equivalent circuit is shown in Fig.1 [3]

III. NONLINEARITY OF THE IMMEDIATE BRANCH

As stated before, the physics of the DLC predicts a voltage dependent value of capacitance. To simplify the model, this property has only been assigned to the first or immediate branch in the simulated DLC model. The usual linear definition of capacitance is the following:

$$C = \frac{Q}{V} \quad \text{............ (1)}$$

With Q the stored charge and V the capacitor voltage. The same definition of applies if the charge Q is the total charge in the device or an incremental charge ΔQ resulting from an incremental change ΔV in voltage. This definition is not valid for voltage-dependent capacitance. A useful definition, as it describes the change in charge at a given voltage, is the differential capacitance. This capacitance is defined as

$$C_{diff}(V) = \frac{dQ}{dV}\Big|_{V'} \quad \text{............................. (2)}$$

With dQ an incremental change in charge at a certain capacitor voltage V′ that produces an incremental change in voltage dV.

Based on the physics of the double layer and the usable range of voltage for the DLC, the differential capacitance is modeled as a constant capacitor and a capacitor which value varies linearly with the voltage

$$C_{diff}(V) = C_{i0} + C_{i1} * V \quad \text{.............................. (3)}$$

To verify this model of the nonlinear capacitance, measurements have been carried out to determine the parameters C_{i0} and Ci1. This nonlinear behavior of the immediate capacitance of the DLC has the consequence that more energy per voltage increment is stored at higher voltage than it would be in a constant linear capacitor. Calculating the stored energy in the immediate branch of the capacitor, it is

$$E = \frac{C_{i0}}{2} \times V^2 + \frac{Ci1}{3} \times V^3 \; (=1/2 C_e V^2) \quad \text{............(4)}$$

This is derived by using (2) and (3) and a constant charge current I, from, E=∫V*idt ……………………………….. (5)

With idt = Idt = dQ = C_{diff} dV and E = ∫(C_{i0} + C_{i1}*V)*V*dV

First, the equivalent capacitance C_q defined as the capacitance value of a linear capacitor holding the same charge as the DLC at some voltage V ($C_q = Q_{DLC}/V$). This capacitance derived from (3) and (4) is

$$C_q = C_{i0} + \frac{C_{i1}}{2} * V \quad \text{................................ (6)}$$

With $Q_{DLC} = \int C_{diff} dV = \int (C_{i0} + C_{i1} * V) * dV = C_{i0} * V + (1/2)\, Ci1 * V^2$

Second, the equivalent capacitance defined as the capacitance value of a linear capacitor holding the same energy as the DLC at some voltage. This capacitance derived from (6) is

$$C_e = C_{i0} + \frac{2}{3} C_{i1} * V \quad \text{………………………….. (7)}$$

IV. LEAKAGE RESISTANCE IDENTIFICATION

The leakage resistance is identified by measuring the decrease in the capacitor terminal voltage over a period of 24 hours. The capacitor used for the leakage resistance determination was previously normalized to 2 volts. After the normalization, it is expected that al1 the internal capacitances in the equivalent model are charged to the same voltage and the voltage decrease as function of time can be attributed to the equivalent leakage resistance. The duration of the test (24 hours) is much greater than the time constants of the three equivalent model branches; therefore, the capacitor is assumed as the parallel equivalent of the three branches and the resultant circuit is an RC circuit. The analysis of a simple RC circuit gives:

$$Vc(t) = V_0 e^{-t / R_{lea} Ct}$$

Where C_t is the parallel equivalent capacitance, Vc is the double-layer capacitor terminal voltage and Vo is the initial voltage for the discharge, or in other words the terminal voltage after the normalization. In the previous equation the value of the leakage resistance is assumed to be much larger than the resistance of the three branches [4] [7] [8].

Table.1. Model Parameter of 470F Capacitors.

Rated Voltage, V_{rated} = 2.3V	
PARAMETER	470F DLC
R_i	2.5mΩ
C_{i0}	270F
C_{i1}	190F/V
R_d	0.9Ω
C_d	100F
R_l	5.2Ω
C_l	220F
R_{lea}	9kΩ

In the previous relation V_o is two volts, ΔVc is measured after 24 hours found 0.04V [3], C_t is known from the previous identification of the internal capacitances which is equal to 470F and Δt is equal to 24 hours. Hence R_{lea} is approximately 9KΩ.The series of measurements and calculations explained

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above were carried out for 470-F DLC's. Table.1. shows the average of the Equivalent model parameter values measured for a double-layer capacitor.

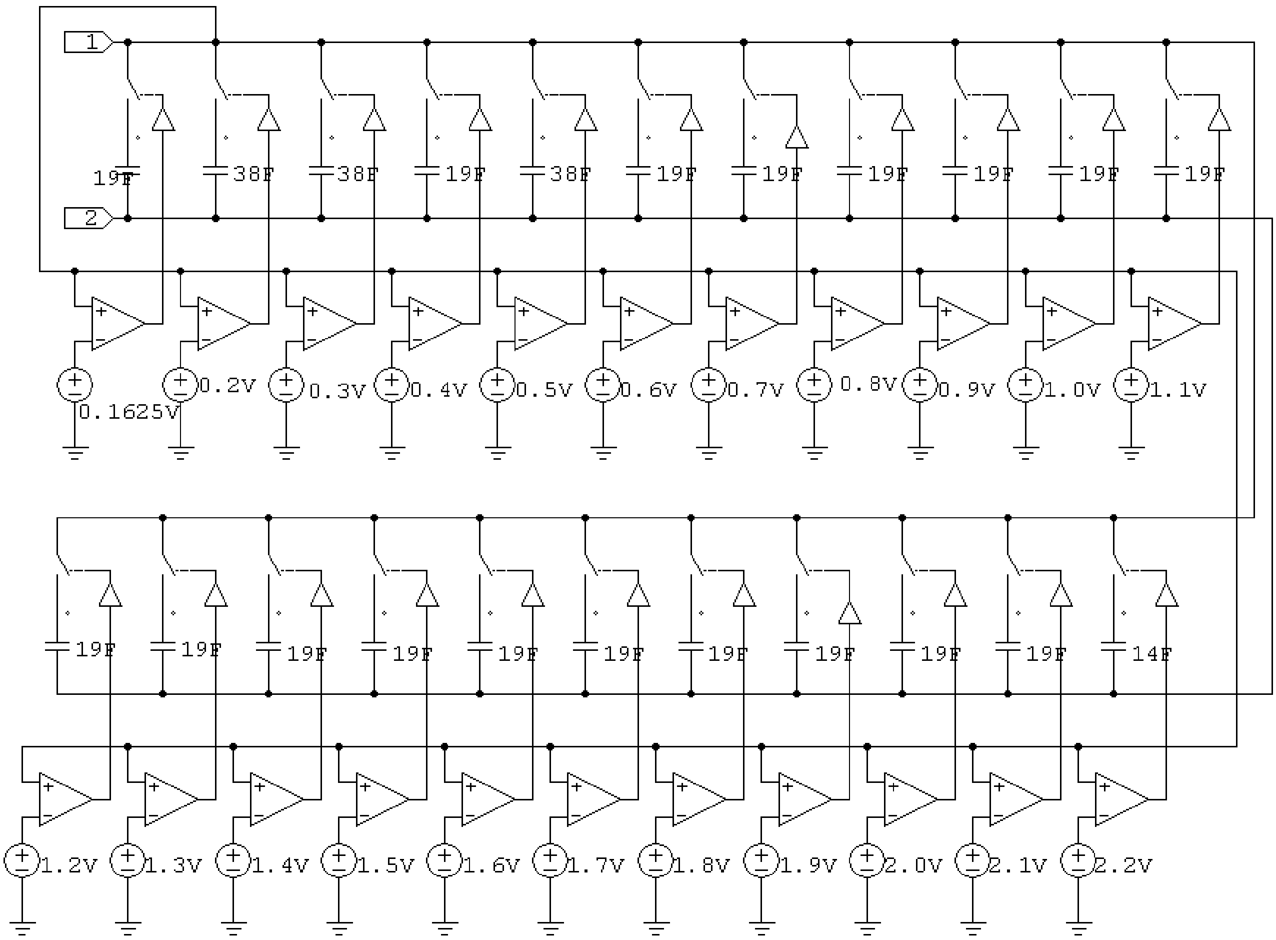

Fig.2. Voltage Dependent Capacitor Simulated using PSIM

V. VOLTAGE DEPENDENT CAPACITOR IMPLEMENTATION

Since in the PSIM simulation software there is no VVC (voltage variable capacitor), so the voltage variable capacitor is implemented using discrete components. Although this simulated device is not changes it's capacitance as continuously as practical device does rather using large number of stages of capacitance variation it has been seen that it follows the practical device quite well. We have 22 capacitors connected in parallel and a switch is connected with each capacitor, the switches are switched in different monotonic voltage levels and thus the parallel branches are added or discarded depending on the terminal voltage. So the capacitance is increased with increasing terminal voltage and decreased with decreasing terminal voltage. The higher the number of parallel branches the better the simulated devices approximates the original device. The voltage dependent capacitor C_{i1} as simulated by PSIM is shown in Fig.2

VI. IMPLEMENTION OF THE CAPACITOR MODEL

In Fig. 3, Capacitor model is constructed according to the Table 1. The 470F capacitor is charged through a constant current of 30A for the time duration required to charge the immediate branch to 2.3V. This is controlled by comparator1, monostable1 & JK FF1. When the terminal voltage reduced to 2.25V, the delayed branch is connected to the circuit which is done by comparator2, monostable2 & JK FF3. Last comparator, monostable & JK FF are used to connect the long term branch, which isn't worked during charging as the result has been seen for few seconds. The discharging period is controlled by two time dependent switches which start at 70s and end at 90s. To discharge the model constant current discharging circuit has been used.

VII. VERIFICATION OF THE PARAMETERS IDENTIFICATION ASSUMPTIONS

Fig. 4 shows the simulation of a simple charge and self charge distribution action. In the figure, the voltages in each of the three equivalent capacitors have been included. The point A shows the instant at which the current source is turned off and the delayed branch begins to be calculated. At this point, the voltage in the delayed branch is lower than 20% of the rated voltage, which means the energy stored in this branch is lower than 4% of the maximum energy in the branch. This result validates the assumption of no charge at the start of the delayed branch calculation used in the parameters identification.

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Point B shows the point of the delayed capacitance calculation. Point C shows the start of the long term branch calculation. Note in this point the almost equalized voltage in the immediate and delayed branches and the low voltage present in the long term branch at this point. Those two observations confirm the validity of the supposition of independent time behavior of the long term branch with respect to the delayed one.

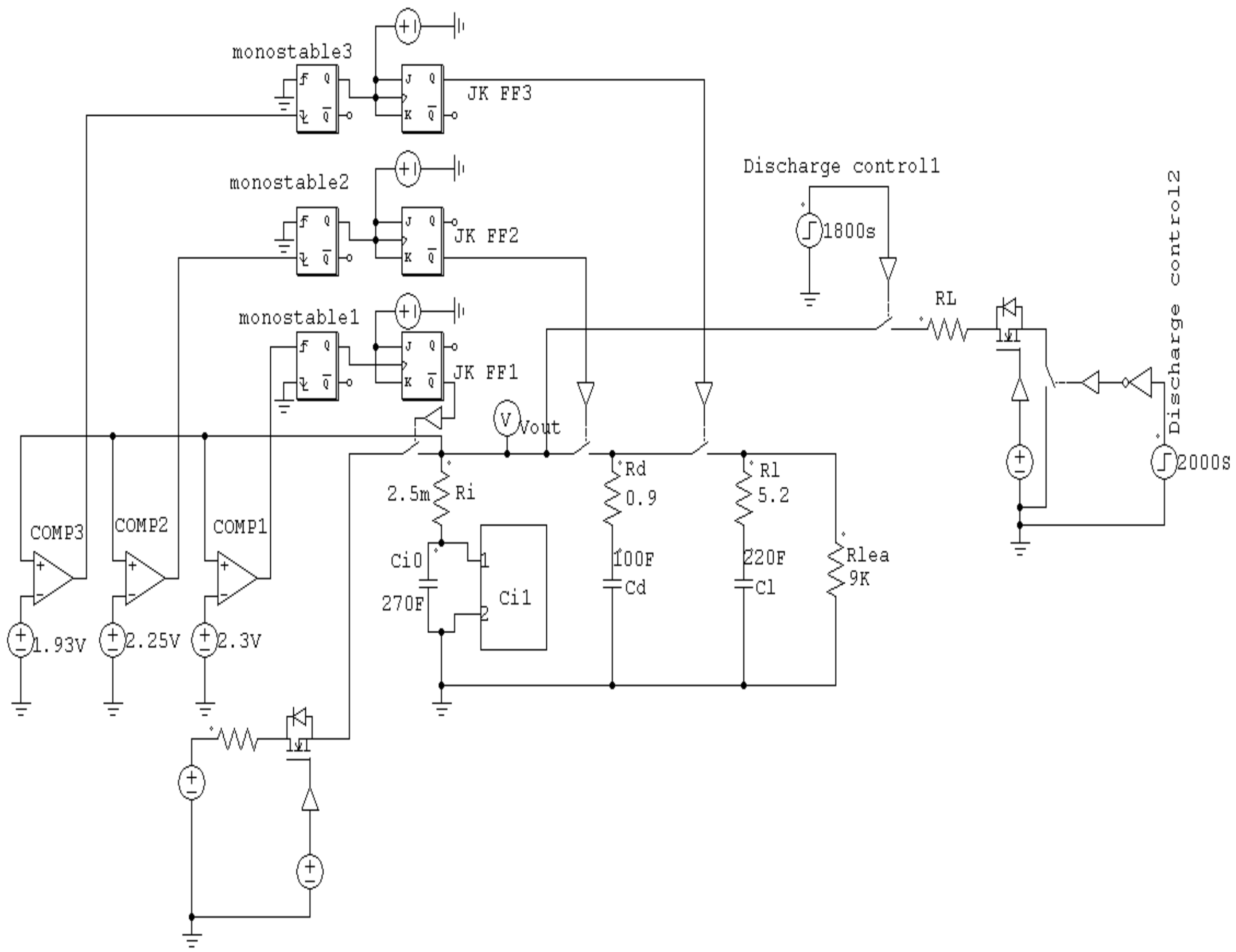

Fig. 3. Equivalent Circuit Model of a DLC with Charge-Discharge Control Circuitry.

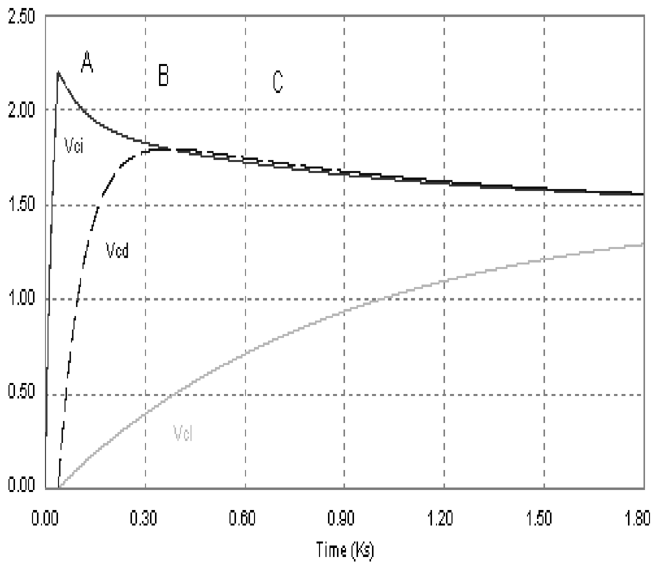

Fig.4. Verification of the Parameter Identification Assumptions**.**

VIII. VERIFICATION OF THE PROPOSED MODEL USING PSIM

The response for 470F DLC was simulated using the equivalent circuit and the Figs. 5, 6, 7 demonstrate a very good agreement between measurements [3] and simulation for a charge cycle using 470F DLC. For operating voltages below 1 V or less than 45% of the rated voltage, the error between simulation and experiment increases.

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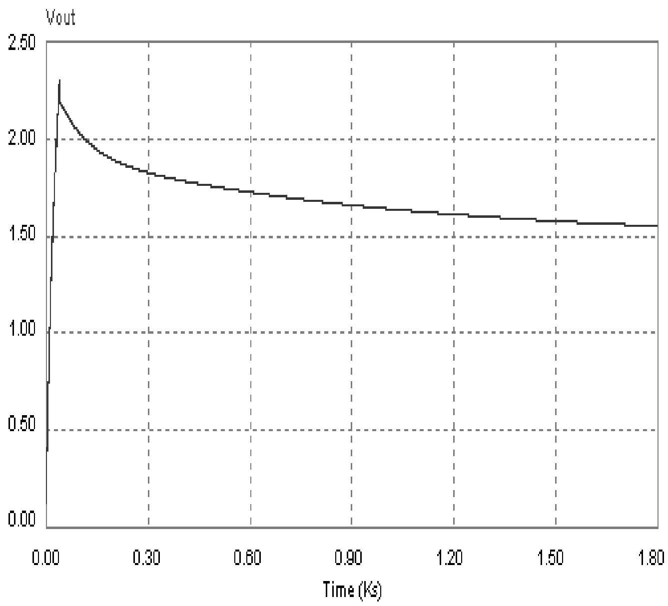

Fig.5. Simulated Output of Long Term Branches using PSIM.

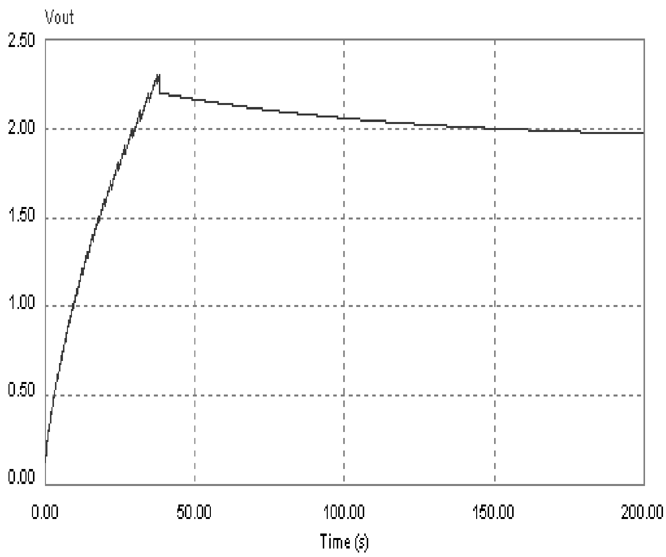

Fig.6. Simulated Output of Immediate & Delayed Branches using PSIM.

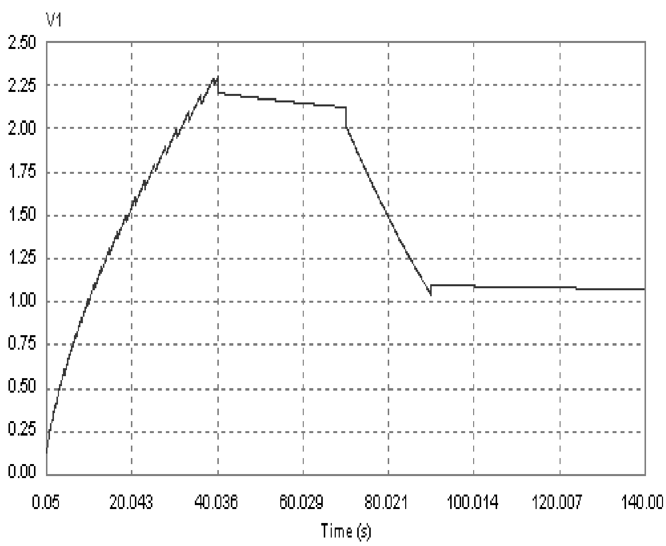

Fig.7. Simulated Output of EDLC Model using PSIM.

The reason for this increased error is our assumption that only the immediate branch capacitance is voltage dependent. In practice, all the equivalent capacitors have some voltage dependence. In addition, the agreement for larger times beyond 30 min is less accurate. The reason for this increased error is the energy stored in *RC* branches with very long time constants of hours or days, which have been neglected in the proposed model. It is estimated, that these branches may hold up to 10% of the energy of the DLC. The increased inaccuracies at low voltage or long time spans are in most practical applications of little importance, as the capacitor holds little energy at low voltage and is used for short-time energy storage. If these properties matter in specific applications, extended models have to be developed.

IX. CONCLUSION

The three RC branch equivalent model of a DLC is simulated using PSIM to describe the terminal behavior of the capacitor which is useful for the engineers to develop any system model using the capacitor. The model has been verified with the experimental results of the thesis work of Zubieta [3]. Simulation work using supercapacitor in the developing country like Bangladesh where supercapacitor is not locally available is now possible with the designed and tested model. Together with the schematic implementation of the charge-discharge control circuitry, this model opens a window for the power electronic engineers.

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