3 Phase Induction Motor Controlled with 9-Level Diode-Clamp Inverter

V. Tipsuwanporn¹, W. Sawaengsinkasikit², A. Numsomran³ and K. somsamai⁴

Abstract—This paper presents a new technique for harmonic reduction using multi-level diode clamp voltage source three-phase inverter. In order to increasing the high-efficiency and low Total Harmonic Distortion (THD), it obtained the output voltage waveform to nearly sinusoidal waveform. In this technique expected to result to eliminate certain harmonics or to minimize a current distortion in the induction motor and it operated system smoothly. In performed, the multi-level diode clamp three-phase inverter is varying the frequencies at 20 to 100 hertz for resistance, three-phase incandescent and induction motor load. Experimental results are presented to demonstrate the good performance of the proposed technique.

Keywords- Harmonics, Multi-level

I. Introduction

R ecently, the multilevel converter is widely applied in the industries because the demand to operate switching,

power converters in high power application has the development continuously. The ability of multilevel converters to operate at high voltages of the AC waveforms has low distortion, high quality and high efficiency. However, the multilevel converter [1] technology has improved efficiency by employing various controls to achieve the high efficiency and maximize to save energy. In this paper, the topology presented nine-level diode-clamp inverter and principle are implemented to control the output waveform approaching to the sine-wave as close as possible. A nine-level PWM inverter to reduce the Total Harmonic Distortion (THD) [2] of the inverter output voltages for three-phase induction motor drive are presented.

II. MULTILEVEL INVERTERS

The advanced power electronic technology, more high frequency switching products has been widely used in home electronic equipment and the industry applications [3]. Generally such systems use a diode bridge rectifier followed by a capacitor filter as the primary unregulated dc voltage. Low power factor and high input current harmonics from the ac mains are the main disadvantages of a diode bridge rectifier [3].

A nine-level diode-clamp inverter is used for experimentations in this proposed. The operations for each phase are performed by connecting 10-gate drives and using the 4-cell DC voltage sources to work with four capacitors per phase. The inverter employed the technique of proportional reduces harmonic elimination type [4], [5], [6] to control switching equipment in the circuit to providing appropriated waveform and increasing the efficiency at high performance. The multi-level power circuit of nine-level diode-clamp inverter can be demonstrated in Figure.1, circuit in Figure.1 was referred from [9].

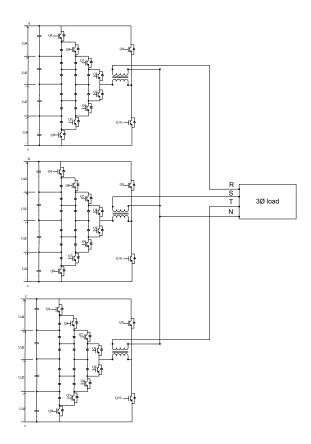


Figure 1 Power Drive Circuit of The nine-level diode-clamp inverter.

A. PRINCIPLES OF THREE-PHASE AC MOTOR

The control scheme is the most common way to control the magnitude and frequency of the stator voltage for an ac motor drive [3]. Several pulse width modulation techniques such as sinusoidal PWM, harmonic injected PWM, hysteresis PWM and space vector PWM have been proposed for the control of three phase ac induction motors [7]. Figure.1 shows this the proposed nine-level to control the three-phase induction motor drives based on the multilevel control approach [8].

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^{1,3,4} Department of Instrumentation and Control Engineering, Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang, Bangkok 10520, Thailand, Tel:66–2329–8347,Ext-102,E-mail: ktvittay@kmitl.ac.th

² Department of Electrical Engineering, Faculty of Engineering, Kasem Bundit University, Bangkok 10250, Thailand, Tel: 66–2320–2777: Ext.1213; E-mail: s_winyu@yahoo.com

The operations of induction motors are initiated by receiving energy from the source providing to the stator, and then, inducing through to the rotor resulting to rotation of the rotor. The stator coils produce constant magnetic field in the air gap between the stator and the rotor. The magnetic field rotates with synchronous speed which is related to following relation as

$$N_S = \frac{120 f}{p} \tag{1}$$

Where N_s = Synchronous speed f = Frequency (Hz)

p = Number of Pole

From (1) we can found speed motor as.

$$N_r = \frac{(1-s)(120f)}{p}$$
 (2)

B. METHOD OF CONTROL VOLTAGE PER

FREQUENCY

Varying of the supplied frequency to the motor causes change of the magnetic field or magnetic flux (ϕ) in air gap change by the following equation.

$$V = K \phi f$$

$$\phi = \frac{V}{Kf} \tag{3}$$

Where V = Voltage supply.

 ϕ = Magnetic flux in the air gap

K =Constant value

After the equation of voltage per frequency is derived, we can analyze the structure of tested inverter. Summation of full-bridge voltage can be written as

$$\begin{split} V_{AN} &= V_{dc1} + V_{dc2} + V_{dc3} + V_{dc4} \\ V_{BN} &= V_{dc1.1} + V_{dc2.1} + V_{dc3.1} + V_{dc4.1} \\ V_{CN} &= V_{dc1.2} + V_{dc2.2} + V_{dc3.2} + V_{dc4.2} \end{split} \tag{4}$$

According to the signal form of the multilevel inverter is shown on in figure 2, it can be written in the Fourier's series as follow:

$$v_{out}(\omega t) = \sum_{n=1}^{\infty} \left[\frac{4E}{n\pi} \sum_{k=1}^{s} \cos(n\alpha_k) \right] \sin(n\omega t)$$
 (5)

Coefficient of the Fourier's series in equation (5) can be written as

$$h_n = \frac{4E}{n\pi} \sum_{k=1}^{s} \cos(n\alpha_k)$$
 (6)

When n is 1, 3, 5 ...

elimination of unrequited harmonics, usually low level harmonics. For example, the 9-level phase voltage can eliminate the $3^{\rm rd}$, $5^{\rm th}$, and $7^{\rm th}$ harmonics level by setting magnitude of fundamental frequency per phase in form of modulation index equal to 0.85, which is substituted to the equation (6) as shown. Equation (7) are nonlinear equations whose solution are obtained by means of Newton-Rap Son method but the solution must be agree to the condition of α_1 , α_2 , α_3 , α_4 $\langle \frac{\pi}{2}$

Determination of switching angle $\alpha_1, \alpha_2, \dots$ and α_s as

shown in figure 2 can reduce %THD value of voltage due to

Figure 2. The 9-level phase voltage and full bridge cell outputs.

$$\cos(\alpha_{1}) + \cos(\alpha_{2}) + \cos(\alpha_{3}) + \cos(\alpha_{4}) = 0.85 \frac{3\pi}{4}$$

$$\cos(3\alpha_{1}) + \cos(3\alpha_{2}) + \cos(3\alpha_{3}) + \cos(3\alpha_{4}) = 0$$

$$\cos(5\alpha_{1}) + \cos(5\alpha_{2}) + \cos(5\alpha_{3}) + \cos(5\alpha_{4}) = 0$$

$$\cos(7\alpha_{1}) + \cos(7\alpha_{2}) + \cos(7\alpha_{3}) + \cos(7\alpha_{4}) = 0$$
(7)

The efficiency of signal form is measured term of the output voltage's THD, which can be calculated by the following equation.

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} H_n^2}}{H_1} \tag{8}$$

When H_1 is magnitude of fundamental frequency H_n is magnitude of nth harmonics

C. NINE-LEVEL PWM INVERTER SWITCHING

STRATEGY

In modeling switching strategy of the power inverter module, It is based on nine-level diode clamp PWM technique. The propose is suitable for modulating signal of arbitrary waveform on voltage and frequency.

Modulating signal generator is generated from microcontroller ARM 7 (ADU 7024) to proper digital signal for switching on the inverter switching driver. Power inverter module is used for the nine-level diode-clamp inverter to combining the signal into Multi-level inverter diode clamp [10].

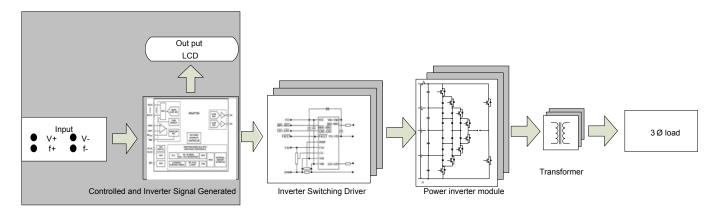


Figure 3. Block Diagram for 9 Level inverter.

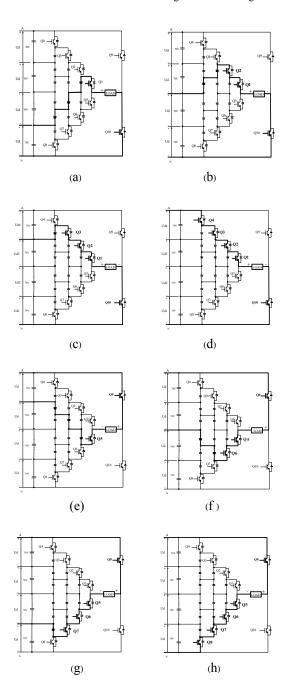


Figure 4. The 9 Level inverter switching strategy.

In figure 4, we can very switch IGBT to 8 step. Step1, on figure4(a) is shown switching Q1 and Q10 to operate the voltage at Ud. Step2, on figure4(b) is shown switching Q1, Q2 and Q10 to operate the voltage at 2Ud. Step3, on figure 4 (c), is shown switching Q1, Q2, Q3 and Q10 to operate the voltage at 3Ud. Step4, on figure4(d) is shown switching Q1, Q2, Q3, Q4 and Q10 to operate at voltage at 4Ud. Step5, on figure 4(e) is shown switching Q5 and Q9 to operate the voltage at -Ud. Step 6, on figure4(f) is shown switching Q5, Q6 and Q9 to operate the voltage at -2Ud. Step7, on figure4(g) is shown switching Q5, Q6, Q7 and Q9 to operate the voltage at-3Ud. and Step 8, on figure4(h) is shown switching Q5, Q6, Q7, Q8 and Q9 to operate the voltage at -4Ud [9].

A. HARDWARE STRUCTURE OF NINE LEVEL INVERTER

In figure 3 is a block diagram of the nine level inverter witch diode clamp. It can be separated to 5 part. Ones is the controlled and inverter signal generated to control frequency, duty cycle and to generate the nine level inverter switching that can see on figure 5. Part two is the inverter switching driver for driving the gate signal of IGBTs that can see on figure 6. Part three is the power inverter module for created the nine level inverter voltage that can see on figure 7. Part four is a transformer to separate the ground of each phase voltage to reduce the problem of floating gate drive. Finally, the block is a load for using.



Figure 5. Controlled and signal switching generated.

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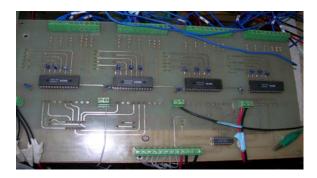
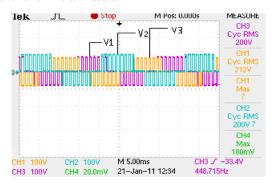
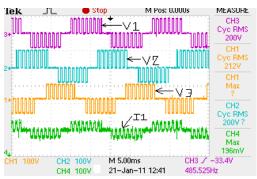


Figure 6. Nine level inverter driver.



Figure 7. Power inverter module.





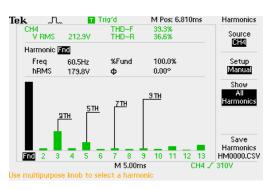


Figure 8. The voltage, current and THDv of general inverter at D=0.6 and $60\,\mathrm{Hz}$ on resistance load.

III. EXPERIMENTATION RESULTS

In order to demonstrate the Total Harmonic Distortion (THD) features of a nine-level diode clamp PWM inverter, a comparison between general inverter and the nine-level inverter with diode clamp of the modulated harmonics based on the following multi-level topologies is presented.

First, we are experiment on the resistance load at D=0.6 and 60 Hz with general inverter. The results of voltage, current and THDv are shown on figure 8.

With the nine level inverter, the results of voltage, current and THDv are show on figure 9. Next, we are experiment on the three phase induction motor(4 pole, Pf=0.8, 330Watt). The voltage and current results are shown on figure 10.

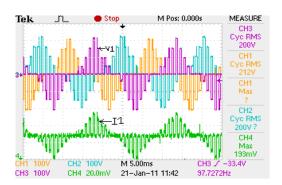




Figure 9. The voltage, current and THDv of nine level inverter at D=0.6 and 60 Hz on resistance load.

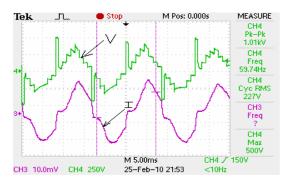


Figure 10. The voltage and current of nine level inverter at D=1 and 60 Hz on three-phase induction motor.

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IV. CONCLUSION

From the experimental results, the nine-level diode clamp three-phase inverter structure used in this paper, it can reduced the Total Harmonic Distortion (THD) about 20% and decreased the low order of harmonics that can see on figure 8-9. Also output voltage has been a nearly sinusoidal waveform compared than the conventional inverter. As a result, the output voltage controlling load as resistance load and three-phase induction motor has satisfied performance.

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