A SPICE-compatible Model for Intel®'s 45nm High-*K* MOSFET

A. Ávila[1], D. Espejo[2].

***Abstract*— An original SPICE-compatible model for Intel®'s 45nm High-K MOSFET is presented. It takes into account some Quantum-Mechanical Effects that occur on small scale like *Channel Length Modulation* (CLM), *Threshold Voltage shift* and *Velocity saturation*, and is the first in its class to not be fully based on ASU's Predictive Technology Model, but incorporates device parameters to fully simulate process variation effects on MOSFET behavior. The model expressions are found first by obtaining and validating a model for the carrier quantization phenomenon in the region near the Si/HfO_2 interface because the effects associated with that particular phenomenon determine the device behavior in a downscaling scenario. Precision of that model, allowed finding equations for the device's compact I-V model. Transient analysis shows precision over 98% for the model equations compared with Intel®'s data.**

Keywords: MOSFET; model; high-k; SPICE; quantization

I. Introduction

As semiconductor industry is looking for increasing levels of circuit integration and fulfilling of Moore's Law [1], the discipline of semiconductor devices modeling is facing challenges arising from scaling. Intel ™ has proposed [2] a new insulating material for MOSFET's dielectric: HfO_2, whose dielectric constant *k*, nearly 4 times that of traditional SiO2, provides the advantage of reducing the probability of the occurrence of leakage currents caused by effects such as tunneling, which are more likely to happen in short channel devices. This article describes the procedure developed in order to build a model compatible with SPICE ™ for Intel®'s *High-k* MOSFET, and that can be used for single-gate MOSFETs with HfO_2 as gate dielectric. This model describes device behavior by considering the effects associated with short *channel length* (L_g) and increasing E_y, with accuracy over 98% compared with Intel®'s data [2].

II. MOSFET Architectures State Of The Art

As a first step, different architectures of current MOSFETs were identified, from 2005 onwards, both in research and production stages, in order to acknowledge their main parameters and size, comparing them under the same parameter: L_g. The results of this stage are summarized in Table 1, which has been ordered by L_g from lowest to highest

TABLE I
Novel Mosfet Structures

Device	FinFET	GAA	High-K	VRG	TriG
State	R	R	P	R	P
Lg (nm)	20	30	45	50	60
Description	Si segment divides the Gate	Gate material surrounds channel	High-k gate dielectric	L_g controlled through a deposited film thickness	Three effective gates, sources and drains
Dissipated power (W)	44n	30n	61n	39µ	72µ

R: Research P: Production

Taking into account that, at the time of this stage of research, Intel's 45nm High-k MOSFET, was the one with the world's smallest L_g in production (being passed in January 2010, following the launch of Core processor 32 nm family [3]), authors chose to describe and achieve a model for this device to provide a considerable relevance to the results of this research.

III. Intel's *High-K* Mosfet Electrical And Physical Parameters

After the review of the available literature about the studied device, the physical (mainly, material properties) and electrical parameters reported by the manufacturer were gathered [2]:

TABLE II
Intel 45nm Mosfet Electrical And Physical Parameters

Physical dimensions	Material parameters	Electrical parameters
$L_g = 40nm$ $T_{ox} = 1nm$	$\varepsilon_r = 20$ K = 14 to 20	V_{gs} range: 0V – 1,7V (N channel) I_d range: 0 - 104µA (N channel)
$I_{th} = 200nm$ x_{dD} y x_{dS} = 20nm~90nm	ρ = 4.5 x 10^3 @1100°C	$V_{th} = 0{,}32$ @ $V_{ds} = 1V$
Gate pitch = 160nm	Band gap = 6eV	$V_{th} = 0{,}42$ @ $V_{ds} = 0{,}5V$

From the above data it is possible to recognize that in this device, T_{ox} has the dimension of a few atomic layers and the insulator material is about 4 times more resistant to carrier tunneling, compared with the traditional SiO_2, which *K* is equal to 3,9. The studied device is considered as a *short channel device*, because its L_g is in the same order of magnitude as x_{dD} and x_{dS}, which sets up a scenario where the electric field in the direction perpendicular to the semiconductor-oxide interface E_y is high with a tendency to keep growing, and where the phenomena known as *Short*

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[1]A. Ávila is an associate professor at the Department of Electrical and Electronics Engineering, University of the Andes (Universidad de los Andes), Carrera 1 Este # 19A-40, Mario Laserna building, ML-320 office, Bogotá, Colombia (Phone: (+571) 339-4949, extension 2828; fax: (+571) 339-4949; e-mail: a-avila@uniandes.edu.co).

[2]D. Espejo is pursuing his Master's degree at the Department of Electrical and Electronics Engineering, University of the Andes (Universidad de los Andes), Carrera 1 Este # 19A-40, Mario Laserna building, ML-008 office, Bogotá, Colombia. (e-mail: de.espejo71@uniandes.edu.co).

Channel Effects is most likely to occur. One of the research questions that motivated the work documented here has to do with the presence or absence of such effects in MOSFET models available in SPICE-based simulators. An observation of models developed by the University of California, Berkeley and other schools and companies such as Phillips Semiconductor, shows that the models still fail to accurately describe the behavior of short channel MOSFETs. That is the case of the latest MOSFET model developed for SPICE: BSIM 4.6.4. Its manual [4], indicates that its L_{eff} designed limit is 1nm, however, to model devices with high-k dielectric, proposes a simple proportions relationship to calculate equivalent EOT from the one of devices with SiO_2 as dielectric. An approach as simplistic as this one, may lead to high inaccuracy in the description of device behavior. These limitations present in the latest MOSFET model developed for SPICE, led to the need for a new device model to be tested with Intel´s 45nm *High-k* MOSFET physical and electrical parameters.

IV. A Model For Carrier Quantization

Given that in Intel's 45nm MOSFET, carrier tunneling through the dielectric is considered more likely to happen, and that under that phenomena, carriers behave in a way similar to waves, also being confined in a potential well by a high E_y; it is necessary to model the behavior of the device through a description of the carrier as particle as well as wave. The proposed procedure starts from Poisson equation describing 2-D potential distribution $\phi(x,y)$ along the channel:

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2}=\frac{q}{\varepsilon_{Si}}(N_A(x)+n(x,y)) \quad (1)$$

In the scenario in which the charge is quantized, the continuous conduction band is now divided into two sub-bands. The wave function of each sub-band is given by the Schrodinger equation:

$$\frac{\overline{h}^2}{2m}\nabla^2\psi-q\phi(x,y)\psi_i(x,y)=E_i\psi_i(x,y) \quad (2)$$

Noting that carriers confinement is higher in the direction perpendicular to the Gate, the one-dimensional Schrodinger equation is enough for the problem. By ensuring a MOS structure with uniform potential distribution along the direction perpendicular to the Gate, y variable can be removed from Poisson's equation, and reduce the problem to coupled one-dimensional equations of Schrodinger-Poisson:

$$\frac{d^2\phi(x)}{dx^2}=\frac{qN_A(x)}{\varepsilon_{Si}}-\sum_i\frac{Q_{inv,i}}{q\varepsilon_{Si}}|\psi_i(x)|^2 \quad (3)$$

$$-\frac{\overline{h}^2}{2m}\frac{d^2\psi(x)}{dx^2}-q\phi(x)\psi(x)=E\psi(x) \quad (4)$$

Reaching an analytical solution for this pair of equations is not an easy task; however, numerical simulations provide some insights into reaching this solution.

Figure 1 shows the results of simulating the carriers population per sub-band, using the parameters of Intel®'s High-K MOSFET: $N_d = 1^{18}cm^3$, $T_{ox} = 1nm$ y $k = 22$:

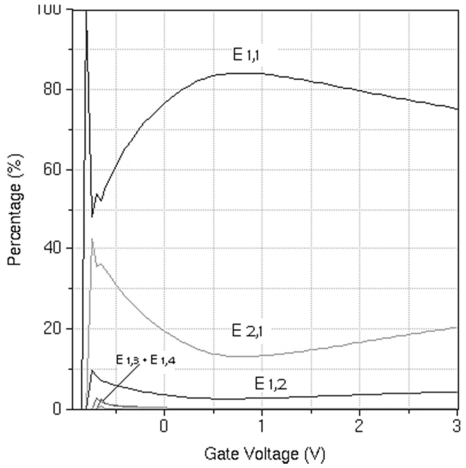

Figure 1. Numeric simulation of carrier populations per sub-band, simulation conduced using SCHRED [5] with parameters Tox = 1nm, T = 300°K and Nd = $10^{18}cm^{-3}$.

From Fig. 1, as we move amid $0V<V_{gs}<3V$, it is possible to see that between 45% and 85% of the carriers reside in the lower sub-band, so only the lowest level of energy will be considered to approach to the analytical solution. With that estimate, the pair of equations (3) and (4) for each valley or group of sub-bands associated with the crystal structure of the interface $Si\text{-}HfO_2$ are reduced to:

$$\frac{d^2\phi(x)}{dx^2}=\frac{qN_A(x)}{\varepsilon_{Si}}+\frac{Q_{inv,1}}{q\varepsilon_{Si}}|\psi_{1,1}(x)|^2+\frac{Q_{inv,2}}{q\varepsilon_{Si}}|\psi_{1,2}(x)|^2 \quad (5)$$

$$-\frac{\overline{h}^2}{2m_i}\frac{d^2\psi_{1,1}(x)}{dx^2}-q\phi(x)\psi_{1,i}(x)=E_{i,1}\psi_{i,1}(x) \quad i=1,2 \quad (6)$$

Where i denotes each of the two valleys where the lowest energy level will be obtained.

A. Solution by Variational Method

Using calculus of variations, wave functions are assumed with shape similar to $\psi_{1,1}$ y $\psi_{1,2}$, thereby ensuring a good level of accuracy for the calculated energy levels [6]. Now we proceed to integrate the simplified Poisson equation from the bulk to the surface. And in order to find the lowest expression of energy, expected value of the wave function $\psi_{1,1}$ Hamiltonian is calculated obtaining the following expression:

$$E_{1,1}=\int_0^\infty\psi_{1,1}(x)\frac{\hbar^2}{2m_1}\frac{d}{dx^2}\psi_{1,1}(x)dx+\int_0^\infty q\phi(x)\,\psi_{1,1}(x)^2dx \quad (7)$$

With the simulation of the sub-bands wave functions, we can get closer to the analytical solution:

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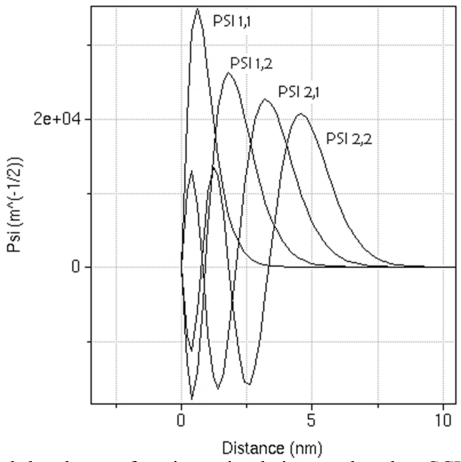

Figure 2. Sub-bands wavefunctions, simulation conduced on SCHRED [5].

Simulation of Fig. 2 shows that the peak of carrier density is a few nanometers (no more than 5 nm) below the channel surface, which leads to approximate:

$$d \gg \frac{1}{\alpha_1} \text{ and } d \gg \frac{1}{\alpha_2}, \qquad (8)$$

Then, this approximation is applied and the result is factorized, based on the parameter γ of proportionality. According to the variation method, α_1 and α_2 should minimize the energy level, ie:

$$\frac{dE_{1,1}}{d\alpha_1} = 0 \qquad \text{and} \qquad \frac{dE_{1,2}}{d\alpha_2} = 0 \qquad (9)$$

Calculating the derivatives, we obtain the expressions for α_1 and α_2, then the mean value of γ is obtained. Finally, replacing the values obtained and the approximations described above, leads to the expressions for $E_{1,1}$ and $E_{1,2}$:

$$E_{1,1} = \frac{3\overline{h^2}{\alpha_1}^2}{2m_1} \qquad \text{y} \qquad E_{1,2} = \frac{3\overline{h^2}{\alpha_2}^2}{2m_2} \approx 1{,}432E_{1,1} \quad (10)$$

Verification of model validity is done by comparing its results with SCHRED simulation of energy levels for sub-bands:

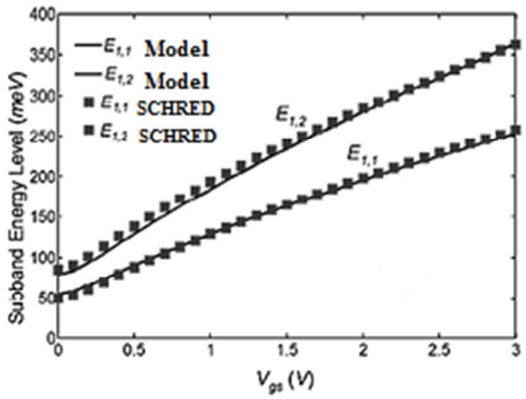

Figure 3. Energy levels at each valley, by model expressions and by SCHRED simulation

Accuracy of the quantization model obtained, allows us to approach a short channel I-V model that takes into account the quantization of charge that occurs at this scale, and enables some approximations for that model, keeping the same accuracy.

V. I-V Short Channel Model

The fact that, in short channel devices, there is no complete control of the channel charge is an indicator that E_y is not negligible compared to E_x and the effects associated with this fact should be incorporated in a compact model. In terms of I_d, the most significant effect to be included is *velocity saturation*, that may result in reduced effective saturation I_d.

A. Velocity Saturation Model

One of the empirical relations in use to model the dependence of carrier velocity v_d with respect to E_x was adopted for this step [7]:

$$|v_d| = \frac{|v_d|max|E_x|/|E_c|}{1+|E_x|/|E_c|} \qquad (11)$$

The first expression to find is the one for I_d in linear region I_{DSn}. E_x is expressed as the differentials of the potential between the polarization of the inversion layer and the end of the piece. Integrating these differences along the channel, we obtain the I_d expression at non saturation regime:

$$I_{DS} = \frac{W}{L}\mu C_{ox}\left[\frac{(V_{GS}-V_{TH})V_{DS}-0.5\alpha V_{DS}^2}{1+\frac{V_{DS}}{LE_C}}\right] \qquad V_{DS} \le V'_{DS} \qquad (12)$$

For the expression in the saturation region, it is necessary to include the effect of *Channel Length Modulation* or CLM [6], finding the value of V_{ds} in which saturation occurs, so the expression of I_{ds} in presence of velocity saturation is given by:

$$I_{DS} = W\mu C_{ox}\left[\frac{(V_{GS}-V_t)V'_{DS}-0.5\alpha V_{DS}^2}{L\left(1-\frac{1}{L}p+\frac{V'_{DS}}{LE_C}\right)}\right] \qquad (13)$$

B. Compact I-V Short Channel Model

Finally, to obtain a unified expression of I_d in presence of velocity saturation, it becomes necessary to incorporate the smoothing equation of V_{ds}:

$$V_{deff} = V_{DSAT} - \frac{1}{2}[V_{DSAT} - V_{DS} - \delta_s + \sqrt{(V_{DSAT} - V_{DS} - \delta_s)^2 + 4\delta_s V_{DSAT}} \quad (14)$$

Thus, V_{deff} is used to replace V_{ds} in the I_{ds} expression, as well as the *Early* effective voltage V_{Aeff} to incorporate CLM in the unified expression, that is then obtained:

$$I_{ds} = \frac{I_{deff}}{1+(R_{sd}I_{deff})/V_{deff}} \qquad (14)$$

with

$$I_{deff} = \left(1 + \frac{V_{DS}-V_{deff}}{V_{Aeff}}\right)I_{ds0} \quad \text{y} \quad V_{Aeff} = \frac{E_{SAT}L_{eff}(E_{SAT}L_{eff}+V_{DS})}{\xi V_{deff}} \qquad (15)$$

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C. Checking Model Results Compared with Manufacturer's Data

With the physical and electrical parameters given in Table 2 and those obtained by the *Arizona State University Predictive Technology Model* for 45 nm node [8], we compare the results using the IV model expressions obtained from the curve provided by the manufacturer [2]:

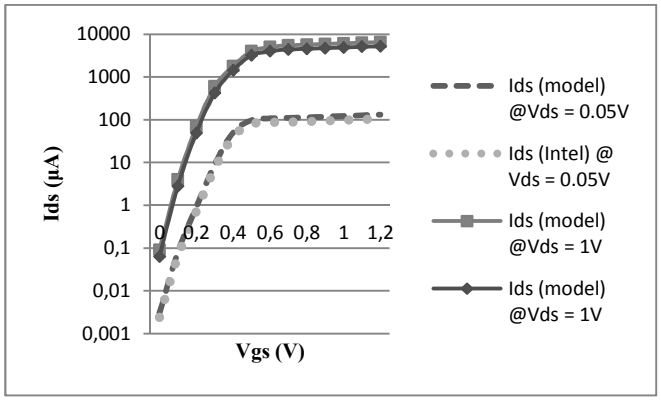

Figure 4. I-V characteristic by model expressions and Intel®'s data

The results show a correlation coefficient R^2 equal to 0,9 and an average error of 0.33, indicating a relatively strong relationship between the data obtained by the model and those reported by the manufacturer. This level of accuracy, allows us to get to the next stage, which is the model equations testing in SPICE.

VI. TESTING THE MODEL EXPRESSIONS IN A SPICE CIRCUIT

To ensure the portability of the model for any SPICE-based simulator, obtained model expressions were incorporated using Analog Behavioral Modeling blocks, included in Orcad© PSPICE 9.1. Those blocks have a maximum of three inputs and one output of voltage or current. They use mathematical relationships to model a circuit segment and, when connected in cascade, and at *netlist* generation stage, the simulator concatenates the blocks to make the entire expression. Expressions are entered in the model and tested in a configuration of half-wave rectifier-inverter, compared with an N-channel MOSFET in the same configuration, whose electrical and physical parameters have been replaced by the ones of Intel's *High-k* MOSFET to verify the performance of BSIM4 model at sub-50nm scale and the operation of the model obtained in a circuital implementation. Simulation shows us the degradation in the description of the MOSFET in sub-threshold regime by BSIM4 model and a good performance of model expressions obtained.

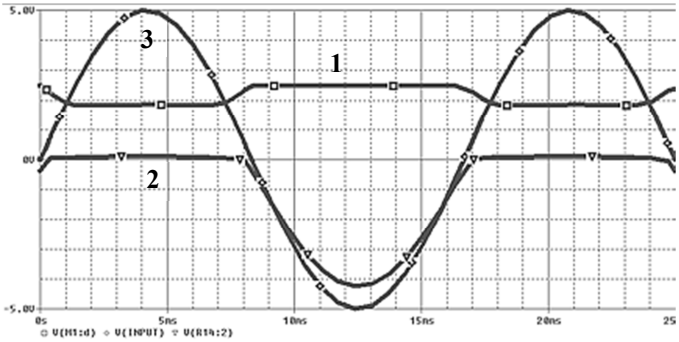

Figure 5. Transient analysis using Orcad PSICE™ 9.1 for three signals: 1 – Output voltage of native N-MOS MOSFET with High-k transistor physical and electrical parameters running under BSIM 4.4 model, 2 – output of ABM blocks running model expressions obtained with this methodology, 3 – input voltage signal with amplitude of 5V and 60 Hz frequency. This results show that current MOSFET compact models like Berkeley's BSIM cannot simulate device behavior properly at the nano scale because the lack of a Quantum-mechanical approach, and show good performance of model expressions in a common circuit configuration.

CONCLUSIONS AND RECOMMENDATIONS

A novel modeling methodology, based on the effects of charge quantization on device behavior has been developed, obtaining a compact model that describes, with accuracy over 98%, the behavior of the Intel™'s *High-k* 45nm MOSFET in the presence of velocity saturation and V_{th} shift. The proposed methodology has been condensed into a learning object SCORM-compatible (Sharable Content Object Reference Model), which is available at *https://nanohub.org/resources/10024*. Future work could include additional effects such as temperature dependence and body effect among others. The model could be simplified to have as few parameters as possible, avoiding a great number of ABM blocks.

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