Method of IPA Cleaning Process on Temperature and Spin Speed for Prevent Pattern Collapse in DRAM Capacitor

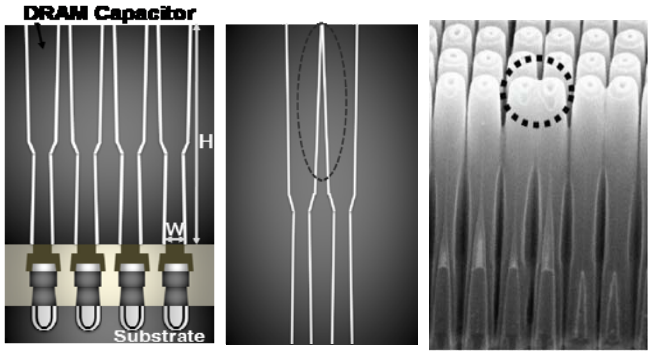
Keun-Sun Kim, Jae-Hyung Jung, Hyung-Joon Kim

***Abstract*— The capacitor is one of the most important element in DRAM (Dynamic Random Access Memory). Many engineers try to raise the amount of the charge in capacitor through improving systems. In order to increase capacitance, there are some methods such as using high-k materials, increasing the area of capacitor or decreasing the thickness of dielectric substance. Although using high-k materials might be very effective for increasing the capacitance, the bandgap energy of high-k materials are small and leakage characteristics are not good compared to SiO_2, relatively. Therefore, many new composite materials have been studied. As the results of shrinking DRAM capacitor scheme and using the variety of materials, the capacitor collapse (leaning) or new defects are appeared. Therefore these problems make the cleaning process important. In this paper, we suggest the method which solves these problems through the temperature increase of IPA cleaning solution and the wafer spin speed control of cleaning process. This proposed method improved the actual DRAM production and yield.**

***Index Terms*— pattern collapse(leaning), DRAM, IPA, capacitor, surface tension**

I. Introduction

As a design rule of semiconductor is continuously being reduced, the aspect ratio of the capacitor DRAM are getting being increased so capacitor are collapsed or leaned on drying process in cleaning process.



(a) (b) (c)

Fig. 1. Aspect ratio due to increases DRAM capacitor leaning schematic.

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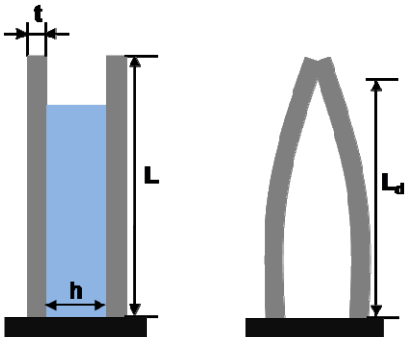
Fig 1 (a) DRAM capacitor structure, (b) high aspect ratio in the cleaning process when doing unstable height caused by leaning on the concept, (c) the actual capacitor contact (bridge) phenomenon of SEM (Scanning Electron Microscopy. In this paper, the collapse of DRAM capacitors leaning problems in the fabrication of semiconductors verified to suggest ways to improve and focus on the actual technology through experiments.

II. Model

A. Capacitor Leaning

When capacitor having high aspect ratio is proceeded in cleaning process, leaning appears by various factors in DRAM of micro pattern.



(a) (b)

Fig. 2. After DRAM capacitor rinse leaning schematic [2][3]

$$L_d = \alpha \left(\frac{2E}{9\gamma_L \cos\theta_c} \right)^{1/4} \left(\frac{h^2 t^3}{1 + t/w} \right)^{1/4} \quad (1)$$

where:

E the Young modulus

h the space between cantilever and substrate (or sacrificial layer thickness)

t the beam thickness

l the beam length

w the beam width

γL the liquid surface tension

θc the contact angle of the liquid on the substrate

Fig. 2 (a) if liquid exist between thin and long materials, it receives capillary force. By this, top part is bent as Fig. 2. If the experiment is implemented at the same condition on materials, length, height, thickness, the surface tension of the

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liquid remains as a variable.

B. *Capacitor Cleaning Process*

Capacitor process is to rinse chemical materials used for etching by using DIW (Deionized Water), and this is one of the purposes of cleaning. At this point, the surface tension of DIW in cleaning process is relatively very high. To reduce the surface tension, after IPA substitution, spin drying process comes first then a process for removing IPA comes next.. To making a drying process that leaning of capacitor does not occurs, It is highly important to substitute IPA for DIW and dry it uniformly. [4]

III. EXPERIMENT

A. *Preparing for Experiment*

After deposition of 300mm Silicon Wafer samples and 7000 Å of single mold for experiments on the TEOS (tetraethly orthosilicate), storage poly capacitor was formed by using a reticle. When the oxide removal process between capacitor was being proceeded, we analyzed leaning to determine if leaning occurs or not by Hitachi SEM and a discovery measuring instrument. And we made the condition of the experiment same like factors of leaning affecting other parameters of the capacitor.

When substituting the IPA for DIW. The concentration of IPA was 100 percent, it is for the phenomenon shown as Fig. 3.

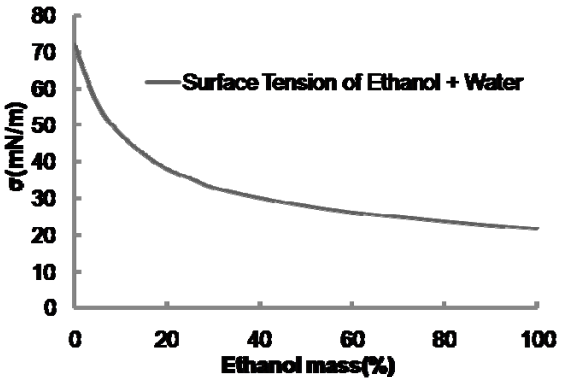

Fig. 3. Surface Tension of Alcohol Water + Water[5]

B. *Equipment*

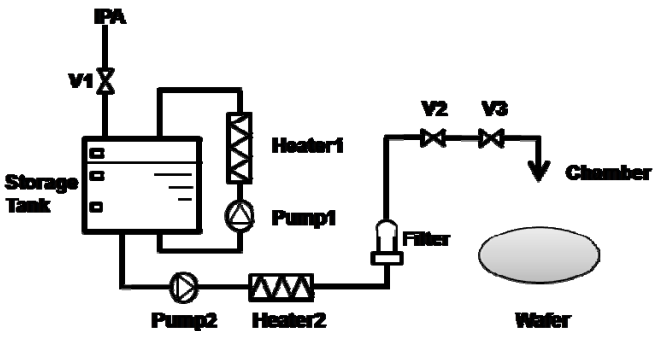

Fig. 4. IPA supply schematic

The experiment equipment was prepared as shown Fig 4. We sprayed IPA on wafer surface during drying step in cleaning process, and make a change of temperature of IPA by using heater pump and circulation line in storage tank.

C. *Method*

The experiment was implemented at the same condition affecting leaning factors, except for the experiment variable. When spraying IPA on the surface of wafer during cleaning process, we made a change on a spin speed of wafer and temperature, then compared the number of occurrence of capacitor leaning per a unit dimensions.

Test 1. Wafer spin speed comparison IPA spray

	Wafer	IPA Spray (rpm)	IPA Temp (°C)	DI Flow (cc)	IPA Time (sec)	Dry (rpm)	Cap Height (□)	Cap Width (□)
Test 1	A	500	25	α	β	γ	δ	ε
	B	300	25	α	β	γ	δ	ε

Test 2. Comparison of IPA spray temperature

	Wafer	IPA Spray (rpm)	IPA Temp (°C)	DI Flow (cc)	IPA Time (sec)	Dry (rpm)	Cap Height (□)	Cap Width (□)
Test 2	C	500	25	α	β	γ	δ	ε
	D	500	75	α	β	γ	δ	ε

D. *Result*

Test 1 and Test 2 showed capacitor leaning after progression. The results were confirmed by Hitachi SEM image Fig. 5. As you can see in the SEM image of the wafer, capacitor leaning more occurs near the edge than near the center.

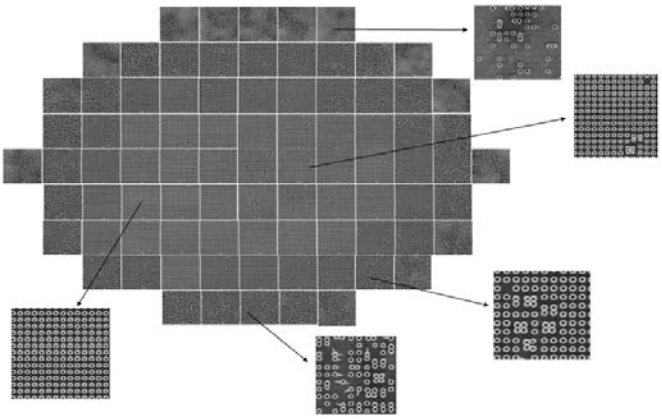

Fig. 5. Capacitor Leaning SEM Image for inspection, Top view.

When spraying IPA on a water surface during drying process, we changed the spin speed of wafer to 300rpm, 500rpm, then the result was shown as Fig. 6.

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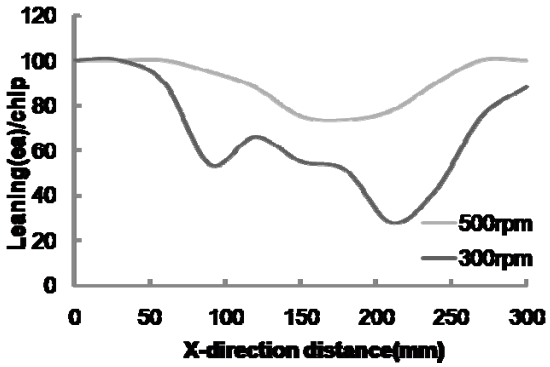

Fig. 6. Spin speed and wafer leaning defect distribution by location.

Fig. 7. shows the number of occurrence of capacitor leaning that occurs, when the temperature of IPA was changed into 25 and 75 degrees Celsius .In the case of C wafer in the experiment 2, the number of capacitor leaning is over 100 per a unit dimension in average. And it is hardly comparable to D wafer that 1 capacitor leaning occurs in average. So It was not drew on the chart. In the case of 75 degrees Celsius test, the number of leaning occurrence was 0.255ea/chip in average. It was uninfluential to operate DRAM in fabrication, and there was almost no difference of the number of leaning between the center and edge.

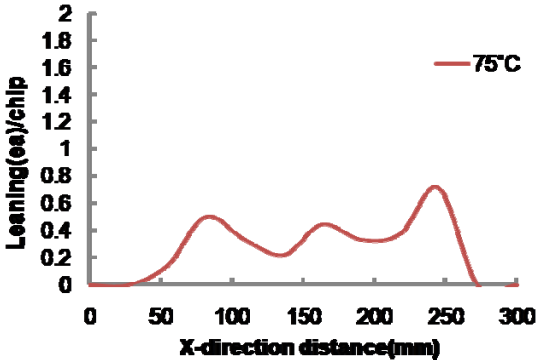

Fig. 7. Temperature and wafer leaning defect distribution by location.

The higher the temperature is, the more the surface tension decreases and the boundary between liquid and gas disappeared at the certain temperature. The thicker a liquid film was, the more the surface tension decreased, however this change slightly influenced a surface tension. Especially, a surface tension of a thin liquid film reacts more sensitively.[6]

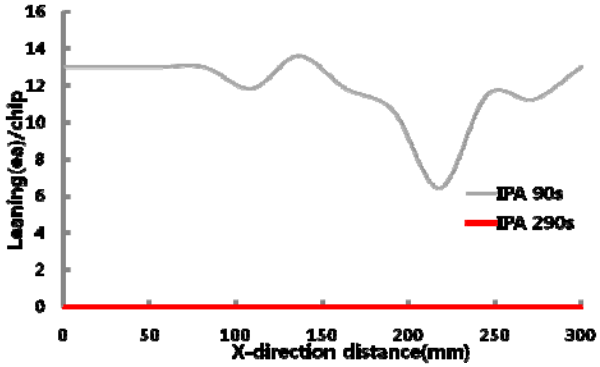

Fig. 8. Processing time and wafer leaning defect distribution by location.

A test 2, D and under the same conditions, When processing time of IPA changed as 90sec, 290sec, the result of leaning distribution was shown as Fig. 8. At the surface of the wafer, IPA was more evaporated then liquid, owing to a low surface tension of IPA. Evaporation is increased, the spinning wafer surface will change the amount of convection in the IPA. Increasing the IPA relative humidity in the surrounding gas during the water–IPA exchange and drying phases, IPA is more effective replacement.

IV. Conclusion and Discussion

In this study of pattern collapse, the impact of temperature and spin speed was confirmed among DRAM capacitors leaning and many factors that affect the IPA process. Firstly the more the temperature increases, the more the number of leaning decreases, and a surface tension of a thin liquid film greatly reacts on a temperature change. Secondly, the more IPA spray speed decreases the more the number of leaning decreases, and that the leaning is more improve on the center of the wafer than the edge of the wafer, is connected with an inertial force by a spin.

The future of semiconductor design rule would be reduced more and more, even getting a place to stand in the capacitor will be reduced. Limit of capacitor aspect ratio should be studied and if the limit is reached, we ought to replace the capacitor by the new way and materials.

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