A Synchronous Rectifier for Isolated Forward DC-DC Converters, Integrated in a High-Voltage Smart-Power IC Technology

Jan Doutreloigne, and Herbert De Pauw

Abstract—**The synchronous rectifier in isolated forward DC-DC converters is traditionally built with discrete DMOS power transistors driven directly from the secondary winding of the pulse transformer. Unfortunately, this technique induces very high switching losses, especially at high switching frequency. This paper presents a new synchronous rectifier topology that drives the DMOS devices in a much more power-efficient manner, employing an additional DC-DC buck converter, and that allows monolithic integration of the whole synchronous rectifier electronics in a suitable high-voltage smart-power IC technology. Special circuitry for suppressing sub-threshold conduction of the DMOS devices is also provided on the chip.**

Index Terms—**DC-DC converter, integrated circuit, forward converter, smart-power technology, synchronous rectifier**

I. Introduction

IN many applications the electronic circuitry is powered by isolated DC-DC converters for safety reasons or other system requirements. Typical examples are the power supplies in central-office ADSL and VDSL telecommunication equipment or the power supply units in Power-over-Ethernet devices. Widely used isolated converter topologies are the fly-back, the forward and the combined forward/fly-back architectures, where the driving electronics at the primary side of the pulse transformer and the rectifying electronics at the secondary side are employing discrete power transistors and/or diodes [1]. When trying to optimize the power efficiency and reduce the physical size of the system, monolithic integration of the driving and rectifying electronics in an appropriate high-voltage smart-power IC technology seems an attractive approach, but the practical IC design is not straightforward. This paper describes the single-chip implementation of the rectifying electronics at the secondary side of the pulse transformer in the specific case of an isolated forward DC-DC converter.

II. Forward DC-DC Converter

The basic architecture of an isolated forward DC-DC converter is shown in Fig.1. Switch 1, actually a power DMOS transistor, is the main driving transistor and is activated during the power transfer phase of the clock cycle. During this power transfer phase, energy is transferred from the primary side of the transformer to the secondary side, and the load current is flowing through the synchronously activated transistor 3, which can be replaced by a diode at the expense of increased conduction losses. The load current is reflected to a proportional current in the primary coil, its precise value being determined by the transformer turns ratio. It's important to note that both windings of the pulse transformer are carrying current simultaneously during this power transfer phase, which is an inherent characteristic of the forward converter in contrast to the fly-back converter. During this same power transfer phase, a magnetization current is also being built up in the primary coil. The maximum value of this current depends on different factors, mainly the primary coil inductance, the supply voltage, the clock period and the duty ratio, but it's typically much smaller than the reflected load current.

After the power transfer phase, the forward converter enters the active clamping phase where the main transistor 1 is switched off and power isn't transferred anymore from the primary to the secondary side. The load current is now flowing through the synchronously activated transistor or diode 4, acting as a free-wheeling device. The reflected load current isn't present anymore in the primary coil of the pulse transformer, and the magnetization current of the primary coil now has to flow through the branch with the clamping capacitor C and the additional DMOS transistor 2. An appropriate voltage is automatically being built up in this clamping capacitor, creating a polarity inversion of the voltage across the primary coil, so that in steady-state circumstances the magnetization of the primary coil during the power transfer phase is perfectly compensated by the demagnetization of the coil during the active clamping phase of the same clock cycle. The exact value of the voltage on the clamping capacitor depends on the supply voltage of the circuit, and more important, also on the duty ratio of the clock signal.

Due to the presence of the LC low-pass filter, having a 3dB cut-off frequency much below the switching frequency, the converter produces an almost perfect DC output voltage equal to the supply voltage of the primary circuit, multiplied by the transformer turns ratio and the duty ratio of the clock signal.

Manuscript received July 22, 2012; revised August 5, 2012.

Jan Doutreloigne and Herbert De Pauw are with the Centre for Microsystems Technology (CMST), affiliated to the Interuniversity Microelectronics Centre (IMEC) and the University of Gent, Technologiepark 914A, 9052 Zwijnaarde, Belgium (phone: +32-(0)9-264-53-56; fax: +32-(0)9-264-53-74; e-mail: jdoutrel@elis.ugent.be).

ISBN: 978-988-19252-4-4
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

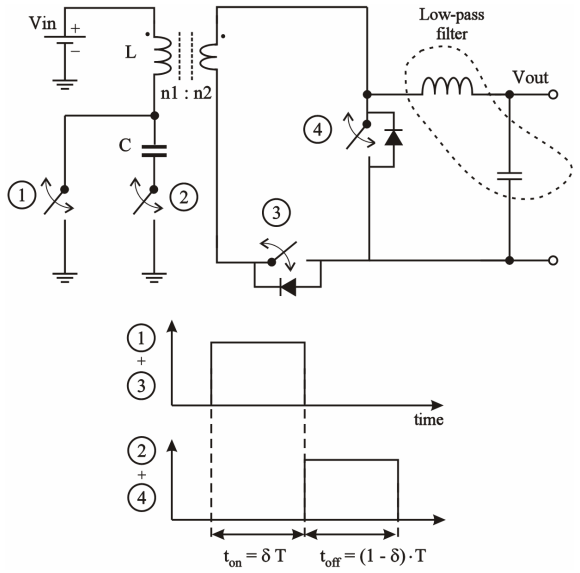

Fig.1. Basic architecture of an isolated forward DC-DC converter.

III. Basic Synchronous Rectifier Circuit

A conventional discrete implementation of the synchronous rectifier at the secondary side of the pulse transformer is depicted in Fig.2. It corresponds to the specific application of a forward DC-DC converter with 48V supply voltage at the input of the pulse transformer and a maximum of 7A load current at a DC output voltage of 12V, as used in central-office ADSL and VDSL telecommunication equipment. The devices nDMOS1 and nDMOS2 correspond to the switches 3 and 4 from Fig. 1. When the pulse transformer produces a positive voltage at its output, the gate of nDMOS1 will be charged directly from the secondary transformer winding through the bipolar transistor NPN1 to a voltage determined by the Zener diode Z1. As a result, nDMOS1 will be in the ON-state, thereby carrying the entire load current at a very small voltage drop. As soon as the voltage polarity at the transformer output has been reversed, the gate of nDMOS1 will be rapidly discharged through diode D1, and consequently nDMOS1 will enter the OFF-state. At the same time, a similar driving circuit will turn on nDMOS2 that will act as an almost ideal free-wheeling diode for the entire load current.

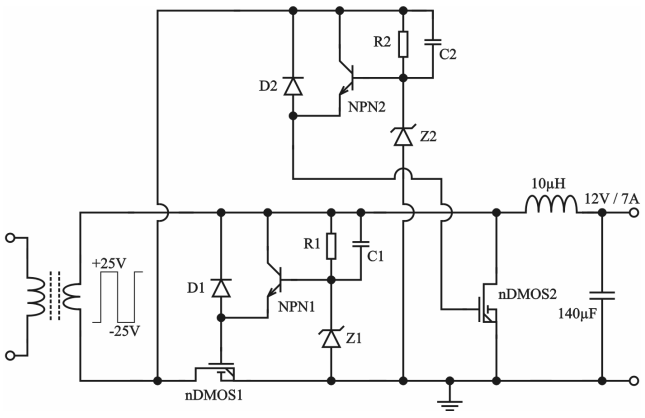

Fig.2. Basic synchronous rectifier circuit.

In an attempt to reduce the total size of the forward DC-DC converter and to improve the overall power efficiency of the system, we looked into the possibility of integrating the synchronous rectifier circuit of Fig.2 into a single silicon chip. In view of the rather high voltage levels at the output of the pulse transformer, a special high-voltage smart-power IC technology is needed. Based on precise system requirements and constraints, we chose the I3T80 smart-power technology from ON Semiconductor, which is an 80V extension of a 0.35µm CMOS process.

As a starting point, several Spectre simulations were carried out on the circuit of Fig.2 in this I3T80 smart-power technology for different channel dimensions of the 2 main transistors nDMOS1 and nDMOS2. The graph of Fig.3 shows the simulated power efficiency of the basic synchronous rectifier at 7A@12V load conditions, for different chip sizes and different values of the switching frequency. Note that the active switches nDMOS1 and nDMOS2 are by far the dominant components in the total chip size.

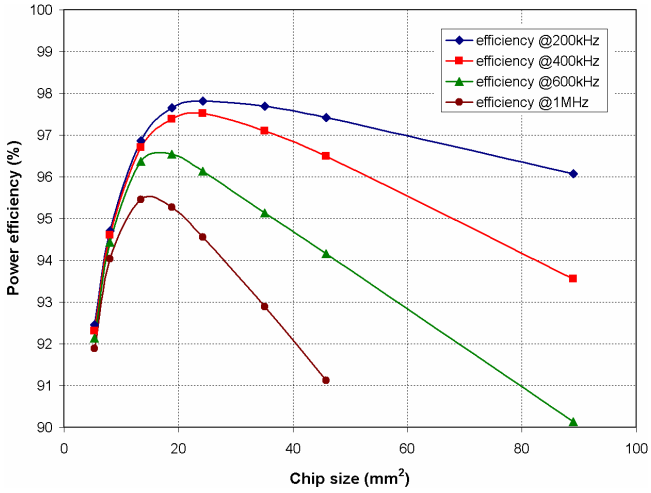

Fig.3. Simulated power efficiency of the basic synchronous rectifier for different chip sizes and switching frequencies.

The shape of the curves in Fig.3 is actually quite logical. Initially, the power efficiency rises steeply for increasing values of the nDMOS channel width because the channel resistance and hence also the static power dissipation in the nDMOS are inversely proportional to this channel width. However, as the channel width goes up, also the gate capacitance of the nDMOS increases, thereby requiring more power in the NPN bipolar transistors to periodically charge this gate capacitance at the switching rate. At a certain critical value of the channel width, this dynamic dissipation in the NPN devices becomes more important than the static dissipation in the nDMOS devices, and from that point on, the power efficiency begins to drop. The higher the switching frequency, the sooner this critical point is reached (because the dynamic losses in the NPN transistors are proportional to the switching frequency) and the steeper the curve will drop.

The contribution of the static dissipation in the nDMOS and dynamic dissipation in the NPN devices is also clear from Table I, where the parameter M_nDMOS is a

ISBN: 978-988-19252-4-4
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

multiplier that defines the total effective channel width of the devices nDMOS1 and nDMOS2. Only for rather small values of the nDMOS channel width in combination with a moderate switching frequency, the static nDMOS dissipation is predominant. For very wide nDMOS channels and/or high switching frequencies, the dynamic NPN dissipation has the main impact on power efficiency.

This table leads to a very important conclusion: if we want to improve the power efficiency of the synchronous rectifier at high switching frequencies, we should find a way to reduce the dynamic power losses in the NPN transistors without deteriorating the static losses in the nDMOS devices. In other words, we should look for a circuit solution that reduces the energy needed to charge the gate capacitance of the nDMOS devices without actually reducing the size of these devices!

TABLE I. CONTRIBUTION OF DIFFERENT TRANSISTORS IN THE TOTAL POWER DISSIPATION FOR DIFFERENT NDMOS SIZES AND SWITCHING FREQUENCIES.

	Average power dissipation (mW)		
Component	M_nDMOS = 100 @ 200kHz	M_nDMOS = 800 @ 200kHz	M_nDMOS = 200 @ 1MHz
nDMOS1	**1120**	360	890
nDMOS2	**1130**	460	910
NPN1	70	**1240**	**1540**
NPN2	70	**1240**	**1530**

IV. DYNAMIC POWER LOSS REDUCTION

When looking at the way the gate capacitance of the nDMOS transistors is being charged by the NPN bipolar transistors in the circuit of Fig.2, it becomes clear that this is done very inefficiently. Indeed, the gate of the nDMOS devices is charged to about 3.3V, being the maximum allowed gate voltage in this 0.35μm I3T80 technology, but this is done through the NPN devices from a 25V power supply (the voltage across the secondary winding of the pulse transformer)! From an energetic point of view, this is a very bad strategy. To illustrate this and to show how we can improve things considerably, let's have a look at Fig.4.

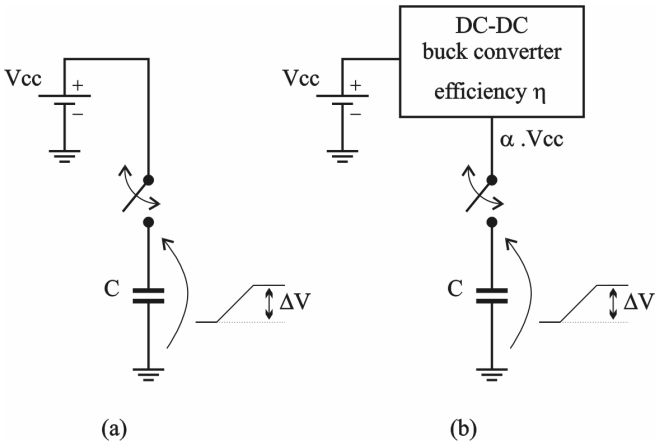

Fig.4. Principle of dynamic power loss reduction.

In circuit (a), the capacitor is charged an amount ΔV from a much higher supply voltage V_{cc} through some solid-state switch. In the circuit of Fig.2, ΔV would be 3.3V, V_{cc} would be 25V, and the switch the NPN bipolar transistor. A very simple calculation shows that the corresponding energy delivered by the supply voltage V_{cc} during the charging process is given by:

$$\Delta E = C \cdot V_{cc} \cdot \Delta V$$

In configuration (b), however, the supply voltage V_{cc} is first down-converted to a level $\alpha \cdot V_{cc}$ slightly above the needed range ΔV (in Fig.2, $\alpha \cdot V_{cc}$ could be e.g. 4V, leaving some margin), and this is done by means of a power-efficient switching DC-DC buck converter having a power efficiency η (e.g. 80%). In this case, the energy delivered by the source V_{cc} during the whole charging process will be given by:

$$\Delta E = \frac{\alpha \cdot C \cdot V_{cc} \cdot \Delta V}{\eta}$$

When we substitute the above mentioned values that correspond to the circuit of Fig.2 into these formulas, we see that the energy consumption in configuration (b) is 5 times less than in the case of configuration (a)! This seems a very interesting approach for boosting the power efficiency of the synchronous rectifier at high switching frequencies and/or for large nDMOS devices. In this way, the original circuit from Fig.2 is transformed into the improved circuit of Fig.5. In this new version, the auxiliary supply voltage of 4V is not directly derived from the 25V transformer voltage, but from the 12V output voltage instead. During start-up, when the output is still far below the desired 12V, the DC-DC buck converter won't operate properly, and hence, the 2 nDMOS devices will entirely rely on their built-in drain-bulk diodes for rectifying the voltage from the pulse transformer. As the output voltage begins to rise, the DC-DC buck converter comes into action, and consequently, the nDMOS devices get activated with a high degree of power efficiency.

A possible implementation of the DC-DC buck converter is depicted in Fig.6. Transistor pDMOS1 is the main switch in this buck converter, while the other transistors form the level-shifter for driving the gate electrode of this switch. The voltage mirror nDMOS1 + FpMOS1, where nDMOS1 is driven by a 1MHz clock signal with 40% duty ratio and FpMOS1 acts as a non-linear active load, directly controls the source-gate voltage of pDMOS1. The additional voltage mirror nDMOS2 + FpMOS3, driven by the complementary clock signal, in combination with FpMOS2, effectively discharges the gate capacitance of pDMOS1 in order to avoid leakage current in the switch during the OFF-state. The simple DC-DC buck converter circuit of Fig.6 was also designed in the I3T80 technology from ON Semiconductor and according to detailed Spectre simulations it converts the 12V into 4V at approximately 80% power efficiency for the output current levels that are needed to drive the 2 NPN bipolar transistors in the synchronous rectifier circuit of Fig.5.

ISBN: 978-988-19252-4-4
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

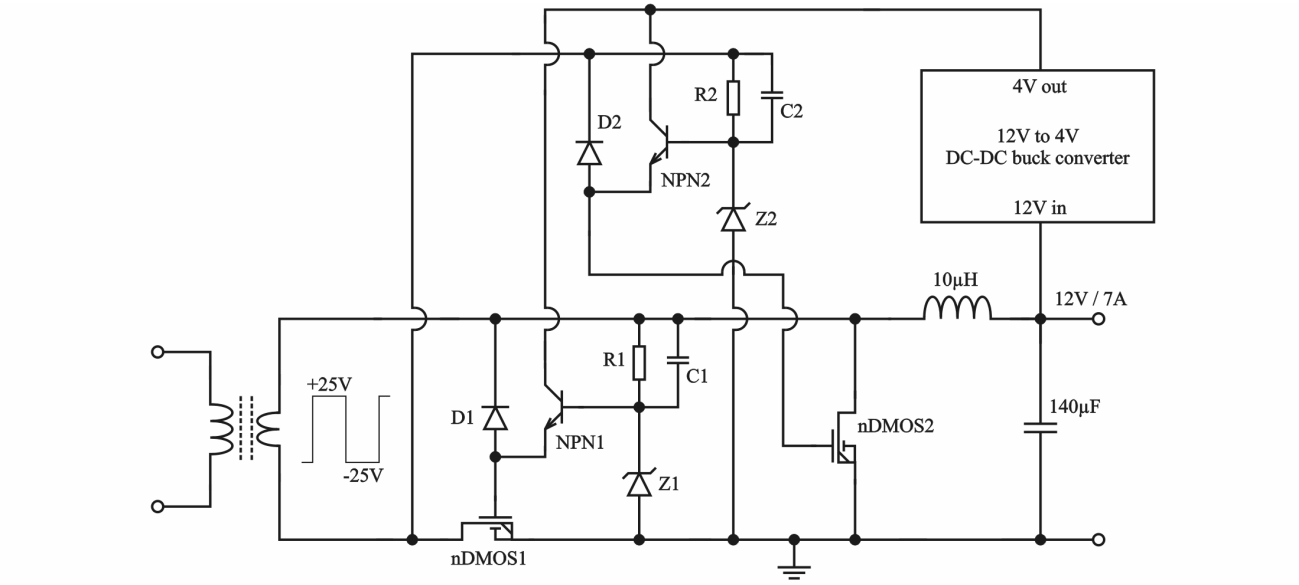

Fig.5. Synchronous rectifier with reduced dynamic power losses.

The impact of this technique to reduce the dynamic switching losses is really astonishing, as evidenced by the simulated data in Table II. In those situations where the dynamic losses in the NPN devices were predominant in the power consumption of the original circuit (for very large nDMOS devices and/or high switching frequencies), the introduction of this new technique makes the dynamic losses in the NPN devices only marginal compared to the static losses in the nDMOS transistors! Note that the additional average power consumption of about 170mW in the active components of the 12V to 4V DC-DC buck converter are taken into account in the Spectre simulation of the efficiency in Table II.

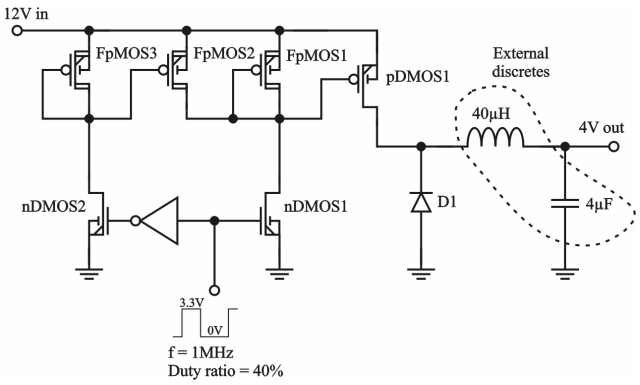

Fig.6. Schematic of 12V to 4V buck converter.

V. Sub-Threshold Current Reduction

Further improvement of the power efficiency should focus on the reduction of the static dissipation in the nDMOS transistors. Hence, we investigated the nDMOS behaviour in the synchronous rectifier of Fig.5 more thoroughly and discovered something peculiar: the nDMOS devices are dissipating as much power during the OFF-state as during the ON-state! This may seem hard to believe, but the cause can be found in unexpected sub-threshold conduction of the nDMOS. Indeed, when nDMOS2 in Fig.5 is activated (acting as freewheeling diode for the load current), its drain potential reaches a value of 50 to 100mV below ground (depending on the actual channel width). As a consequence, the gate electrode of nDMOS1 is discharged through diode D1 to a level at one diode threshold above the drain potential of nDMOS2. In other words, the gate of nDMOS1 is not entirely discharged to ground but to a level of approximately 0.4V. This is only slightly below the nDMOS threshold voltage, which is typically 0.5V for the chosen transistor type. Due to the very wide transistor channel, this gate voltage triggers a considerable sub-threshold current of several mA. As the source-drain voltage of nDMOS1 is roughly 25V at that moment, this sub-threshold current can easily cause a static power dissipation of hundreds of mW, comparable to the static power consumption during the ON-state of the device (when the drain current is much higher, around 7A, and the drain voltage much lower, in the range from 50 to 100mV)! This is confirmed by the simulations in Table III, proving that the static dissipation in the OFF-state of the nDMOS can indeed be as large as during the ON-state.

TABLE II. Impact of Dynamic Power Loss Reduction on Transistor Power Dissipation and Global Power Efficiency.

Component	Average power dissipation (mW)			
	M_nDMOS = 800 , @ 200kHz		M_nDMOS = 200 , @ 1MHz	
	Basic circuit	Improved circuit	Basic circuit	Improved circuit
nDMOS1	360	370	890	850
nDMOS2	460	510	910	860
NPN1	**1240**	**160**	**1540**	**180**
NPN2	**1240**	**160**	**1530**	**180**
Global power efficiency	**96,1%**	**98,1%**	**94,6%**	**97,0%**

ISBN: 978-988-19252-4-4
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

TABLE III. STATIC NDMOS POWER DISSIPATION DURING ON- AND OFF-STATE.

	ON-state	OFF-state
Vgs	3.3V	400mV
Vds	45mV	25V
Id	7A	13mA
Dissipation	**315mW**	**325mW**

The technique to avoid sub-threshold conduction of the 2 nDMOS transistors is fairly straightforward. As the 2 transistors operate in a complementary way, the one being turned off when the other is turned on, we can use the gate signal of one nDMOS to discharge the gate electrode of the other, simply by adding a pair of small low-voltage nMOS transistors. This leads to the schematic of Fig.7. When nDMOS2 is activated, its gate being charged to about 3.3V, the additional low-voltage transistor nMOS1 (marked by an arrow) will be turned on, resulting in the complete discharging of the gate electrode of nDMOS1 and eliminating the sub-threshold current. The same occurs when activating nDMOS1.

The effectiveness of this technique to avoid sub-threshold conduction is clearly evidenced by Spectre simulations. The gate electrode of the nDMOS is now completely discharged to 0V instead of sticking at 0.4V, and the corresponding drain current has dropped to less than 1mA instead of the 13mA we observed before. Fig.8 represents the simulated global power efficiency of the synchronous rectifier from Fig.7 for different chip sizes and switching frequencies, and compares it to the data that correspond to the original circuit from Fig.2.

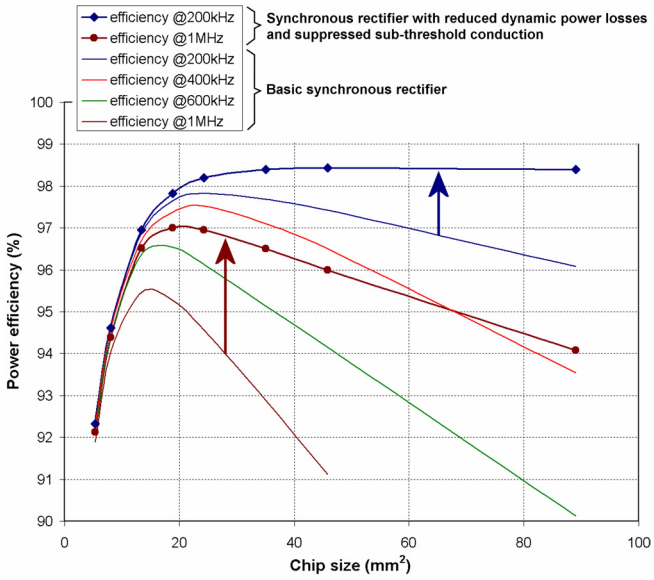

Fig.8. Simulated power efficiency of the synchronous rectifier with reduced dynamic power losses and suppressed sub-threshold conduction (+ comparison with basic synchronous rectifier) for different chip sizes and switching frequencies.

This comparison reveals the superior performance of the circuit from Fig.7. When looking at a switching frequency of 1MHz, the original circuit yielded a maximum efficiency of 95.5%, whereas the introduction of the techniques for dynamic power loss reduction and suppression of sub-threshold conduction boosts the power efficiency to 97.0%! At frequencies above 1MHz, the efficiency increase would be even more pronounced.

Two versions of the optimized synchronous rectifier circuit of Fig.7 have been integrated in the 80V 0.35µm I3T80 smart-power technology of ON Semiconductor. Both prototypes were designed to be used in the isolated forward DC-DC converter for the central-office ADSL and VDSL application, operating from a 48V supply voltage and capable of delivering a maximum current of 7A into the

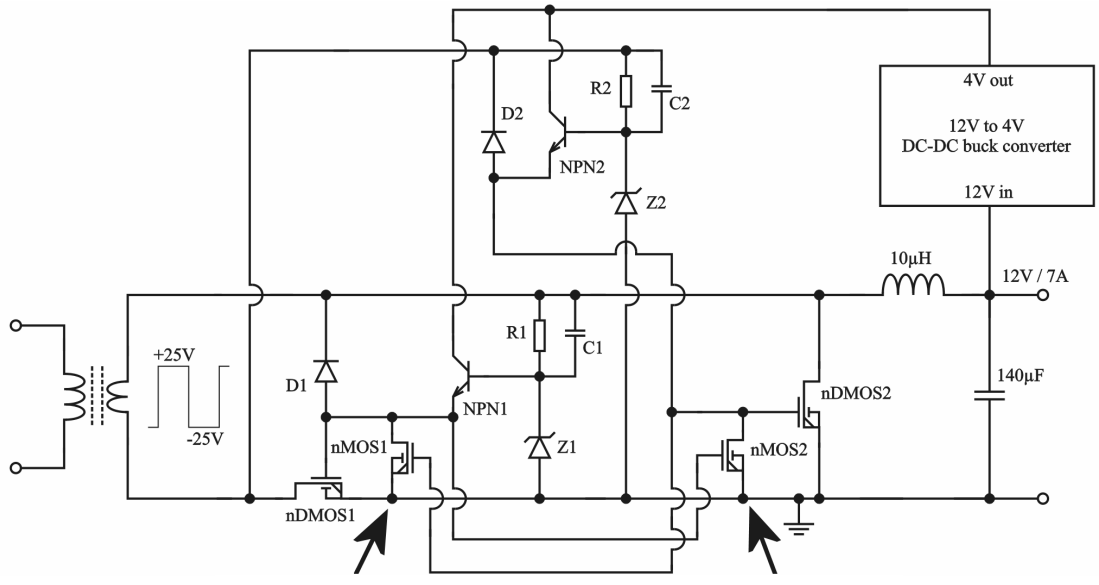

Fig.7. Synchronous rectifier with reduced dynamic power losses and suppressed sub-threshold conduction.

ISBN: 978-988-19252-4-4
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

load at 12V DC output voltage. Experimental results of both prototypes will be presented at the conference.

VI. Conclusion

A new synchronous rectifier circuit for isolated forward DC-DC converters was presented. A special DMOS driving technique, employing an additional DC-DC buck converter, reduces the dynamic switching losses and boosts the power efficiency considerably. The circuit is suitable for monolithic integration of the synchronous rectifier in a smart-power IC technology and provides effective suppression of DMOS sub-threshold conduction.

References

[1] L. Bor-Ren, "Analysis, design, and implementation of an active clamp forward converter with synchronous rectifier," *IEEE Transactions on Circuits and Systems I*, vol. 53, no. 6, pp. 1310-1319, 2006.

ISBN: 978-988-19252-4-4
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)