Scalable Pulsed Computational Module Using Integrate and Fire Structure and Margin Propagation Algorithm

Thamira Hindo *

***Abstract*—In this paper a novel circuit is proposed for pulse-based logarithmic computation using integrate-and-fire (IF) structures. The smallest unit in the module is a network of three IF units that implements a margin propagation (MP) function using integration and threshold operations inherited in the response of an IF neuron. The three units are connected together through excitatory and inhibitory inputs to impose constraints on the network firing-rate. The MP function is based on the log likelihood computation in which the multiplication of the inputs is translated into a simple addition. The advantage of using integrate-and-fire margin propagation (IFMP) is to implement a complex non-linear and dynamic programming functions of spike based (pulse based) computation in a modular and scalable way. In addition to scalability, the objective of the proposed module is to map algorithms into low power circuits as an attempt to implement signal processing applications on silicon. The paper shows the mechanism of IFMP circuit, dynamic characteristics, the cascaded modularity, and finally a verification of the algorithm in analog circuit using standard $0.5\mu m$ CMOS technology.**

***Index Terms*—Integrate and fire, excitatory, inhibitory, pulse mode computation, margin propagation, log-sum-exp.**

I. Introduction

Although Von Neumann computer architecture perform high speed computation and communication but they are unable to perform brain tasks processes in an efficient way such as the biological sensing in the retina and cochlea. A new trend in computer architecture for applications other than precise, high speed calculation and efficient communications is now in the fourth generation of research work to built up a neuromorphic systems. The goal of the neuromorphic systems is to implement sensory devices in an efficient way as in the biological sensors [1], [2], [3], [4], [5]. The architecture of the morphed biological systems are different from the traditional Von Neumann architecture such as asynchronous- parallel processing instead of synchronous-single processing, hybrid computation instead of digital computation, neuron model as a basic core of the processing instead of the arithmetic logic unit and finally, analog VLSI design instead of digital VLSI. As a contribution in this huge project, a novel and scalable algorithm is proposed to approximate non-linear function as an important procedure to implement signal processing algorithms in the sensory applications such as recognition and classification. The main objective of this work is to map a pulsed mode algorithm into low power silicon circuits as an attempt to implement signal applications in the neuromorphic systems.

The proposed module has three concepts, the first concept is to map the non-linear functions into margin propagation "MP" [6] which is an approximation function to the log -sum - exp (LSE) expression. The second concept of the proposed module is based on an integrate and fire neuron model. The third concept is to implement the non-linear function in pulse stream mode. The proposed pulse mode computation module is abbreviated as "IFMP" since it implements a MP function using IF neuron model.

For the first concept, the LSE math function is used in factor graph algorithms in which the sum of product terms are used [7]. In these algorithms, the probabilities or the marginal functions of passing messages are evaluated between the nodes and variables of a factor graph. Since the product of probability terms tend to decrease as the number of probability terms increase, then we would have a problem of underflow that cause false computations. Therefore, such algorithms use the log-likelihood computation to eliminate the underflow problem as well as to increase the dynamic range of variables in the computation process. But the representation of LSE is not scalable in hardware design. Therefore the margin propagation function (scalable function in hard ware design) is used as an approximation method to the LSE function. The concept of margin propagation (MP) algorithm is based on the idea of reverse water-filling (RWF) algorithm, [8]. Given a set of random inputs (scores) $L_i \in R; i = 1 : m$, the RWF algorithm computes the solution z according to the constraint,

$$\sum_{i=1}^{m}[L_i - z]_+ = \gamma \tag{1}$$

where $[.]_+ = max(., 0)$ denotes a threshold operation and $\gamma \geq 0$ represents a parameter of the algorithm. Note that z is in the log domain. The solution of the equation 1 is represented by z, where z can be written in LSE and MP forms as ,

$$z = log(\sum_{i=1}^{m} e^{L_i} \simeq M(L_1, L_2, L_3....L_m, \gamma) \tag{2}$$

Where M denotes as the MP function, m denotes the number of the input operand. In previous work [9], it was proven that MP is successfully an approximation method to LSE. The input/output variables in the above work are represented as currents, also the computation procedure is implemented using kirchoffs current law. MP was

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Thamira Hindo is a Phd candidate in the Department of Electrical and Computer Engineering, Michigan State University, East Lansing , MI, 48824 USA e-mail: (hindotha@msu.edu)

implemented in [9] to achieve scalability in the decoding algorithms. In this work, we introduce the concept of MP propagation as an approximation method to LSE in pulse computation mechanism.

Secondly, the structure of the proposed module is based on an integrate and fire (IF) neuron model that implement integration and threshold operation. Since the IF model is a simple representation of a neuron", it is extensively used as a neuron model in spiking neural networks [10], [11], [12] and neuromorphic systems [13], [4]. The IF neuron itself is the basic computational unit in the sophisticated and efficient architecture, "the brain".

The brain is the most realistic example of an efficient system, "hybrid system", which is the third concept of the proposed module. The type of the signals (data) transferred in the brain is mixed between digital as spikes (pulses) and analog as the variable time between these spikes. The above signal processing is called pulse stream mode or hybrid computations [14], [15]. Hybrid (pulse) computation is a promising research topic since it mixes the advantages of analog and digital designs. The noise accumulation in analog stages can be eliminated by digital noise immunity. The analog design has the advantage of small area, low cost and low power especially if the design of computational units is implemented in weak inversion mode of complementary metal oxide semiconductors (CMOS). Fig. 1 shows the flow of the proposed module which includes manipulating the input pulse rate (scaling and converting into logarithm domain), mapping the function into MP and evaluate the output z, then scaling back and calculating the exponent of z to realize the function.

The concept of the proposed algorithm is analysed and synthesised, proved theoretically, mapped and verified into a low power analog circuit, implemented in applications and finally verified on $0.5\mu m$ process chip. This paper is organized as following: In section II, the analysis, synthesis and dynamic characteristics of the IFMP module is explained as well as the mathematical proofs of rate convergence in IFMP are demonstrated in appendix A and B. Section III is the circuit description and hard ware verification of IFMP. Section IV is to conclude the paper with the future work.

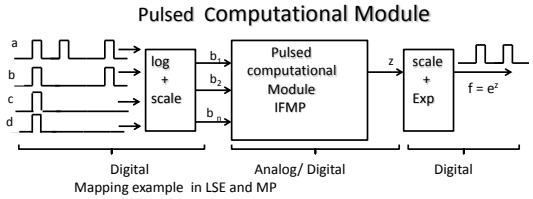

Fig. 1: Input/output stages in the pulsed computational module.

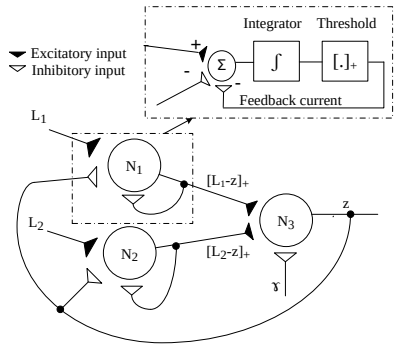

Fig. 2: Schematic of the proposed IFMP unit comprising of three integrate-and-fire modules.

II. IFMP: CONCEPTS AND ANALYSIS

Fig. 2 shows a schematic diagram of the proposed spiking network module. The network is referred to as an IFMP module and consists of three integrate-and-fire structures N_1, N_2 and N_3. The excitatory/inhibitory inputs are represented by black /white triangles. Units N_1 and N_2 have self-inhibitory feedback connections and unit N_3 has inhibitory input denoted as γ. Given the rate of input spike-trains $L_1[n]$ and $L_2[n]$ with n being a discrete time-index, it can be shown that firing-rate of the output $L_z[n]$ (denoted by $\mathcal{E}(L_z) = \lim_{T\to\infty} \frac{1}{T}\sum_{n=1}^{T} L_z[n]$) asymptotically satisfies the following equation,

$$[\mathcal{E}(L_1[n]) - \mathcal{E}(L_z[n])]_+ + [\mathcal{E}(L_2[n]) - \mathcal{E}(L_z[n])]_+ \longrightarrow \mathcal{E}(\gamma[n]) \tag{3}$$

and in general for m inputs,

$$\sum_{i=1}^{m} [\mathcal{E}(L_i[n]) - \mathcal{E}(L_z[n])]_+ \longrightarrow \mathcal{E}(\gamma[n]) \tag{4}$$

Note that equation 4 converges only in probability. The difference between the left and right hand side of the above equation decreases as the time increases (or the number of stream sequence of random inputs increases) and hence the summation of the expected values of the input stream converges to the expected values of the output stream. In order to prove the convergence of IFMP equation 4 (Appendix B), it must be first proof the convergence of one neuron (Appendix A) such that the expected value of output spikes $d[n]$ is equal to the expected value of the input spike $L[n]$ overall the samples,

$$\mathcal{E}_n\{L[n]\}_+ = \mathcal{E}_n\{d[n]\} \tag{5}$$

Fig. 4 shows the plot of instantaneous spiking-rates for N_1,N_2 and N_3, when input rate of the inputs are varied as shown in Fig. 4 (below). In this experiment, $\gamma = 0.3$ and the input rate $L_2 = 0.5$ for N_2 while input rate L_1 for N_1 increases from 0 to 1. The dynamic of the figure follows the IFMP equation 4 such that $[L_1 - z]_+ + [L_2 - z]_+ = \gamma$. Initially, when L_1 is between 0 and 0.25, then the output rate of N_1, N_2 and N_3 is equal to $0,\ 0.3$ and 0.2 respectively. When L_1 is 0.3, then the output rate of units N_1, N_2 and N_3 are $0.05, 0.25$ and 0.25 respectively. When L_1 is 0.6, then the output rate of units N_1, N_2 and N_3 are $0.2, 0.1$ and 0.4

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respectively and so on. Hence, the sum of the output rates for the first two IF units N_1, N_2 converges to a constrain rate γ over enough and sufficient time for convergence in which the dynamics of IFMP satisfies equation 4 as shown in Fig. 4.

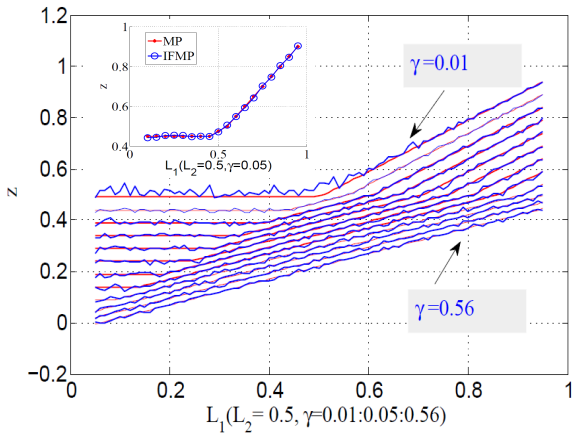

Fig. 3: Dynamic characteristics of IFMP unit for different values of γ for MP and IFMP (the analog mode and pulse mode of MP respectively).

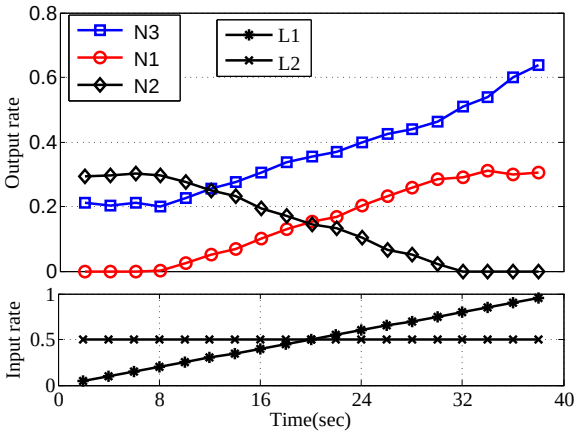

Fig. 4: Spike-rates for neurons N_1, N_2 and N_3 (upper fig) when the spike-rate of L_1 is monotonically increased, The rate L_2 is kept constant at 0.5 (lower fig).

Fig.3 shows the plot of instantaneous spiking-rates for N_3, when spiking-rate of the input rate L_1 is varied from 0.01 to 0.99. For this result, the spiking-rate for input L_2 is kept constant to 0.5 as γ changes from $0.01 : 0.05 : 0.56$. The plot shows that the spiking-rate of N_3 increases according to a piece-wise linear approximation to the margin propagation function.

It was shown in [9] that the margin propagation (MP) is an approximation to the log-sum-exp. However, they did not provide close form representation for the approximation and the parameters involved. Furthermore, they did not demonstrate the efficacy of cascading the approximated model. To address the issues above, we state the followings:
Let $L_1, L_2..L_m$ denote to the input pulse rates to the IF units of Fig. 2 [m=2 for this fig], and let $z_{LSE} = log(\sum_i^m e^{L_i})$ is a solution to

$$\sum_i^m e^{[L_i - z_{LSE}]_+} = 1 \tag{6}$$

where $\{z_{LSE} : R^m \longrightarrow R\}$, then using the fact that

$$e^{[L_i - z_{LSE}]} \geq [1 + L_i - z_{LSE}]_+$$

We can say that,

$$\sum_i^m [1 + L_i - z_{LSE}]_+ \geq 1 \tag{7}$$

To make normalization ideal, the above equation equates to one,

$$\sum_i^m [1 + L_i - z_{LSE}]_+ = 1 \tag{8}$$

$$\sum_i^m [L_i - z_{MP}]_+ = 1 \tag{9}$$

where z_{MP} is the approximated MP value to the LSE as $z_{MP} = z_{LSE} - 1$

If normalization factor changes to $z_{LSE}/\gamma = log(\sum_i^m e^{(L_i/\gamma)})$ as a solution to

$$\sum_i^m e^{[L_i - z_{LSE}]/\gamma} = 1 \tag{10}$$

MP is approximated as following, (see Fig. 6-a)

$$\sum_i^m [L_i - z_{LSE} + 1]_+ \geq 1 \tag{11}$$

$$\sum_i^m [\gamma + L_i - z_{LSE}]_+ \geq \gamma \tag{12}$$

$$\sum_i^m [\gamma + L_i - z_{LSE}]_+ = \gamma \tag{13}$$

$$\sum_i^m [L_i - z_{MP}]_+ = \gamma \tag{14}$$

such that $z_{MP} = z_{LSE} - \gamma$

Fig. 5 shows the above approximation which is equal to γ between z_{LSE} and z_{MP}, z_{IFMP} where $z_{IFMP} = z_{MP}$

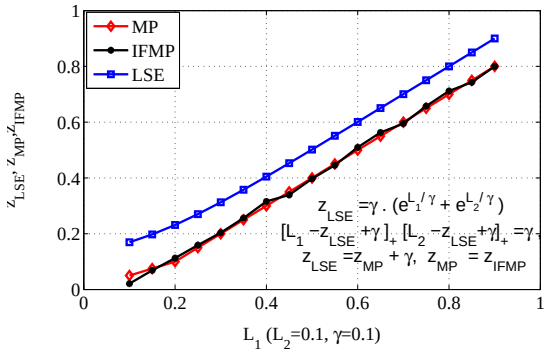

Fig. 5: Approximation of rate z between the log-sum-exp rate (z_{LSE}), Margin Propagation rate (z_{MP}) and Integrate-Fire Margin Propagation (z_{IFMP}).

The MP formulation can be mapped onto a cascaded topology by rewriting the LSE equation $z_{LSE} = log(\sum_i^m e^{(L_i)})$ in a recursive form as following,

$$z_{LSE[m]} = log(\sum_i^{m-1} e^{(L_i)} + e^{(L_m)}) \tag{15}$$

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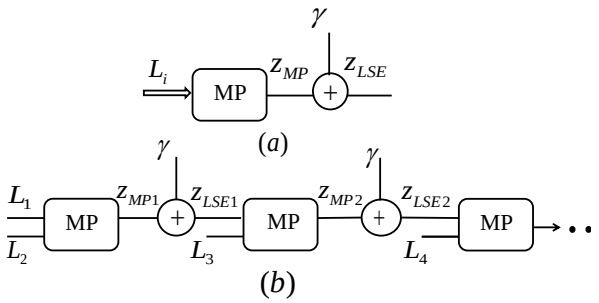

Fig. 6: (a): Approximation of IFMP to the LSE math function. (b): Serial cascading or (modularity) of IFPM structure.

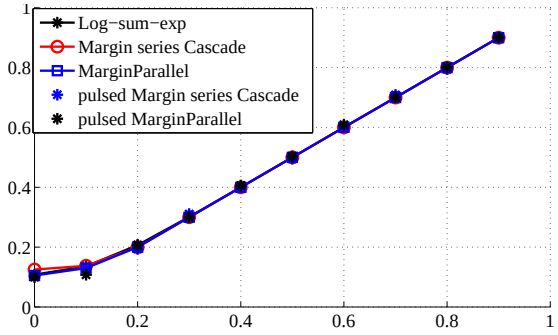

Fig. 7: Dynamic characteristics of pulsed serial and parallel cascaded architecture of the IFMP modules compared to the LSE function MP. The y-axis represents the output rate (z) for different cases showed in the legend. The x-axis represents the change of input rate for one input while keeping the rate of other input constant.

$$z_{LSE[m]} = log(e^{log(\sum_i^{m-1} e^{(L_i)})} + e^{(L_m)}) \quad (16)$$

$$z_{LSE[m]} = log(e^{(z_{LSE[m-1]})} + e^{(L_m)}) \quad (17)$$

Above is the recursive equation for LSE. Now, Let's derive the equations of MP cascading shown in Fig. 6-b. For the first MP unit,

$$[L_1 - z_{MP1}]_+ + [L_2 - z_{MP1}]_+ = \gamma \quad (18)$$

Let $L_2 = -\infty$ for the sake of clarity to show the cascading property. It was shown earlier that $z_{LSE} = z_{MP} + \gamma$ then for the second block,

$$[z_{LSE1} - z_{MP2}]_+ + [L_3 - z_{MP2}]_+ = \gamma \quad (19)$$

$$[z_{LSE1} - [z_{LSE2} - \gamma]]_+ + [L_3 - [z_{LSE2} - \gamma]]_+ = \gamma \quad (20)$$

$$[z_{LSE1} - z_{LSE2} + \gamma]_+ + [L_3 - z_{LSE2} + \gamma]_+ = \gamma \quad (21)$$

Denote $z_{LSE[n]}$ and $z_{LSE[n-1]}$ are equal to z_2 and z_1, then

$$[z_2 - z_1 + \gamma]_+ + [L_3 - z_1 + \gamma]_+ = \gamma \quad (22)$$

Equation 22 shows that three inputs MP can be implemented using two identical units of MP which is applicable for higher number of inputs too as shown in Fig. 6-b. The advantage of cascading is that the algorithms can be implemented using array of 2-IFMP units integrated on silicon while the connectivity could potentially be achieved using an FPGA. Therefore, we do not have to redesign the hardware for different applications. Fig. 7 shows the match in the response of LSE, MP function for both serial and parallel cascaded architecture as well as the IFMP topology for both cases as well.

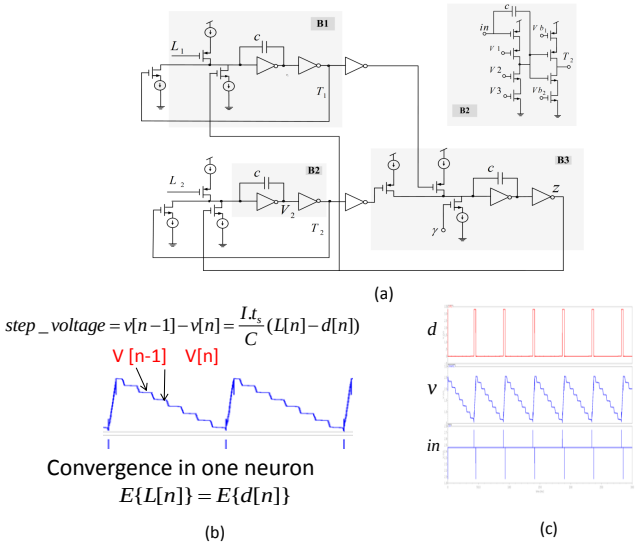

Fig. 8: (a): Schematic circuit of the IFMP model, (b): The membrane voltage of block B1 and the convergence equation between the input and output rates for one neuron, (c): output pulses of block B1 (d), the membrane voltage at the output of the integrator (v), and input voltage of the integrator (in).

III. IFMP: CIRCUIT DESCRIPTION

The analog circuit of IFMP is shown in Fig.8-a. The shaded area round blocks B1, B2 ,and B3 represent units N1, N2 and N3 of Fig. 2 respectively. Block B2 in the upper right of Fig.8-a represents the circuit of the integrator and inverter for the three blocks B1, B2 and B3. Fig.8-b shows the response of the membrane voltage and the convergence equation between the input and output rates for one neuron (represented by block B1 in Fig.8-a). Fig.8-c shows the output pulses (d), membrane voltage (v) and input voltage (in) of the integrator in Block B1.

The integration and threshold are designed between two bounds $(2.34v, 0.9v)$. Initially, if the input of the integrator is zero, the outputs of the integrator and the cascoded inverter are equal to 3.3 and zero volts respectively. If the input voltage increases and reaches the high gain region of integrator amplifier $(60db)$, then the integration phase will be built which is the discharging phase of the capacitor. The input current is integrated and the output voltage of the integrator discharges to the lower bound. At this point, the output of the cascoded inverter turned into logic one which will turn the output voltage of the integrator to the upper bound (charging phase of capacitor). The cycle of charging and discharging the capacitor C is repeated according to the amount of the current injected to the inputs of the integrator ('in' node). The injected currents to the three integrators are applied respectively during off and on states of the input pulses for the excitatory path (PMOS transistors) and inhibitory path (NMOS transistors). Modules N_1, N_2 have two excitatory inputs (PMOS path), one self feedback inhibitory input (NMOS path) and one feedback inhibitory input (NMOS path) from the output of unit N_3, whereas module N_3 has two excitatory inputs (PMOS paths) and one inhibitory input. The last inhibitory input is represented by an adjustable constrain rate γ explained earlier.

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The dynamic characteristics of the IFMP module is verified in Matlab simulation (discussed in section II), cadence simulation and layout design on .5μ process. Fig. 9 shows successfully the balance trend in the dynamic characteristics of one IFMP out of an array of 8*8 IFMP on a (1.5 mm*1.5 mm) package. Two experiments are applied, the first one when the value of γ rate varies from 0.01 to 0.5 and values of the two inputs (L1 and L2) are equal to 0.5 and .25 respectively. The second experiment is implemented when the two inputs rates are 0.5 and 0.5 respectively for the same change in $gamma$ rate. The two experiments are successively matched in the dynamic characteristics between the theoretical results (simulated circuits) and practical results (designed low power layout on a chip).

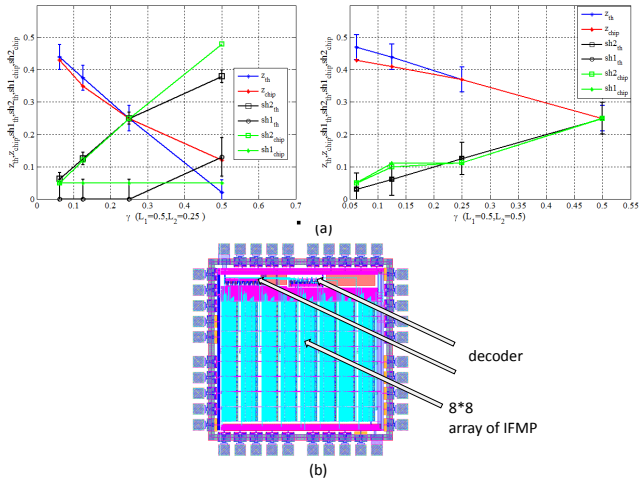

Fig. 9: (a): Dynamic characteristics for two experiments for one IFMP unit an array designed using 0.5μ process chip shown in (b)

IV. Conclusion

A scalable IFMP computational module is analysed, synthesised, proved theoretically, mapped and verified into an analog design circuit on a standard $0.5\mu m$ process. The importance of this module is to map a pulsed mode algorithm into low power silicon circuits as an attempt to implement signal processing in the neuromorphic applications. The layout of the chip is designed to include an array of 8*8 IFMP circuit in order to verify algorithmic applications. The above applications need more than one IFMP unit to map the algorithms. The above applications are already verified using IFMP module in both Matlab and cadence simulation. The applications used to verify the IFMP operation are concerned with sequence detection using Hidden Markov Model algorithm and binary classification using support vector machine. These applications are to be verified in hard ware using the designed chip as a future work.

Appendix A
Proof of one neuron convergence

The convergence of IF means that the expected value of output spikes $d[n]$ is equal to the expected value of the input spike $L[n]$ overall the samples,

$$\mathcal{E}_n\{L[n]\}_+ = \mathcal{E}_n\{d[n]\} \tag{23}$$

To proof the convergence of IF unit, the equation for step voltage change shown in Fig. can be written as,

$$V\,[n] = V\,[n-1] - \frac{t_s I}{C}(L[n] - d[n]) \tag{24}$$

where V is the membrane voltage, n is the instance time, C is the capacitance that represent the membrane, t_s is the time sampling, I is the biasing current in the NMOS and PMOS paths, $L[n]$ is the Bernoulli random input variables and $d[n]$ is the output spikes that take the values { 0,1 } according to the threshold voltage (v_{th})and the membrane voltage V. where

$$d[n] = 0.5[sgn(V_{th} - V[n]) + 1] \tag{25}$$

Then it must be proven that if the membrane voltage $V[n]$ is bounded, then the expected value of the output $d[n]$ is equal to the expected value of the input $L[n]$:

$$\text{if} \quad |V[n]| \leq c \quad \text{then} \quad \mathcal{E}_n\{L[n]\}_+ = \mathcal{E}_n\{d[n]\}$$

where c is a constant.

we write the recursive equations of the membrane potential, sum them to deduce the expectation equation of input/ output and let $\alpha = \frac{t_s I}{C}$, then:

$$V\,[n] = V\,[n-1] - \alpha(L[n] - d[n]) \tag{26}$$

$$V\,[n-1] = V\,[n-2] - \alpha(L[n-1] - d[n-1]) \tag{27}$$

$$V\,[n-2] = V\,[n-3] - \alpha(L[n-2] - d[n-2]) \tag{28}$$

Until

$$V\,[1] = V\,[0] - \alpha(L[0] - d[0]) \tag{29}$$

If we sum these equations, divide them by the number of samples N and take the $\lim_{N\to\infty}$ of both side of the equation, then we get:

$$\lim_{N\to\infty}\Big[\frac{V\,[n]}{N}\Big] = \lim_{N\to\infty}\Big[\frac{V\,[0]}{N}\Big] - \alpha\Big[\frac{1}{N}\sum_{n=1}^{N} L[n] - \frac{1}{N}\sum_{n=1}^{N} d[n]\Big] \tag{30}$$

If $|V[n]|$ is bounded (if $|V[n]| \leq constant$), then we can write equation 30 as:

$$\lim_{N\to\infty}\Big[\frac{1}{N}\sum_{n=1}^{N} L[n]\Big] = \lim_{N\to\infty}\Big[\frac{1}{N}\sum_{n=1}^{N} d[n]\Big] \tag{31}$$

Now, return to equation 26: $V\,[n] = V\,[n-1] - \alpha(L[n] - d[n])$ where the output d_n is equal to:

$$d[n] = 0.5[sgn(V_{th} - V[n-1]) + 1] \tag{32}$$

Let $V'[n] = V_{th} - V[n]$ and $V'[n-1] = V_{th} - V[n-1]$. If we substitute them in equation 26 and 32 then

$$d[n] = 0.5[sgn(V'[n-1]) + 1] \tag{33}$$

and

$$V'\,[n] = V'\,[n-1] + \alpha(L[n] - d[n]) \tag{34}$$

Now let

$$d'[n] = sgn[V'[n-1]] \tag{35}$$

Substitute equation 35 in 33

$$d[n] = 0.5[d'[n] + 1] \tag{36}$$

Substitute equation 36 in 34

$$V'\,[n] = V'\,[n-1] + \alpha(L[n] - 0.5d'[n] - 0.5) \tag{37}$$

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$$2V'[n] = 2V'[n-1] + \alpha(2L[n] - 1 - d'[n]) \quad (38)$$

Now Let
$L'[n] = 2L[n] - 1$, $V''[n] = 2V'[n]$ and

$$V''[n-1] = V'[n-1] \quad \text{then} \quad (39)$$

$$V''[n] = 2V''[n-1] + \alpha(L'[n] - d'[n]) \quad (40)$$

Now substitute 35 and 39 to find $d'[n]$ such that $d'[n] = sgn[V''[n-1]]$ too.

$$V''[n] = V''[n-1] + \alpha(L'[n] - sgn(V''[n-1]))$$

If $V''[n-1] > 0$ then
$V''[n] = V''[n-1] + \alpha(L'[n] - 1)$

$$\text{and } V''[n] \leq V''[n-1]$$

if $V''[n-1] \leq c$

$$\text{then } V''[n] \leq V''[n-1] \leq c$$

and if $V''[n-1] < 0$
then $V''[n] = V''[n-1] + \alpha(L'[n] + 1)$

$$\text{and } V''[n] \geq V''[n-1]$$

and if $V''[n-1] \geq c$
then $V''[n] \geq V''[n-1] \geq c$ Therefore $V[n]$ is bounded since $|V[n]| \leq c$.
and hence the convergence of one neuron can be written as, $\mathcal{E}_n\{L[n]\}_+ = \mathcal{E}_n\{d[n]\}$

APPENDIX B
PROOF OF IFMP CONVERGENCE

The convergence equation of IFMP for Fig 2 is listed as,

$$\sum_{i=1}^{m} [\mathcal{E}(L_i[n]) - \mathcal{E}(L_z[n])]_+ \longrightarrow \mathcal{E}(\gamma[n])$$

or

$$[\mathcal{E}_n\{T_1[n]\} + \mathcal{E}_n\{T_2[n]\}]_+ = \mathcal{E}\{\gamma[n]\} \quad (41)$$

where, $T_1[n] = \mathcal{E}(L_1[n]) - \mathcal{E}(L_z[n])$
and $T_2[n] = \mathcal{E}(L_2[n]) - \mathcal{E}(L_z[n])$

The equation for the membrane voltage for units 1,2 and 3 can be written as,

$$V_1[n] = V_1[n-1] - \alpha(L_1[n] - T_1[n] - z[n]) \quad (42)$$

$$V_2[n] = V_2[n-1] - \alpha(L_2[n] - T_2[n] - z[n]) \quad (43)$$

$$V_3[n] = V_3[n-1] - \alpha(T_1[n] + T_2[n] - \gamma[n]) \quad (44)$$

The membrane potential $V_3[n]$ in the IFMP is designed to be bounded between threshold voltage and restart voltage (initial voltage). Let T_1, T_2, and z be the output spike rate for structures $N1$, $N2$ and $N3$ respectively and γ is the inhibitory input rate for unit $N3$. Then , taking recursively the membrane equation for $N1$ and sum them starting from the first recursion below,

$$V_1[n-1] = V_1[n-2] - \alpha(L_1[n-1] - T_1[n-1] - z[n-1]) \quad (45)$$

$$V_1[n-2] = V_1[n-3] - \alpha(L_1[n-2] - T_1[n-2] - z[n-2]) \quad (46)$$

Until the initial recursion equation,

$$V_1[0] = V_1[1] - \alpha(L_1[0] - T_1[0] - z[0]) \quad (47)$$

Then divide the above sum by N, we get:

$$\frac{V_1[n]}{N} = \frac{V_1[0]}{N} - \alpha\left(\frac{1}{N}\sum_{i=1}^{N} L_1[i] - \frac{1}{N}\sum_{i=1}^{N} T_1[i] - \frac{1}{N}\sum_{i=1}^{N} z[i]\right) \quad (48)$$

since $|V_1[n]|$ is bounded, then the $\lim_{N\to\infty}$ of the above equation becomes as,

$$[\mathcal{E}\{L_1[n]\} - \mathcal{E}_n\{z[n]\}]_+ = \mathcal{E}_n\{T_1[n]\} \quad (49)$$

Similarly for $N2$,

$$[\mathcal{E}_n\{L_2[n]\} - \mathcal{E}_n\{z[n]\}]_+ = \mathcal{E}_n\{T_2[n]\} \quad (50)$$

For $N3$, the membrane potential is listed below:

$$V_3[n] = V_3[n-1] - \alpha(T_1[n] + T_2[n] - \gamma[n]) \quad (51)$$

Since V3 is bounded, then the expected value of the output for neuron 3 will be as :

$$[\mathcal{E}_n\{T_1[n]\}]_+ + \mathcal{E}_n\{T_2[n]\} = \mathcal{E}_n\{\gamma[n]\} \quad (52)$$

Now, substitute equations (49) and (50) in (52), we will get the convergence expectation equation as listed below,

$$[\mathcal{E}_n\{L_1[n]\} - \mathcal{E}_n\{z[n]\}]_+ + [\mathcal{E}_n\{L_2[n]\} - \mathcal{E}_n\{z[n]\}]_+ = \mathcal{E}_n\{\gamma[n]\} \quad (53)$$

and hence the convergence of IFMP module can be written as,
$\sum_{i=1}^{m} [\mathcal{E}(L_i[n]) - \mathcal{E}(L_z[n])]_+ \longrightarrow \mathcal{E}(\gamma[n])$

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