

An Active Clamping H-Bridge for Isolated Forward DC-DC Converters, Integrated in a High-Voltage Smart-Power IC Technology

Jan Doutreloigne, and Herbert De Pauw

Abstract—Conventional active clamping circuits for driving the pulse transformer in isolated forward DC-DC converters put considerable voltage stress on the DMOS power devices at high duty ratio. This is not so much an issue for an implementation based on discrete DMOS components, but monolithic integration becomes nearly impossible. This paper presents a new 4-transistor active clamping H-bridge topology that significantly reduces the voltage requirements and allows integration in a junction-isolated smart-power IC technology.

Index Terms—Active clamping H-bridge, DC-DC converter, integrated circuit, isolated forward converter, smart-power technology

I. INTRODUCTION

IN many applications the electronic circuitry is powered by isolated DC-DC converters for safety reasons or other system requirements. Typical examples are the power supplies in central-office ADSL and VDSL telecommunication equipment or the power supply units in Power-over-Ethernet devices. Widely used isolated converter topologies are the fly-back, the forward and the combined forward/fly-back architectures [1] [2], where the driving electronics at the primary side of the pulse transformer and the rectifying electronics at the secondary side are employing discrete power transistors and/or diodes. When trying to optimize the power efficiency and reduce the physical size of the system, monolithic integration of the driving and rectifying electronics in an appropriate high-voltage smart-power IC technology seems an attractive approach, but the practical IC design is not straightforward. This paper describes the single-chip implementation of the driving electronics at the primary side of the pulse transformer in the specific case of an isolated forward DC-DC converter.

II. FORWARD DC-DC CONVERTER

The basic architecture of an isolated forward DC-DC converter is shown in Fig.1. Switch 1, actually a power DMOS transistor, is the main driving transistor and is activated during the power transfer phase of the clock cycle.

Manuscript received July 22, 2012; revised August 5, 2012.

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During this power transfer phase, energy is transferred from the primary side of the transformer to the secondary side, and the load current is flowing through the synchronously activated transistor 3, which can be replaced by a diode at the expense of increased conduction losses. The load current is reflected to a proportional current in the primary coil, its precise value being determined by the transformer turns ratio. It's important to note that both windings of the pulse transformer are carrying current simultaneously during this power transfer phase, which is an inherent characteristic of the forward converter in contrast to the fly-back converter.

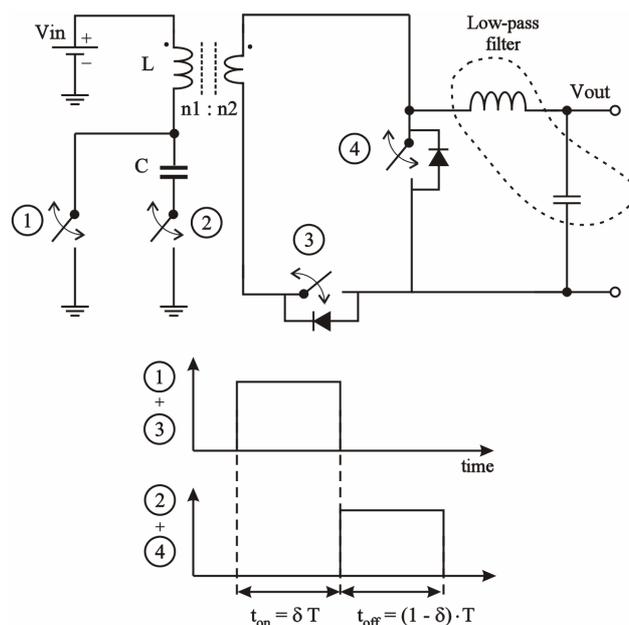


Fig.1. Basic architecture of an isolated forward DC-DC converter.

During this same power transfer phase, a magnetization current is also being built up in the primary coil. The maximum value of this current depends on different factors, mainly the primary coil inductance, the supply voltage, the clock period and the duty ratio, but it's typically much smaller than the reflected load current.

After the power transfer phase, the forward converter enters the active clamping phase where the main transistor 1 is switched off and power isn't transferred anymore from the primary to the secondary side. The load current is now flowing through the synchronously activated transistor or diode 4, acting as a free-wheeling device. The reflected load

current isn't present anymore in the primary coil of the pulse transformer, and the magnetization current of the primary coil now has to flow through the branch with the clamping capacitor C and the additional DMOS transistor 2. An appropriate voltage is automatically being built up in this clamping capacitor, creating a polarity inversion of the voltage across the primary coil, so that in steady-state circumstances the magnetization of the primary coil during the power transfer phase is perfectly compensated by the demagnetization of the coil during the active clamping phase of the same clock cycle. The exact value of the voltage on the clamping capacitor depends on the supply voltage of the circuit, and more important, also on the duty ratio of the clock signal.

Due to the presence of the LC low-pass filter, having a 3dB cut-off frequency much below the switching frequency, the converter produces an almost perfect DC output voltage equal to the supply voltage of the primary circuit, multiplied by the transformer turns ratio and the duty ratio of the clock signal.

III. BASIC 2T ACTIVE CLAMPING CIRCUIT

We will now examine the possibility of integrating the electronics at the primary side of the pulse transformer into a single IC. As explained in the previous section, the pulse transformer is driven by the basic 2-transistor (2T) active clamping circuit shown in Fig.2. The devices T1 and T2 represent the main driving n-type DMOS transistor and the active clamping p-type DMOS transistor respectively, while the 2 diodes are the built-in drain-bulk diodes of these DMOS devices. The main low-side switch T1 is activated during a fraction δ (the duty ratio or duty cycle) of a clock period T, while the active clamping switch T2 is enabled during the remainder of the clock period.

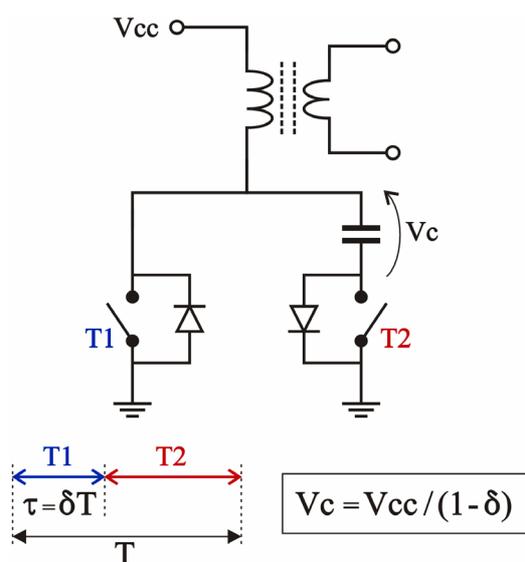


Fig.2. The basic 2T active clamping circuit for driving the pulse transformer.

The equation for the clamping capacitor voltage V_c can be deduced from the observation that in steady-state regime, the average voltage across the primary coil during 1 clock cycle must be zero. When the capacitor value is large

enough so that the capacitor voltage V_c can be assumed constant during 1 clock period, the formula for the clamping capacitor voltage V_c as a function of the supply voltage V_{cc} and the duty ratio δ becomes:

$$V_c = \frac{V_{cc}}{1 - \delta}$$

It's a very interesting exercise to put some values of the duty ratio into this equation:

$$\begin{aligned} \delta = 0.25 &\rightarrow V_c = 1.33V_{cc} \\ \delta = 0.5 &\rightarrow V_c = 2V_{cc} \\ \delta = 0.75 &\rightarrow V_c = 4V_{cc} \end{aligned}$$

Apparently, the clamping capacitor voltage increases rapidly with the duty ratio. In a practical application, the duty ratio is typically varied in the range from 0 to 50%, meaning that the internal node voltages can reach levels up to 2 times the supply voltage. E.g. in the specific case of the power supplies in central-office ADSL and VDSL telecommunication equipment where the supply voltage is nominally 48V but can go up as high as 72V according to the specifications, this means that the devices within the circuit should withstand voltages up to 144V, which already makes integration in a smart-power IC technology, i.e. a high-voltage extension of a core CMOS process, rather problematic. And that's not all! During the power transfer phase, the top electrode of switch T2 (i.e. the drain of the p-type DMOS transistor) is polarized to an electric potential of $-V_c$, or in other words, the drain potential of T2 should be able to go 144V negative with respect to the system ground for a duty ratio of 50%. For most junction-isolated smart-power technologies, this is not possible! And even if the technology allows doing so, it means that a total node voltage range of 288V must be tolerated by the IC technology! Obviously, junction-isolated smart-power technologies are no longer an option when such operating voltages are required, but very expensive dielectrically isolated SOI technologies (Silicon On Insulator) must be used instead.

IV. THE 4T ACTIVE CLAMPING CIRCUIT

This issue was thoroughly analyzed in an attempt to reduce the required voltage swing in the circuit, so that integration in a less expensive junction-isolated smart-power IC technology would become possible anyway. This study has led to an alternative driving circuit topology containing 4 solid-state switches in an H-bridge configuration, where the clamping capacitor is incorporated in one of the 2 branches of the H-bridge. An idealized version of the new 4-transistor (4T) H-bridge driving circuit is shown in Fig.3.

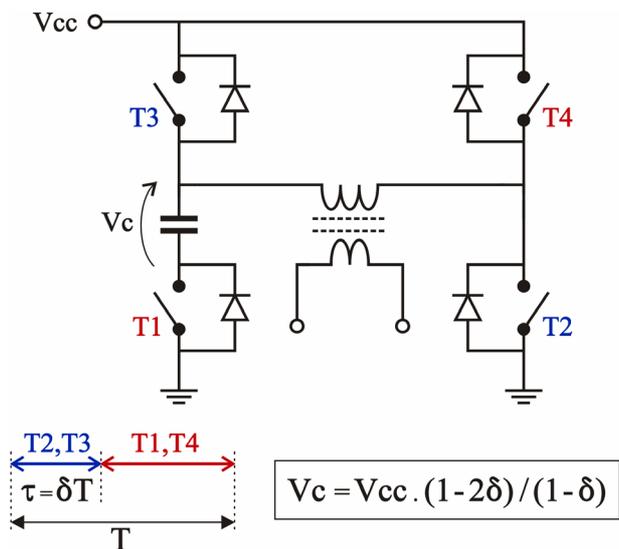


Fig.3. The new 4T active clamping circuit (H-bridge).

During the power transfer phase, the main switches T2 and T3 are activated, thereby connecting the supply voltage V_{cc} directly to the primary transformer coil. During the active clamping phase, on the other hand, the switches T1 and T4 are turned on, causing the clamping capacitor to apply an appropriate voltage with changed polarity across the primary coil and initiating the demagnetization of the coil. When analyzing the operation of this circuit in more detail, it turns out that the voltage and current waveforms in the primary coil are 100% identical to the waveforms in the conventional 2T circuit of Fig.2, and hence, there is absolutely no change in the behaviour of the whole isolated forward DC-DC converter. But there is a very important change in the voltage across the clamping capacitor, caused by the fact that the H-bridge configuration inherently produces a voltage polarity inversion in the primary coil, unlike the 2T circuit of Fig.2 where the polarity inversion entirely relies on the effect of the clamping capacitor. Therefore it's logical that the dependence of the clamping capacitor voltage on the duty ratio behaves very differently in the new 4T circuit of Fig.3 compared to the 2T circuit of Fig.2.

A calculation very similar to the one for the 2T circuit of Fig.2 leads to the following expression of the clamping capacitor voltage V_c as a function of the supply voltage V_{cc} and the duty ratio δ for the new 4T H-bridge circuit of Fig.3:

$$V_c = V_{cc} \cdot \frac{1 - 2\delta}{1 - \delta}$$

Putting some values of the duty ratio into this equation yields:

$$\begin{aligned} \delta = 0.25 &\rightarrow V_c = 0.67V_{cc} \\ \delta = 0.5 &\rightarrow V_c = 0 \\ \delta = 0.75 &\rightarrow V_c = -2V_{cc} \end{aligned}$$

These values prove that the new circuit imposes much less stringent voltage requirements on the switches than the conventional circuit. For a duty ratio in the range from 0 to 50%, the clamping capacitor voltage never exceeds the supply voltage! Moreover, in the same duty ratio range, the node potentials in the circuit never get negative with respect to the system ground. This is of course excellent news when aiming at integration in a junction-isolated smart-power technology!

Figs. 4 and 5 give a very interesting comparison between the conventional 2T and new 4T active clamping circuits in terms of voltage requirements. The graphs show the variation of the clamping capacitor voltage as a function of the duty ratio, and more important, the variation of the minimum and maximum node potentials in the circuit. Clearly, for duty ratio values between 0 and 50%, the conventional 2T circuit has to withstand electric potentials between $-2V_{cc}$ and $+2V_{cc}$, while the potentials in the new 4T circuit never exceed the supply voltage and never go negative either. For the previously mentioned central-office ADSL and VDSL application with a nominal 48V supply voltage and a maximum deviation up to 72V, integration of the 4T active clamping H-bridge circuit becomes e.g. possible in the 80V 0.35 μ m I3T80 junction-isolated smart-power technology of ON Semiconductor. The data from Figs. 4 and 5 are also repeated in Fig.6, showing the required node voltage range (i.e. the difference between the minimum and maximum node potentials occurring in the circuit) as a function of the duty ratio. As mentioned before, it can be seen that for a 50% duty ratio, a total voltage range of $4V_{cc}$ (equal to 288V for the central-office ADSL/VDSL application) is needed in the conventional 2T circuit, in contrast to only V_{cc} (equal to 72V) in the new 4T H-bridge circuit.

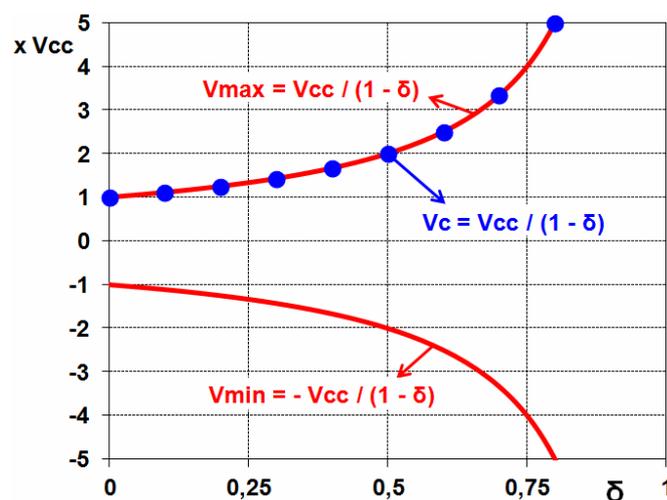


Fig.4. Variation of the minimum and maximum node potentials as a function of the duty ratio in the 2T active clamping circuit.

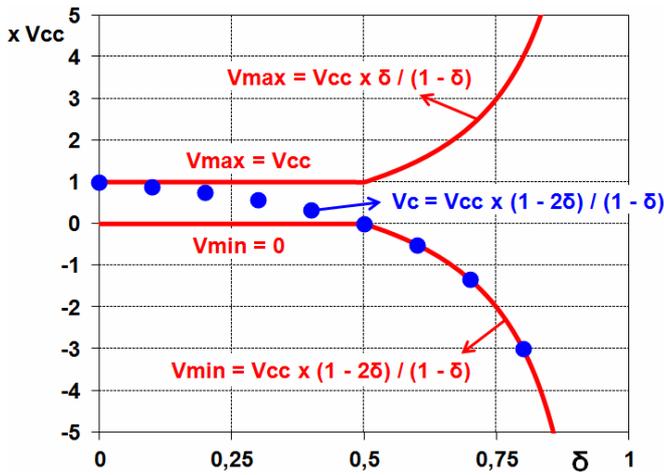


Fig.5. Variation of the minimum and maximum node potentials as a function of the duty ratio in the new 4T active clamping circuit.

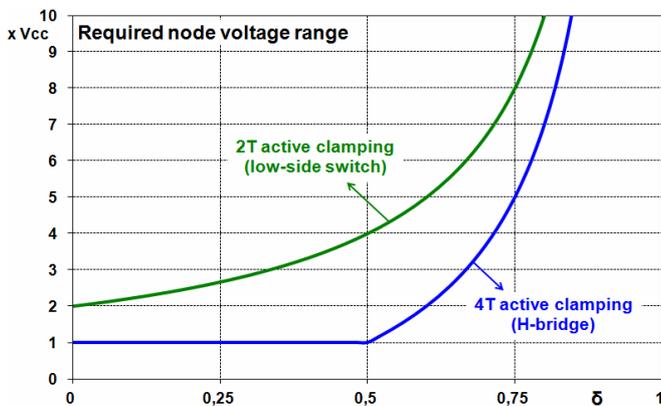


Fig.6. Comparison between the conventional 2T and new 4T active clamping circuits in terms of required node voltage range.

V. OPTIMAL 4T ACTIVE CLAMPING CIRCUIT

A practical implementation of the circuit of Fig.3 could be based on a complementary architecture, where the low-side switches T1 and T2 are n-type DMOS transistors while the high-side switches T3 and T4 are p-type DMOS devices, but this is definitely not the optimum implementation of the 4T active clamping principle as the p-type DMOS transistors occupy quite some silicon area due to their rather low hole mobility. It would be much more area-efficient to use floating n-type DMOS devices instead, offering a 2 to 3 times higher carrier mobility and hence a factor 2 to 3 reduction of silicon area. This requires, however, the possibility to drive the n-type DMOS high-side switch with a gate signal that exceeds the supply voltage of the H-bridge. Indeed, if the floating n-type DMOS high-side switch is supposed to connect the transformer terminal to the supply voltage with only a minor residual voltage drop between its source and drain contacts in order to minimize the static power losses in the switch, and taking into account that the source-gate voltage of this switch should be considerably larger than the threshold voltage in order to reach the minimum on-state resistance, then the electric

potential of its gate electrode must be a few volts above the supply voltage. This is normally achieved by using the “bootstrapping” technique that provides a temporary auxiliary voltage level exceeding the supply voltage of the system.

The principle of the bootstrapping technique is illustrated in Fig.7 for the case of a standard n-type push-pull driver. When the n-type DMOS low-side switch T1 is activated, meaning that the output voltage V_{out} is pulled down towards ground, the bootstrap capacitor C_{boot} is charged to 3.3V through the diode (neglecting the residual voltage drop between source and drain of T1 and considering the diode as ideal, i.e. with 0V forward voltage drop during conduction). When T1 is switched off and T2 has to be turned on, the 3.3V across the bootstrap capacitor acts as a temporary supply voltage for the level-shifter and buffer of the high-side switch T2. As soon as T2 is switched on, its source potential is pulled up, and the auxiliary supply voltage level V_{aux} is shifted upwards as well because the bootstrap capacitor maintains the necessary 3.3V to power the level-shifter and buffer. Note that the diode becomes reversely biased. Of course, the bootstrap capacitor will slowly be discharged by the current that is drawn by the level-shifter and, above all, the buffer, but if the capacitor value is large enough, it can keep sufficient charge until the moment T2 has to be switched off again. It is clear from Fig.7 that the gate potential of T2 can indeed be driven a few volts above the supply voltage V_{cc} .

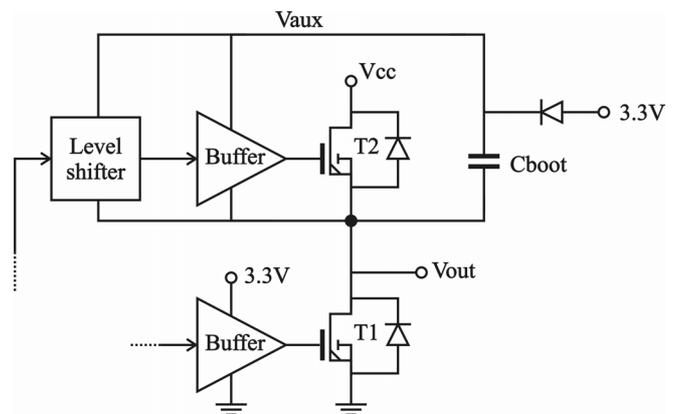


Fig.7. Bootstrapping technique for driving the n-type high-side switch in a push-pull driver.

The question now arises whether we can employ this bootstrapping technique to build a purely n-type 4T active clamping H-bridge circuit according to the schematic of Fig.3. For the right-hand branch (T2,T4), there is absolutely no problem as it is identical to the n-type push-pull driver of Fig.7. In the left-hand branch (T1,T3), however, the presence of the clamping capacitor in the lower half poses serious difficulties. When the duty ratio δ is within the range 0 to 50%, the clamping capacitor voltage V_c varies between 0 and V_{cc} . Whenever the low-side switch T1 is activated, the source potential of the high-side switch T3 is not pulled down towards ground, but it sticks at a strictly positive voltage determined by the value of clamping capacitor voltage V_c . Hence, the bootstrap capacitor (connected to the

source of the high-side switch as in Fig.7) cannot be charged to 3.3V through the diode and consequently, there is no temporary 3.3V supply voltage available for powering the level-shifter and buffer of the high-side switch. When a duty ratio in excess of 50% is used, meaning that the clamping capacitor voltage V_c becomes negative, the opposite situation is obtained. Now the source potential of the high-side switch T3 is pulled down to a strictly negative value, thereby charging the bootstrap capacitor to a voltage that can be considerably higher than 3.3V. As a result, the level-shifter and buffer circuits of the high-side switch now receive a much too high supply voltage that will cause breakdown of the low-voltage floating CMOS transistors in the level-shifter and buffer circuits! In any case, whatever the duty ratio may be, the bootstrapping circuit cannot work properly.

A solution to this problem is obtained by moving the clamping capacitor from the lower left-hand side of the H-bridge to the upper right-hand side, above the high-side switch T4, as shown in Fig.8.

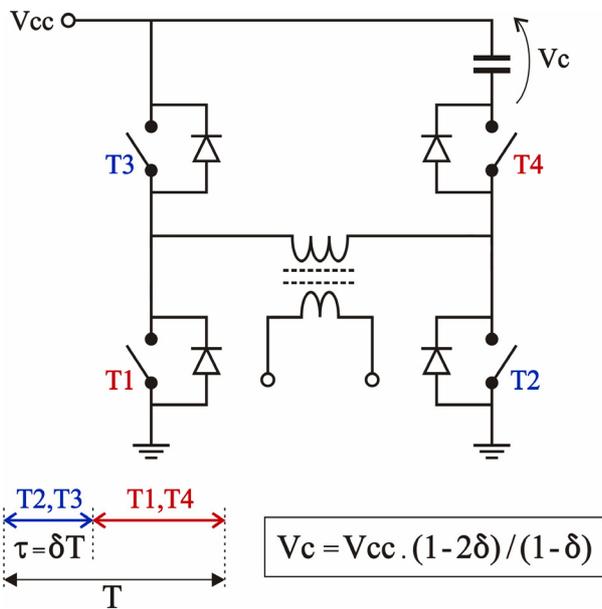


Fig.8. Optimized 4T active clamping circuit (H-bridge).

From the operational point of view, e.g. the voltage and current waveforms in the pulse transformer, the circuit of Fig.8 behaves in an identical way as the one from Fig.3, but the driving of the high-side switches becomes quite different. The H-bridge now consists of 2 normal n-type push-pull drivers, the left one being powered directly from the supply voltage V_{cc} , and the right one being powered by a duty-ratio-dependent supply voltage ($V_{cc} - V_c$). Of course, for the bootstrapping technique it doesn't matter whether the push-pull driver is powered by a fixed supply voltage or a variable one, so the same bootstrapping technique can now be applied to both branches of the H-bridge in Fig.8. This leads to the practical implementation of the area-efficient, purely n-type 4T active clamping H-bridge circuit shown in Fig.9.

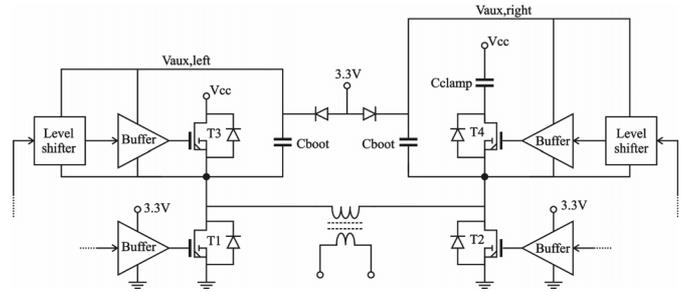


Fig.9. Optimized 4T active clamping circuit with bootstrapping technique.

There is even another important reason why the circuit of Fig.8 is preferred above the one from Fig.3. Calculations show (and it's also obvious from Fig.8 when looking at the built-in drain-bulk diodes of the DMOS switches) that the potential of the different nodes in the circuit can never go negative with respect to the system ground, in contrast to Fig.3 where the top electrode of the clamping capacitor goes negative for duty ratios in excess of 50%. Hence, for many junction-isolated smart-power technologies that do not allow negative potentials with respect to ground, the circuit of Fig.8 is definitely a better choice than the circuit of Fig.3. The curves in Fig.10 show how the minimum and maximum potentials in the circuit of Fig.8 depend on the duty ratio of the PWM signal. Regarding the maximum potential, there is no difference with the circuit of Fig.3, but the minimum potential now is 0, independently from the duty ratio, although the clamping capacitor voltage V_c goes negative above 50% duty ratio, just like in the circuit of Fig.3.

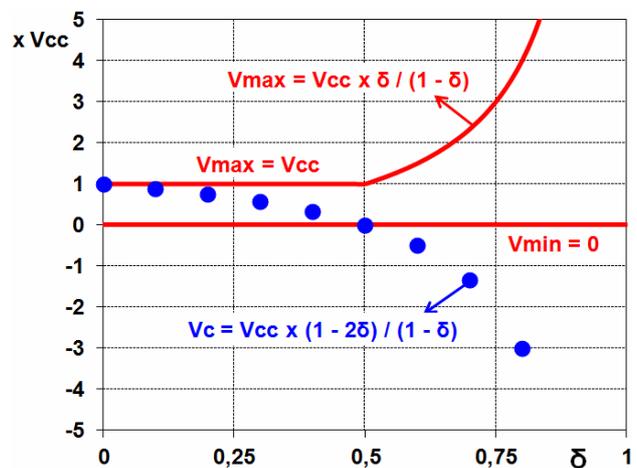


Fig.10. Variation of the minimum and maximum node potentials as a function of the duty ratio in the optimized 4T active clamping circuit.

Finally, Fig.11 compares the required node voltage range (difference between minimum and maximum node potentials in the circuit) as a function of the duty ratio for the 3 circuits that have been discussed so far. Up to 50% duty ratio, the 2 versions of the 4T active clamping H-bridge behave identically, but above 50%, the version of Fig.8 is clearly better because the required node voltage range increases less steeply than in the case of the Fig.3 version.

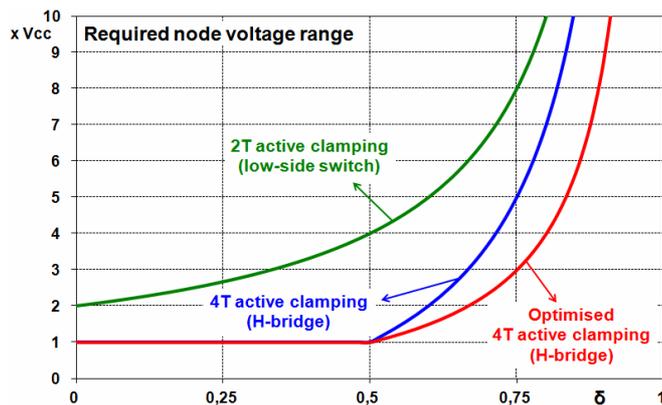


Fig.11. Comparison between the conventional 2T, the 4T and the optimized 4T active clamping circuits in terms of required node voltage range.

Two versions of the optimized 4T active clamping H-bridge circuit have been integrated in the 80V 0.35 μ m I3T80 junction-isolated smart-power technology of ON Semiconductor. Both prototypes are intended to drive the pulse transformer in the isolated forward DC-DC converter for the central-office ADSL and VDSL application. They operate from a 36V - 72V supply voltage and are designed to deliver a maximum current of 7A into the load at 12V DC output voltage. Experimental results of both prototypes will be presented at the conference.

VI. CONCLUSION

A new 4-transistor active clamping H-bridge topology for driving the pulse transformer in an isolated forward DC-DC converter was presented. The circuit exhibits significantly reduced voltage requirements and allows monolithic integration in a junction-isolated smart-power IC technology.

REFERENCES

- [1] L. Bor-Ren, "Analysis, design, and implementation of an active clamp forward converter with synchronous rectifier," *IEEE Transactions on Circuits and Systems I*, vol. 53, no. 6, pp. 1310-1319, 2006.
- [2] F. A. Himmelstoss, "Comparison of a new combined four-diode forward-flyback converter with the classical forward converter," *International Symposium on Signals, Circuits and Systems (ISSCS)*, pp. 1-4, 2009.