A 1.2 GHz Band-Pass Sigma Delta Analog to Digital Modulator with Active Inductor based Resonators

Kevin Dobson, Shahrokh Ahmadi and Mona Zaghloul

***Abstract*—This paper presents a 1.2 GHz continuous time 6th order band-pass Sigma Delta Analog to Digital modulator in IBM 0.18 um CMOS technology. Traditional RLC circuits, with spiral inductors as resonators, were replaced with active inductor based resonators with negative impedance circuits to enhance the quality factor, reduce chip area and eliminate post processing needs. Simulink and Cadence simulation yield an enhanced SNDR of 75 dB and power consumption of 29 mW. The modulator occupies 0.9 mm^2 of chip area.**

***Index Terms*— Active Inductor, Analog to Digital Converter, Negative Impedance Circuit , Sigma Delta, sixth order.**

I. Introduction

Analog to Digital Converters (ADCs) allow us to convert analog signals to digital representations suitable for processing by a digital computer. Sigma-Delta (ΣΔ) modulators utilize the processes of oversampling and noise shaping to obtain high Signal to Noise Ratios (SNR). ΣΔ modulators utilize a few critical components and produce high accuracy results [1]. These are highly desirable features. The relationship between the SNR measured at the output of a ΣΔ modulator and the effective number of bits (ENOB) is given by:

$$SNR = 6.02ENOB + 1.76 \quad (1)$$

Continuous Time (CT) ΣΔ modulators offer inherent antialiasing and are able to operate at higher frequencies than their discrete time counterparts.

In Radio Frequency (RF) receivers an incoming signal is repeatedly filtered and mixed down to lower frequencies before being digitized and processed. A CT band-pass ΣΔ modulator capable of digitizing an RF carrier signal would eliminate the need for analog filtering and mixing, and these functions would be passed on to a Digital Signal Processor (DSP). This results in a simpler, cheaper and more efficient receiver [2].

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II. Design of Continuous Time Sigma Delta Modulator

The general architecture of a CT ΣΔ modulator is shown in Fig. 1. When designing the loop filter *G(s)* for a CT ΣΔ modulator we begin with a discrete time modulator transfer function *F(z)*.

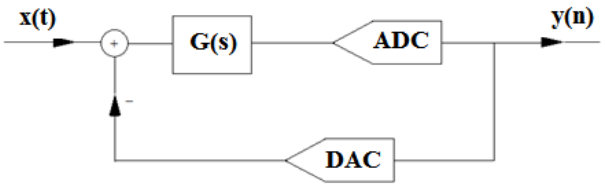

Figure 1: Continuous Time Sigma Delta Modulator

Once *F(z)* has been chosen the impulse invariant method can be used to determine the equivalent CT loop filter *G(s)* [3]. For modulators with a non-return-to-zero (NRZ) feedback we get:

$$F(z) = (1 - z^{-1}) Z_T \{ L^{-1} [\frac{G(s) e^{-ds}}{s}] \} \quad (2)$$

Here *d* represents the delay introduced by the ADC and Digital to Analog Converter (DAC). For a sixth order band-pass Sigma Delta modulator the equivalent continuous time loop filter transfer function is of the form:

$$G(s) = \frac{(s-p)(s^2 + \frac{\omega_a}{Qa} s + \omega_a{}^2)(s^2 + \frac{\omega_b}{Qb} s + \omega_b{}^2)}{(s^2 + \frac{\omega_0}{Q_0} s + \omega_0{}^2)(s^2 + \frac{\omega_1}{Q_1} s + \omega_1{}^2)(s^2 + \frac{\omega_2}{Q_2} s + \omega_2{}^2)} \quad (3)$$

ω is the normalized resonator frequency with respect to the sampling frequency in radians per second, and Q is the quality factor of the resonators. The sampling frequency is T. When *d* is equal to 1.4T and the sample rate is 4 times the frequency of the input signal then the term *p* in the numerator approximates to zero [4].

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III. Active Inductor Resonator Structure

A parallel RLC resonator is shown in Fig. 2 below.

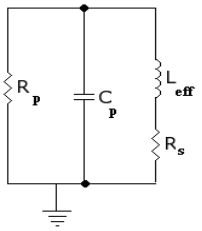

Figure 2: RLC Resonator

The transfer function of a parallel RLC circuit resonator *H(s)* is given by:

$$H(s) = \frac{As}{s^2 + \frac{\omega_0}{Q} + \omega_0^2} \tag{4}$$

Where $\omega_0 = \frac{1}{\sqrt{LC}}$ and $Q = R_P C \omega_0 = \frac{R_P}{L \omega_0}$

G(s) cannot be realized as a cascade of resonators but can be realized by the structure in Fig. 3. Here g, A_H and A_L represent amplifier gains, and *H* the resonators. The Σ block is an analog adder.

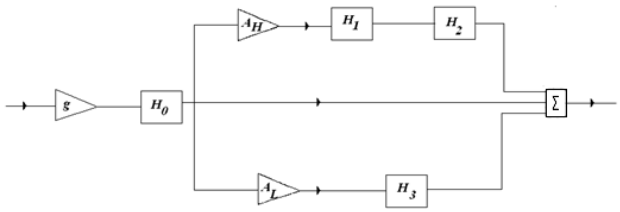

Figure 3: Sixth order Active Inductor Based Loop Filter

Traditionally resonators for band-pass CT ΣΔ modulators have been realized by RLC parallel circuits with spiral inductors. Such circuits occupy a large silicon area. Spiral inductors also have low quality factors. Active inductor based RLC circuits occupy a much smaller area, and when *Q* enhancement techniques are used, high quality factors can be achieved. The active inductor based resonator is explained by the gyrator C theorem as shown in Fig. 4 below.

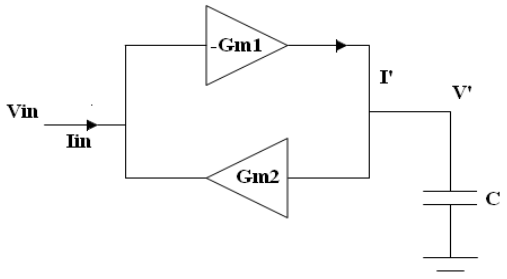

Figure 4: Gyrator Topology

$$I' = -V_{in} G_{m1} \tag{5}$$

$$-I_{in} = V' G_{m2} \tag{6}$$

$$V' = I' \frac{1}{sC} \tag{7}$$

After substitution we get:

$$\frac{V_{in}}{I_{in}} = \frac{sC}{G_{m1} G_{m2}} \tag{8}$$

In (8) we note that the *s* is in the numerator indicating that the circuit is inductive. G_{m1} and G_{m2} can be realized using CMOS devices.
The circuit in Fig. 5 realizes an active inductor with M1 and M2 acting as G_{m1} and G_{m2} respectively.

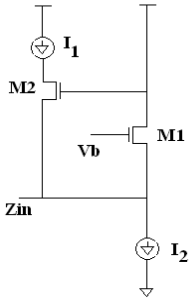

Figure 5: CMOS Active Inductor

A detailed small signal analysis results in an expression for Z_{in} as shown below [5].

$$Z_{in} = \frac{g_{oc} + g_{o1} + s(C_{gs2} + C_{gd2} + C_{ds1})}{g_{m1} g_{m2} + [g_{m2} - g_{m1} + g_{oc} + s(C_{gs2} + C_{ds1})](g_{o2} + sC_{gd2})} \tag{9}$$

Here g_o is the drain-source conductance and g_{oc} represents the loading effect of the non-ideal biasing current source. Z_{in} can be interpreted to represent the parallel RLC circuit as shown in Fig. 2.
Separating the Resistive, Capacitive and inductive parts of (9) yields the following:

$$R_p = \frac{1}{g_{m1}} \tag{10}$$

$$C_p = C_{gs1} \tag{11}$$

$$L_p = \frac{C_{gs2}}{g_{m1} g_{m1}} \tag{12}$$

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$$R_s = \frac{g_{oc} + g_{o1}}{g_{m1} g_{m2}} \tag{13}$$

The intrinsic self-resonant frequency and intrinsic quality factor of the circuit is given respectively by:

$$\omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_{gs1} C_{gs2}}} \tag{14}$$

$$Q_0 = \sqrt{\frac{g_{m2} C_{gs1}}{g_{m1} C_{gs2}}} \tag{15}$$

By utilizing two similar circuits to that in Fig. 5 and a Negative Impedance Circuit (NIC), a high Q fully differential resonator can be designed for use in a band-pass ΣΔ modulator. This resonator is shown in Fig. 6 below. Output buffers are used but not shown.

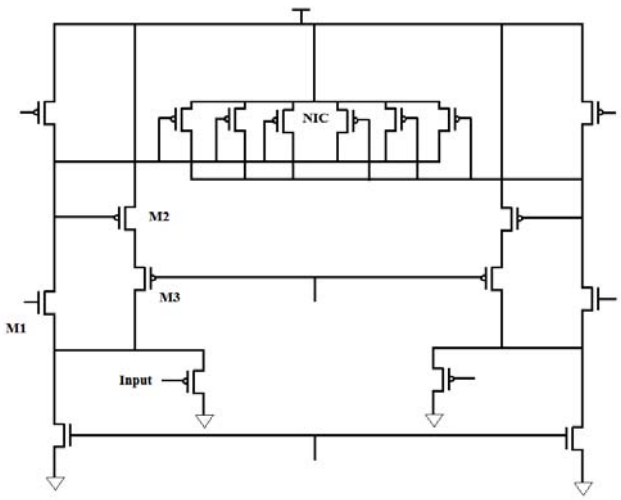

Figure 6: CMOS Active Inductor based Resonator with NIC

A PMOS device is used to couple the input to the circuit. It draws a small amount of current and does not disturb the gyrator function. Output gain can be controlled by varying the size of this MOSFET. The effect of cascoding M3 with M2 reduces the output conductance thereby reducing R_s and increasing the Q. The NIC is comprised of 3 cross-coupled differential pairs of MOSFETs with drains tied to the opposing gates. It provides a negative resistance that seeks to cancel the parallel resistance R_p, further increasing the Q. When one cross coupled pair of MOSFETs is used as a NIC, it provides a negative resistance of $-2/g_m$ and adds a $C_{gs}/2$ parasitic shunt capacitance [7]. These simple NICs however are notoriously nonlinear. In order to obtain greater linearity a multi-tanh version of the NIC circuit was used. This requires the addition of two extra cross coupled pairs of MOSFETs with a 2:1 size ratio [6][8]. When the signal is large and the symmetrical differential pair has saturated, the unbalanced differential pairs can still provide a differential current proportional to the input voltage. This scheme works effectively at high frequencies. We can rewrite Q_0 as:

$$Q_0 = \frac{1}{g_{m1}} \sqrt{\frac{C_p}{L_p}} \tag{16}$$

If we denote the enhanced quality factor of the circuit with a NIC as Q_n , then;

$$Q_n = \frac{1}{g_{m1} - g_{nic}} \sqrt{\frac{C_p + C_{nic}}{L_p}} \tag{17}$$

Here g_{nic} is the NIC transconductance and C_{nic} is the capacitance the NIC adds to the circuit [6]. As can be seen from (17) the closer the transconductance of M1 and the NIC the higher the Q. Care must be taken during design to ensure that the NIC transconductance does not exceed the transconductance of M1. The added NIC capacitance decreases the resonant frequency. This can be compensated for by increasing biasing currents.

While there is no limit to the voltage that can be applied to spiral inductors, the maximum input voltage to active inductor based circuits must not cause MOSFETs to cease operating in saturation mode. Active inductor based circuits are also noisier than circuits with real inductors by a factor of $2Q_0$ [6].

We were able to design and simulate in Cadence active inductor based resonators with a resonant frequency of 300MHz and a Q of 50 with linear operation when the input is less than 10mv p-p.

IV. Simulation

A Matlab program was used to generate initial values of the resonator multiplying coefficients g, A_H and A_L. Pole-Zero plots were then done to confirm modulator stability. Next, Simulink simulations were used to further refine the modulator design. The Simulink model was easily modified to reflect the non-idealities of an actual circuit such as limited gain due to nonlinearity and small delays introduced by each circuit component. In the ideal case with high gain in the path containing the most resonators a theoretical Signal to Noise-plus-Distortion Ratio (SNDR) of 95dB was obtained. When the limitations of nonlinearity and circuit delay were considered a goal of 75 dB for operation at 1.2 GHz was settled on. Cadence simulation followed.

A block diagram of the complete circuit simulated in Cadence is shown in Fig. 7 below.

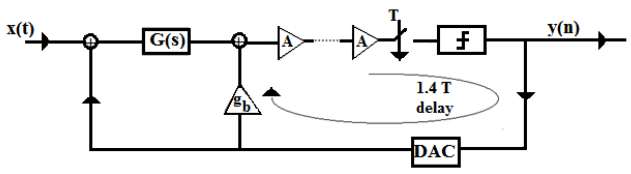

Figure 7: Active Inductor based Sixth Order Continuous Time Modulator

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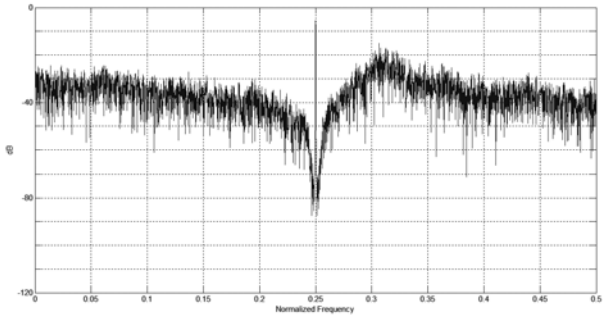

Figure 8: Simulink modulator output power spectrum density

A series of comparators [9] *A*, are used to provide the required delay of 1.4T and effective amplification of the signal prior to quantization. A large enough signal at the input of the quantizer is necessary to prevent clock feed-through [9]. Since there is a non-zero delay it is necessary to add a direct loop between the DAC and the ADC input [1]. The Adder used is described in [4].

A Differential pair is used to subtract the DAC output from the input signal, Fig. 9.

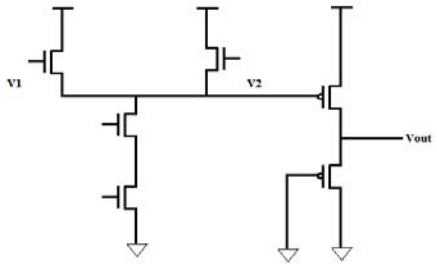

Figure 9: Subtracter differential pair with buffered output

A clocked comparator [9] coupled with a SR flip flop is used to generate the modulator output. The flip flop is necessary because a NRZ output is required.

The DAC converts the rail to rail output swing of the quantizer to a smaller voltage equal to the maximum peak to peak analog input, Fig. 10.

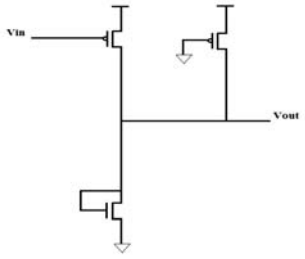

Figure 10: DAC

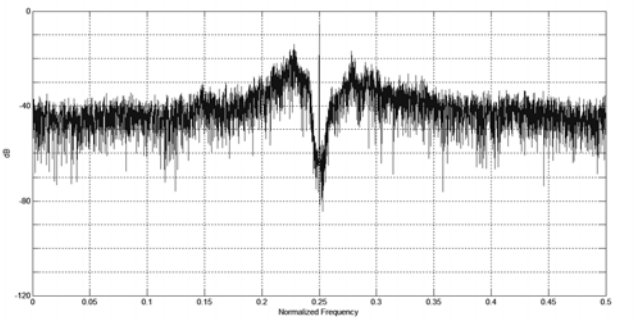

Figure 11: Cadence modulator output power spectrum density

Cadence simulation results shown in Fig. 11, are similar to Simulink simulations in Fig. 8, albeit with deteriorated noise shaping due to the circuit non-idealities previously mentioned and others such as settling time of the adder output, and offset errors. Nevertheless both yield a SNDR of 75dB. This compares favorably with other non-active inductor based sixth order band-pass ΣΔ modulators such as [10], which yields a SNDR of 68dB. Our circuit consumes 29 mW which is much smaller than the 160 mW consumed in [10]. Our design occupies only 0.9 mm^2 compared to the 2.5 mm^2 used by [10].

V. Conclusion

We have succeeded in designing and simulating the first sixth order CT ΣΔ modulator using active inductor based resonators in the loop filter. The use of *Q* enhancing techniques has resulted in a modulator with a high SNDR, and we have avoided the use of area consuming spiral inductors. When compared to the 47 dB fourth order active inductor based CT ΣΔ mentioned in [11] we are able to achieve a greater SNDR and consume roughly the same amount of power.

References

[1] P. Benabes, M. Keramat and R. Kielbasa, "Synthesis and Analysis of Sigma-Delta Modulators Employing Continuous-Time Filters," Analog Integrated Circuits and Signal Processing, no. 23, pp. 141-152, Jul. 1998.

[2] R. Schreier, G. Temes, "Understanding Delta-Sigma Data Converters" 2005.

[3] C. Lelandais-Perrault, P. Benabes, J. De Gouy, R. Kielbasa, "A parallel structure of a continuous-time filter for bandpass sigma-delta A/D Converters", 10th IEEE International Conference on Electronics, Sharjah (Emirates Arabes Unis), DEC. 2003.

[4] S. Benabid, P. Benabes, "High linear integrated LC filter for a continuous-time bandpass sigma-delta ADC" Circuits and Systems, 2003 IEEE 46th Midwest Symposium on, pp. 291 - 294 Vol. 1, 30 Dec. 2003

[5] Zhiqiang Gao, Mingyan Yu, Yizheng Ye, Jianguo Ma, "A CMOS bandpass filter with wide-tuning range for wireless applications", Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on.

[6] Yue Wu, Xiaohui Ding, Mohammed Ismail, and Håkan Olsson, "RF bandpass filter design based on CMOS active inductors", IEEE Transactions on circuits and systems—II: Analog and Digital Signal Processing, vol 50, no.12, Dec. 2003.

[7] Byunghoo Jung, Harjani, R., "A wide tuning range VCO using capacitive source degeneration" Circuits and Systems, 2004. ISCAS apos;04. Proceedings of the 2004 International Symposium on Volume 4, Issue , 23-26 May 2004 Page(s): IV - 145-8 Vol.4.

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[8] A. P. Ryan, O. McCarthy, "A novel pole-zero compensationscheme using unbalanced differential pairs", IEEE transactions on circuits and systems—I: Regular papers, vol. 51, no. 2, Feb. 2004.

[9] R. Jacob Baker, "CMOS, Circuit Design, Layout, and Simulation", IEEE Press Series on Microelectronic Systems.

[10] Cho-Ying Lu, Silva-Rivas, J.F.; Kode, P.; Silva-Martinez, J., Hoyos, S., "A Sixth-Order 200 MHz IF Bandpass Sigma-Delta Modulator With Over 68 dB SNDR in 10 MHz Bandwidth", Solid-State Circuits, IEEE Journal of, Volume: 45, Issue: 6, 2010 , Page(s): 1122 – 1136

[11] Quining Chen, Kamal El-Sankary and Ezz El-Masry, "A UHF continuous-time current-mode band-pass delta sigma modulator based on active inductor" Circuits and Systems, 2008. MWSCAS 2008. 51st Midwest Symposium on

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