An Efficient Multilevel-Synthesis Approach and its Application to a 27-Level Inverter

P. Satish Kumar, *Member IAENG*, G. Sridhar, and Ch. Lokeshwar Reddy

***Abstract*—In this paper, an efficient multilevel wave form synthesis technique is proposed and applied to a 27-level inverter. The basic principle of the proposed scheme is that the continuous output voltage levels can be synthesized by the addition or subtraction of the instantaneous voltages generated from different voltage levels. This synthesis technique can be realized by an array of switching devices composing full-bridge inverter modules and proper mixing of each transformer terminal voltage. The most different aspect, compared to the conventional approach, in the synthesis of the multilevel output waveform is the utilization of a combination of transformers rather than the accumulation of capacitor voltage sources. A 27-level inverter consists of three full-bridge modules and their corresponding transformers. Quasi-sinusoidal voltage waves can be generated from a suitable selection of the turn's ratio of the transformer. The validity of the proposed scheme is verified by the simulation.**

***Keywords*—Multilevel inverter, synthesis, cascaded connection, Total Harmonic Distortion.**

I. INTRODUCTION

THE Multilevel inverters have emerged as a new kind of power-conversion systems. General multilevel inverters have an arrangement of power switching devices and capacitor voltage sources. By the control of the switching devices, they can synthesize stepped output voltages with low harmonic distortions. The principal motivation for multilevel topologies is the increase of power, the reduction of voltage stress on the power switching devices, and the generation of high-quality output voltages and sinusoidal currents.

The multilevel inverter synthesizes a 27-level output voltage with considerably

i. Reduced harmonic components.
ii. Compared to the Conventional approaches, considering the same output-voltage level of a 27-level inverter; it can save on the number of the main switches and diodes up to 77% without considering the power rating of the devices.
iii. In addition, the gate amps and their independent voltage sources are proportionally reduced to the number of the used switches.
IV.

In the viewpoint of the latter, three presentable topologies can be considered for multilevel inverters: diode clamped (or neutral clamped), flying capacitors (or capacitor clamped), and cascaded H-bridge cells with separate dc sources. Theoretically, they can synthesize an infinite output-voltage level. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a large number of levels increase the number of switching devices, gate amp, Diodes and other passive elements. Moreover, it causes control complexity and introduces voltage-imbalance problems. Consequently, these multilevel-inverter schemes are not suitable for increasing the output-voltage levels because of their large number of switching devices. To increase the number of the output voltage levels in order to obtain high-quality output voltage waveforms by means of multilevel-inverter schemes, the above problems should be solved in advance.

In this paper, an efficient multilevel-waveform synthesis technique is suggested and a new multilevel-inverter topology and its control scheme are presented. It consists of three full-bridge inverter modules and their corresponding three transformers, which have a series connected secondary winding.

II. BASIC PRINCIPLE OF THE PROPOSED MULTILEVEL SYNTHESIS

Conventional multilevel inverters include an array of switching devices and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the switching devices withstand only reduced voltages. Fig. 1(a) shows a basic concept of the general multilevel-waveform synthesis method with different numbers of levels, for which an ideal switch with several positions represents the action of the switching devices. A two-level inverter generates an output voltage with two values with respect to the negative terminal of the capacitor, while the three-level inverter generates three voltages.

Fig. 1(b) shows a basic principle of the proposed multilevel-waveform synthesis method. Considering the array of individual voltage Sources having different values, the continuous-output-voltage levels can be synthesized by the

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P. Satish Kumar is working as Assistant Professor with the Department of Electrical Engineering, University College of Engineering, Osmania University, Hyderabad, Andhra Pradesh, INDIA, 500 007.
(e-mail: satish_8020@yahoo.co.in).

G. Sridhar is with the Department of Electrical and Electronics Engineering, Jyothishmathi Institute of Technology & Science, Karimnagar, Andhra Pradesh, INDIA.

Ch. Lokeshwar Reddy is with the Department of Electrical and Electronics Engineering, CVR College of Engineering, Hyderabad, Andhra Pradesh, INDIA.

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selection of suitable switching combinations. In the proposed multilevel scheme, this can be realized by an array of switching devices composing full bridge inverter modules and proper mixing of each transformer terminal voltage. The most different aspect, compared to the conventional approach, in the synthesis of the multilevel output waveform is the utilization of a combination of transformers rather than the accumulation of capacitor voltage sources.

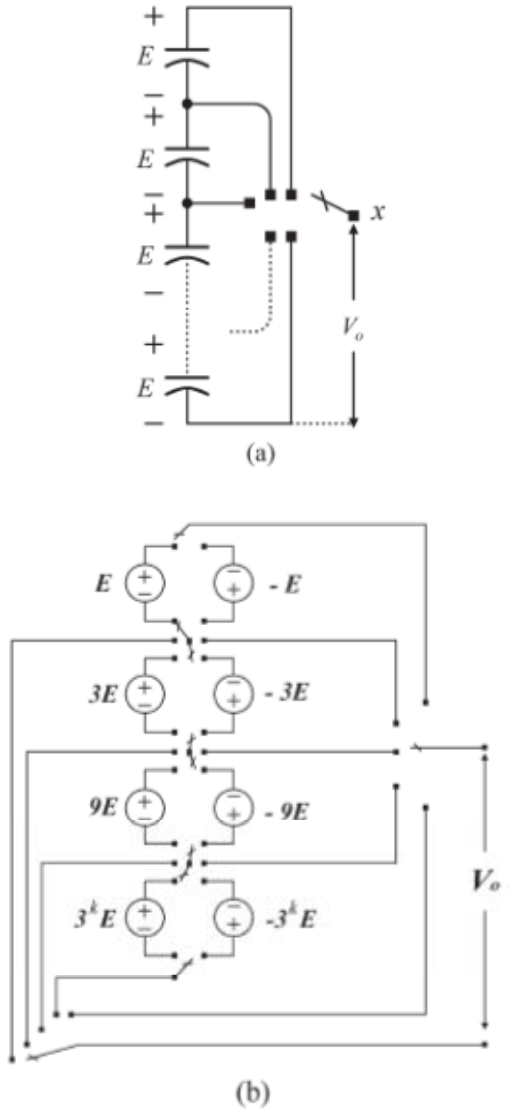

Fig. 1. Basic concept of the general and proposed multilevel waveform synthesis a) General approach; b) proposed method

III. PROPOSED MULTILEVEL INVERTER

Fig. 2(a) shows a single-phase full-bridge inverter connected with a transformer. The output voltage V_o appears as $+aV_{dc}$, 0, and $-aV_{dc}$ according to the ON–OFF conditions of switching devices, where a is the secondary turns ratio of the transformer. Therefore, the output voltage can be determined by the dc input voltage and the turns ratio of the transformer. Because a general Inverter system has a constant dc input source, it is desirable that the turns ratio of the transformer determines the amplitude of output voltage. Fig. 2(b) shows a cascaded connection of the secondary turn's ratio of the transformers to obtain a large number of output-voltage levels. In the level selection of the output voltage, it should be noted that the focuses are both the result of the output-voltage combination of the inverter and the determination of the turn's ratio of the transformer, which can synthesize a continuous-output-voltage level with an integral ratio. Because each full-bridge inverter module can generate three levels, the required turn's ratio of the secondary winding, which can generate a continuous-output-voltage level with an Integral ratio, can be selected as

$$a_k = a.3^{k-1}, k = 1,2,3..... \quad (1)$$

Here, k means the rank of the stacked transformers in series, and a is determined by the turns ratio of the transformer.

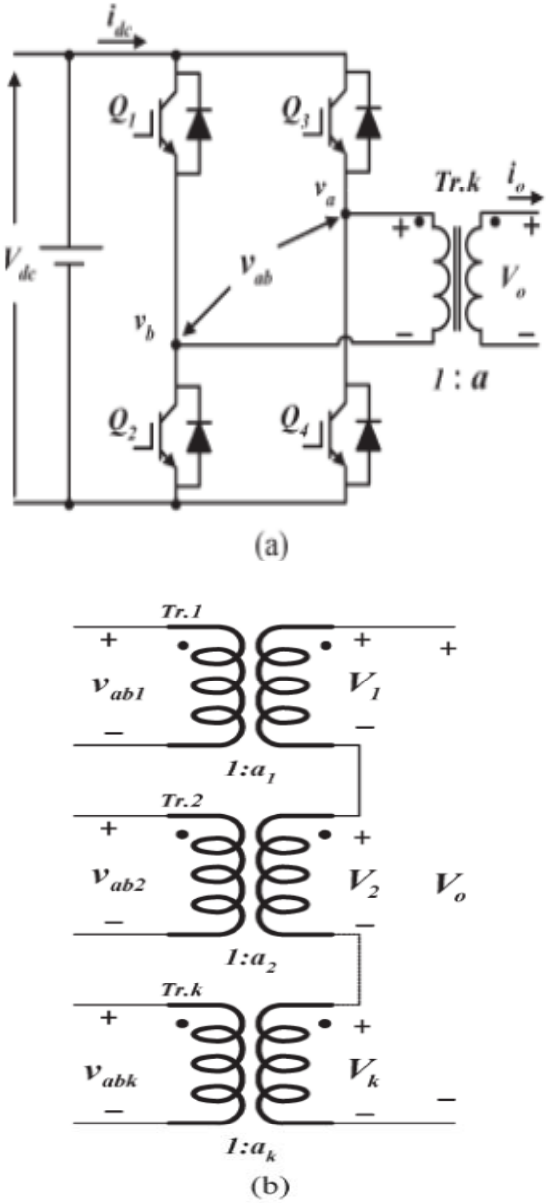

Fig. 2. Basic concept of the proposed multilevel waveform synthesis; (a)Single phase full bridge inverter module; (b) Cascaded connection of the secondary winding of the transformer

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TABLE I
EACH TURNS RATIO OF THE SECONDARY WINDING OF THE TRANSFORMER IN THE SERIES CONNECTION

Transformer	Rank	Turn-ratio
1	α_1	a
2	α_2	3a
3	α_3	9a
4	α_4	27a
5	α_5	81a
K	α_k	3^{k-1}

When the input voltage is V_{ab}, therefore, its value determines the difference between output levels. Table I illustrates the secondary turns ratio of the transformer. The possible number of output-voltage levels when it employs *n* number of transformers is written as

$$V_n = 3^n, n = 1,2,3..... \quad (2)$$

Where *n* is the number of cascaded transformers. The switching functions of single-phase full-bridge inverter shown in Fig. 2(a) are summarized as

$$S_{FB} = 1: Q2, Q3 = \text{ON}$$
$$S_{FB} = 0: Q1, Q3 \text{ (or } Q2, Q4) = \text{ON}$$
$$S_{FB} = -1: Q1, Q4 = \text{ON} \quad \ldots. \ (3)$$

With the switching functions as defined in eq. (3), the overall output voltage (V_o) of the proposed inverter is expressed as

$$V_0 = \sum_{n=1}^{\infty} S_{FB_n} . a_n . V_{dc} \quad \ldots(4)$$

From the result of eq.(4), it can be found that three transformers having a series-connected secondary winding can synthesize a 27-level output voltage and an 81-level output voltage with four transformers. If the number of transformer is boundless, the output-voltage levels are infinite, which is similar to the analog one. However, a large number of transformers can be a cause of cost increase and manufacturing problems. Therefore, It should be selected considering the amplitude of input voltage, the THD of output voltage, and the system price. The equivalent circuit of the proposed multilevel inverter employing three transformers with a series-connected secondary winding is shown in Fig. 3. In this figure, the output voltage by the switching function can be rewritten as

$$Vo = \sum S_{FB_n} . a_n . V_{dc} = (9S_{FB3} + 3S_{FB2} + S_{FB1}) . a . V_{dc}. \quad \ldots.(5)$$

$$where \therefore a_1 = a, a_2 = 3a, a_3 = 9a, and, S_{FBn} \in \{1,0,-1\}$$

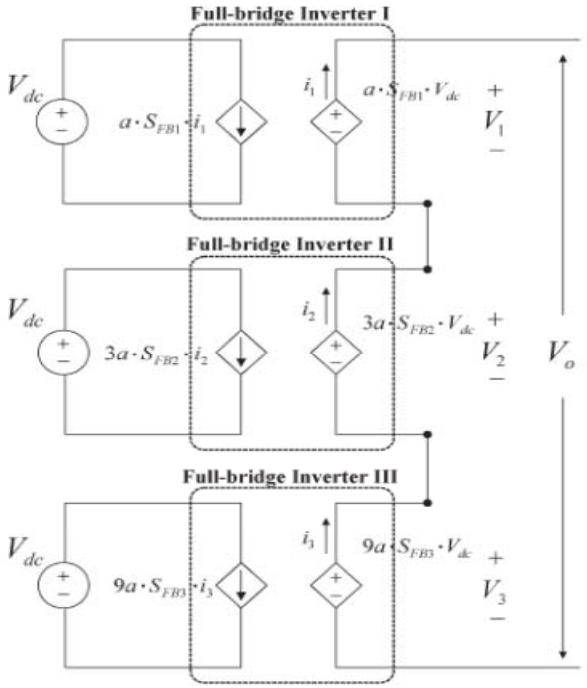

Fig. 3. Equivalent circuit of the proposed multilevel inverter employing cascaded three transformers with a series connected secondary winding

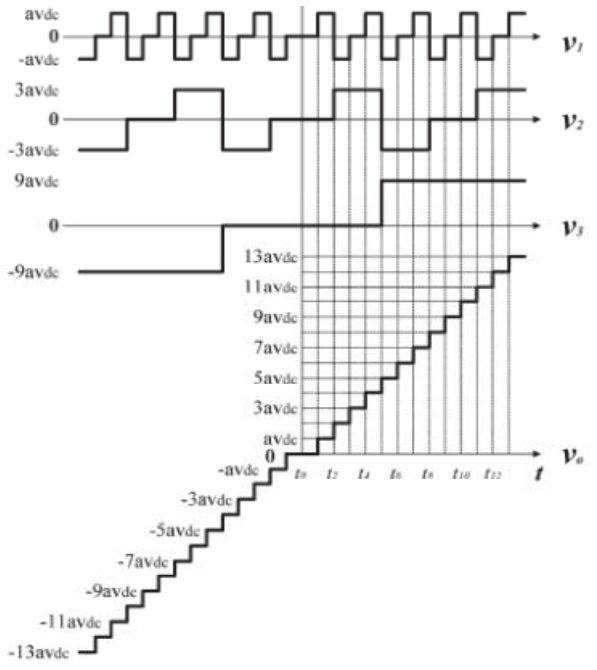

Fig. 4. Expected output voltage levels and each terminal voltage of the transformer

Fig. 4 shows the expected output-voltage levels and each terminal voltage of the transformer. It is very useful to understand the multilevel synthesizing procedure. Table II lists the switching functions according to each output-voltage level in the case of positive output voltage. For a negative case, they can be easily obtained by multiplying -1 to Table II.

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In the case of SFB3, which is the switching function of the lowest inverter module, it takes a naught when a desired output level is equivalent or lower than a fourth level in Table II. In contrast, it takes a unity when a wanted output-voltage level is higher than the fourth level. The switching function SFB3 can be expressed by using eq. (6). For the sake of convenience, we just deal with the positive portion given in Table II. Here, all variables are considered as an integer.

$$\text{If } (m \le 4) \text{ then } S_{FB3} = 0$$
$$\text{If } (m > 4) \text{ then } S_{FB3} = 1 \quad \ldots\ldots (6)$$

Here, m means the number of output-voltage levels. The switching function SFB2 of the middle inverter is determined as

$$if\left[\frac{(m+1)}{3\%3}=0\right], then....S_{FB2}=0$$
$$if\left[\frac{(m+1)}{3\%3}=1\right], then....S_{FB2}=1$$
$$if\left[\frac{(m+1)}{3\%3}=2\right], then....S_{FB2}=-1 \quad .....(7)$$

Where % is a modulus operator. The switching function SFB1 of the upper inverter is determined by

$$\text{if } (m\%3) = 0 \quad \text{then} \quad S_{FB1} = 0$$
$$\text{if } (m\%3) = 1 \quad \text{then} \quad S_{FB1} = 1$$
$$\text{if } (m\%3) = 2 \quad \text{then} \quad S_{FB1} = -1 \quad .....(8)$$

TABLE II
SWITCHING FUNCTIONS ACCORDING TO OUTPUT VOLTAGE LEVEL

Output level (m)	S_{FB3}	S_{FB2}	S_{FB1}
0	0	0	0
1	0	0	1
2	0	1	-1
3	0	1	0
4	0	1	1
5	1	-1	-1
6	1	-1	0
7	1	-1	1
8	1	0	-1
9	1	0	0
10	1	0	1
11	1	1	-1
12	1		0
13	1	1	1

Fig. 5(a) shows the command voltage of the inverter and its output-voltage waveform. Because it has a symmetric configuration, the selection of the output level and its corresponding duration, which define the switching functions, can be performed by a quarter portion of one period. As the possible maximum number of output levels for the positive portion is 13, except for zero, the amplitude of the quarter sine wave is divided into 13, with the same height. Then, t_1–t_{13} are determined. Fig. 5(b) shows the method to determine the duration of a corresponding output-voltage level. The output-voltage level is determined by an average value between points A and B, which are selected by comparison with the reference voltage.

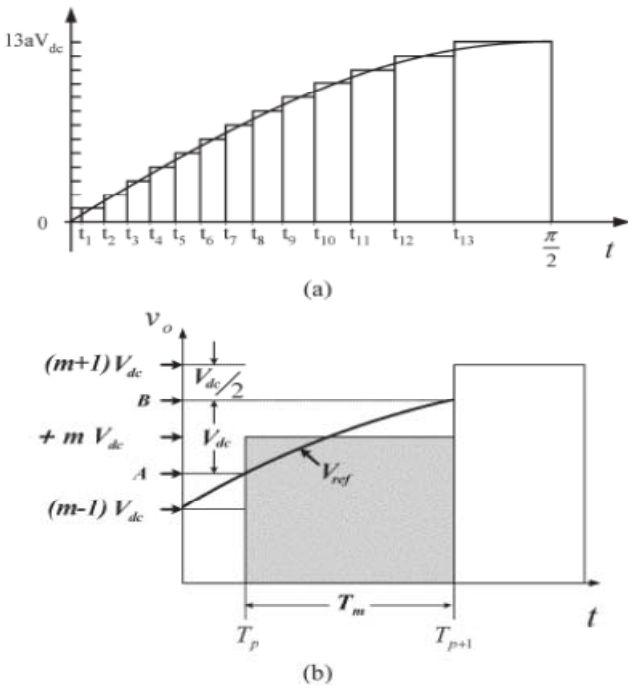

Fig. 5. Reference and output voltage of the proposed multilevel inverter a) Reference and output voltages for ¼ cycles; b)Determination of corresponding duration

The output-voltage level is selected between one level lower and the upper one compared to a desired output level. The maintaining time (T_m) of the output voltage $+mV_{dc}$ is given by this figure as $T_{p+1} - T_p$. In order to determine those durations, the output voltage is normalized by $13aV_{dc}$; then, each level's duration is given as

$$T_m = \sin^{-1}\left[\frac{(\frac{m-1}{13}+\frac{1}{26})13aV_{dc}}{V_p}\right], m = 1,2,3,..... \quad ....(9)$$

Where V_p is the peak value of the normalized command sine voltage, and m means the number of the output-voltage level. In eq. (9), m is calculated up to the number that arcsine is not exceeding unity. It is proportional to the amplitude of the output command voltage, and it has a maximum value of 13. A control block diagram of the proposed multilevel inverter is shown in Fig. 6. It basically depends on the traditional proportional and integration (PI) control. The reference voltage V_{ref} is generated by the feedback of the output voltage via the PI controller. It is used to determine and calculate the output voltage level and its corresponding duration.

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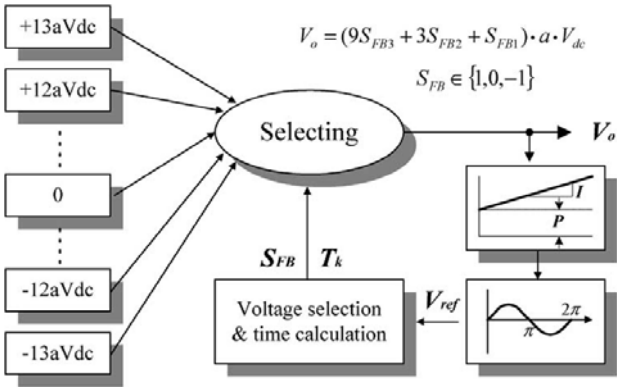

Fig. 6. Control block diagram of the proposed multilevel inverter

IV. SIMULATION RESULTS AND ANALYSIS

The validity of the proposed synthesis approach is verified by the simulation using MATLAB/simulation. The output-voltage waveform has a 27-level output voltage waveform by the combination of the series-connected transformers 1: *a*, 1: 3*a*, and 1: 9*a* in sequence. The simulation diagram of 27-level multilevel inverter is shown in Fig. 7. The gate signals applied to the switches of proposed inverter are shown in Fig. 8. As shown in Fig. 9 the output-voltage waveform with R-load is very similar to a sinusoidal one, owing to a large number of output-voltage levels. In addition, the output voltage will turn into a more sinusoidal wave if the output load current increases, since the inductance components of cascaded transformers are operated as a high-performance filter; it will be proved from Fig. 9 and Fig. 10. The Fig. 11 and Fig. 12 shows the fast Fourier transform (FFT) results of the output voltage with a R-load and an inductive load respectively. From these results, it is clear that the proposed multilevel inverter in higher load conditions can generate a more sinusoidal output voltage than those cases of a lower or a no-load condition.

The most outstanding advantage of the proposed multilevel-inverter schemes is the reduced main switching devices and diodes. Forty switching devices can be saved without considering the current rating of the used switching devices. In addition; the gate amp is proportional to the number of the switching devices. The proposed multilevel approach is suitable for constant voltage and constant frequency (CVCF) applications such as uninterruptible power supply (UPS) and photovoltaic inverter systems because of the property of the transformer used. However, this method is not desirable for the motor drives employing variable-frequency (VF) control method because of the transformer saturation.

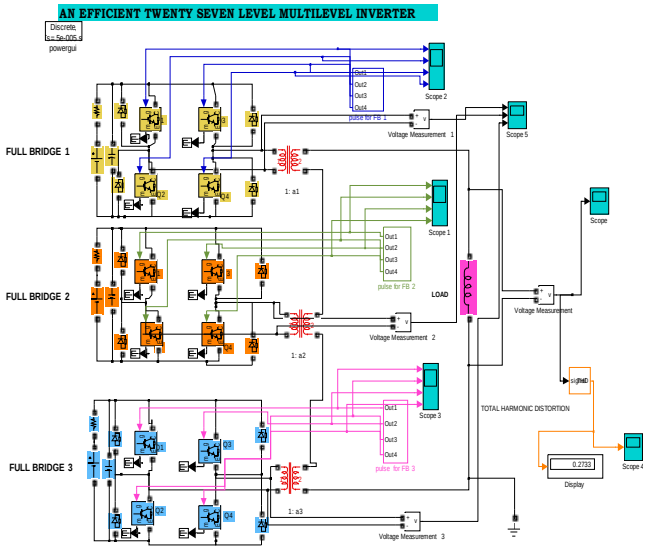

Fig. 7. Simulation diagram for an Efficient 27- Level Multilevel Inverter with L-Load

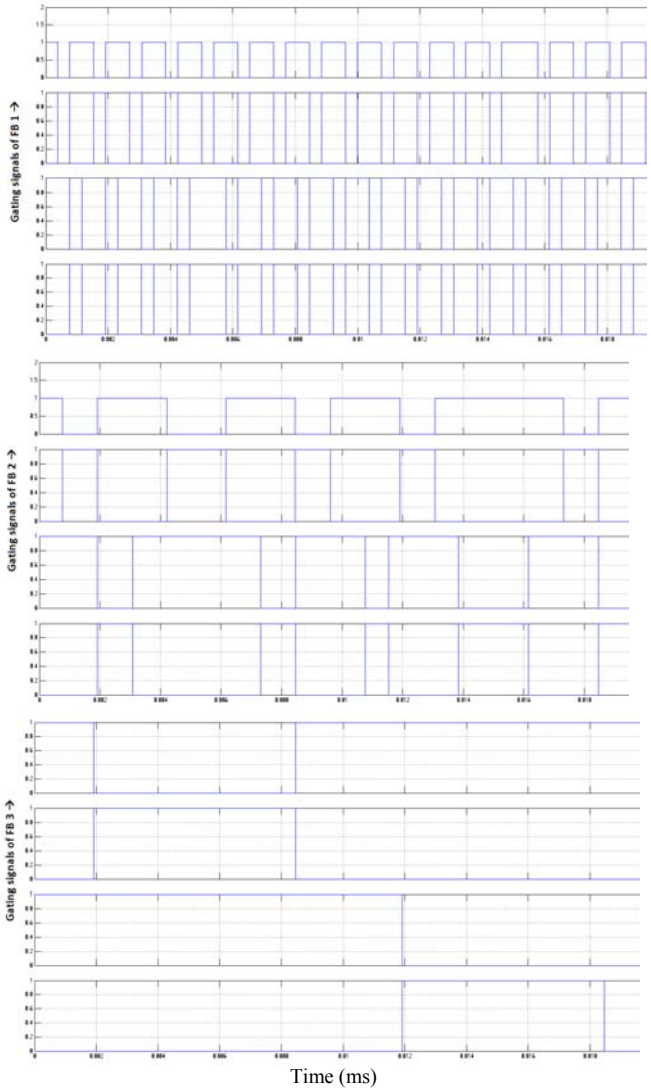

Fig. 8. Gate signals applied to IGBTs

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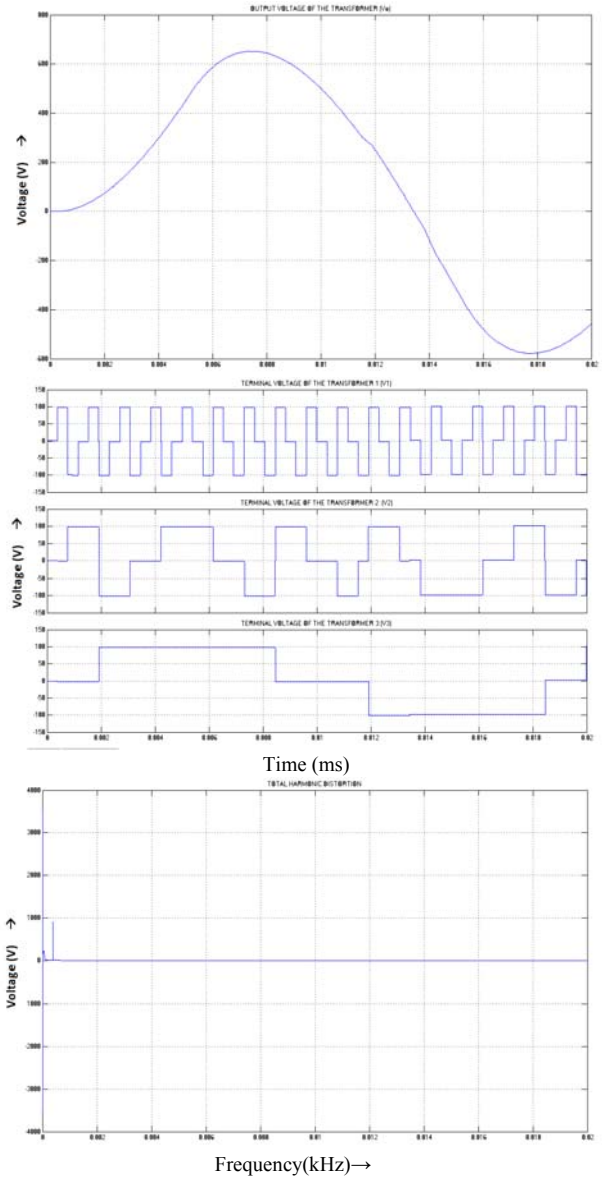

Fig. 9. Waveforms of the proposed 27-level inverter with R-load

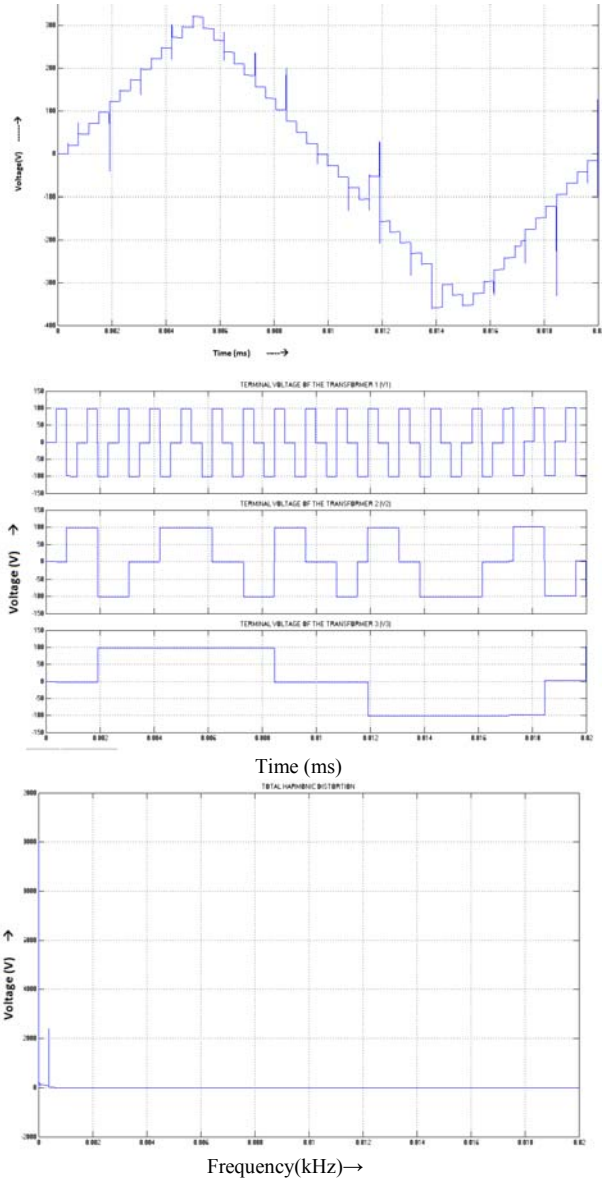

Fig. 10. Waveforms of the 27-level inverter with inductive load

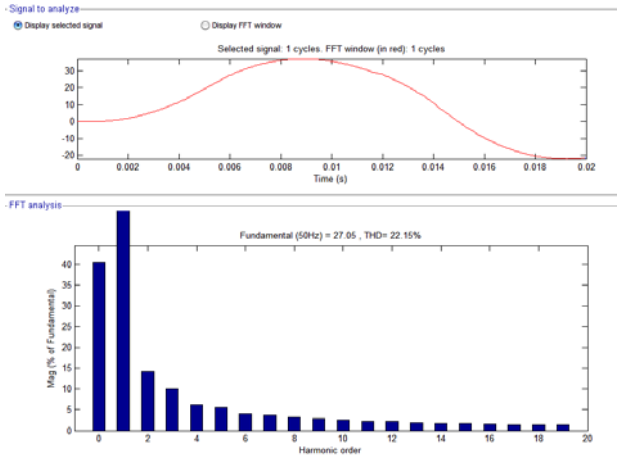

Fig. 11. FFT Analysis for Resistive load

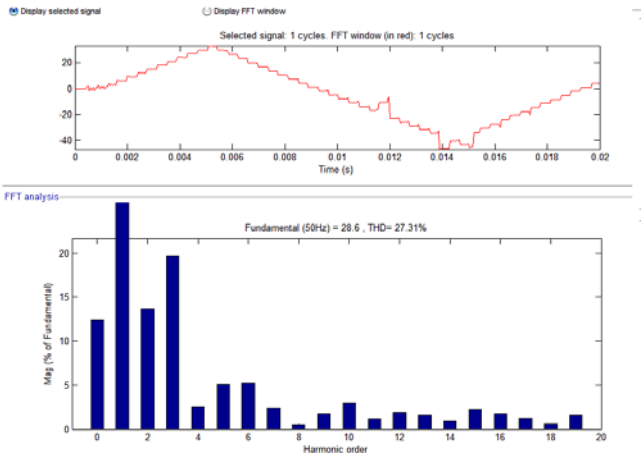

Fig. 12. FFT Analysis for Inductive load

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V. Conclusions

The basic principle of the suggested multilevel-inverter scheme is that the continuous-output-voltage levels can be synthesized by the addition or subtraction of the instantaneous voltages generated from different voltage levels. In the proposed multilevel inverter, this can be realized by an array of switching devices composing full-bridge inverter modules and proper mixing of each transformer terminal voltage. The most different aspect, compared to the conventional multilevel approaches, in the synthesizing of the multilevel output levels is the utilization of a voltage combination of transformers rather than the accumulation of capacitor voltage sources. In addition, the gate amps and their independent voltage sources are proportionally reduced to the number of the used switches. The Validity of the proposed multilevel-synthesis scheme is verified through simulation results for a 27-level inverter.

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P. Satish Kumar was born in Karimnagar, Andhra Pradesh, INDIA in 1974. He obtained the B.Tech. degree in Electrical and Electronics Engineering from JNTU College of Engineering, Kakinada, INDIA in 1996. He obtained M.Tech degree in Power Electronics in 2003 and Ph.D. in 2011 from JNTUH, Hyderabad. He has more than 17 years of teaching experience and at present he is an Assistant Professor in the Department of Electrical Engineering, University College of Engineering, Osmania University, Hyderabad, INDIA. His research interests include Power Electronics, Special Machines, Drives and Multilevel inverters and guiding seven research scholars. He presented many research papers in various national and international conferences and published many papers in various international journals. He is the Editorial Board member of many international journals. At present he is actively engaging in two Research Projects in the area of multilevel inverters funded by University Grants Commission (UGC), New Delhi, and Science and Engineering Research Board (SERB), New Delhi. India.

G. Sridhar obtained the B.Tech. degree in electrical engineering from University of Madras, INDIA in 2000 and M.Tech. degree in power systems with emphasis on high voltage engineering in 2005 from JNTU College of engineering, Kakinada. He is pursing Ph.D. degree in the area of multilevel inverters. He has 13years teaching experience. He is working as Associate Professor in the Department of Electrical and Electronics Engineering, Jyothishmathi Institute of Science and Technology, Karimnagar. His research interests include Power Electronics and Multilevel inverters.

Ch. Lokeshwar Reddy was born in Khammam, Andhra Pradesh, INDIA in 1977. He obtained the B.Tech. degree in electrical engineering from KITS Warangal, A.P., INDIA in 1999 and M.Tech. degree in High Voltage Engineering in 2001 JNTU College of engineering, Kakinada. He is pursing Ph.D. degree in the area of multilevel inverters. He has 12 years teaching experience. He is working as Associate Professor in the Department of Electrical and Electronics Engineering, CVR College of Engineering, Hyderabad. He presented many research papers in various national and international conferences and journals. His research interests include Power Electronics Drives and Multilevel inverters.

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