A Novel Topology for Multilevel Inverter with Reduced Number of Switches

Hulusi Karaca

Abstract— **Multilevel inverter is energy conversion device that is generally used in medium-voltage and high-power applications. It offers lower total harmonic distortion, switching losses and voltage stress on switches than conventional inverter. In this paper, a novel multilevel inverter topology with the decreased number of power switches is proposed, and its modulation technique is introduced. This multilevel inverter structure consists of the level module units to enhance the level of the output voltage. Since a level module unit consists of only a DC voltage source and a bidirectional switch, this structure allows a reduction of the system cost and size. Effectiveness of the proposed topology has been demonstrated by analysis and simulation.**

Index Terms— **Multilevel inverter, multilevel converter, power converter, H-bridge.**

I. Introduction

IN RECENT YEARS, a great number of industrial applications have begun to request higher power instruments [1]. However, semiconductor power switches which endure the medium voltage have not been produced still. A source in medium voltage level is inconvenient to directly connect only one switching device. Consequently, the multilevel inverter topology has emerged as a different option for working with medium voltage and high power. A multilevel inverter not only produces high power ratings, but also facilitates the use of renewable energy sources [2].

A multilevel inverter is power conversion device that produces an output voltage in the needed levels by using DC voltage sources applied to input [3]. Multilevel inverter which performs power conversion by using the discrete DC voltage sources was firstly introduced in 1975 [4]. This multilevel inverter structure consists of the H-bridges connected in series. Then, the diode-clamped multilevel inverter was emerged [5], [6]. It employs the capacitors connected in series to separate the DC bus voltage in different levels. In 1992, the capacitor clamped multilevel inverter was introduced [7]. This structure is similar to the structure of the diode-clamped multilevel inverter, but it uses the capacitors instead of the diodes to clamp the voltage levels.

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Some advantages can be obtained using multilevel inverter as follows: the output voltages and input currents with low THD, the reduced switching losses due to lower switching frequency, good electromagnetic compatibility owing to lower dv/dt, high voltage capability due to lower voltage stress on switches. These attractive features have encouraged researchers to undertake studies on multilevel inverter.

However, multilevel inverters have required more power components. Their driver isolations become more complicated because each extra level requires the additional isolated power source. So, the cost of the driver circuit will be increased according to the traditional single-cell inverters [8]. Recently, some multilevel inverter structures with decreased number of switches have been developed to overcome this disadvantage [3], [9], [10].

In this paper, a novel multilevel inverter topology with reduced number of switches which uses the separate DC sources has been proposed. The control technique has been discussed to control this topology. The proposed topology consists of level module units to increase the output voltage level. The feasibility of the proposed topology has been proved by analysis and simulation.

II. Proposed Multilevel Inverter Topology

The proposed multilevel inverter topology consists of the level module units. A level module unit is constructed by a DC voltage source and a bidirectional switch capable of conducting current and blocking voltage in both directions as shown in Fig. 1. Such devices are currently available as module in markets. Also, discrete devices can be used to construct suitable switch cells. Advantage of this switch structure is that each level module unit requires only one isolated power supply instead of two for the gate driver.

As a result, the construction cost of the proposed topology is lower than other conventional and multilevel inverters with reduced number of switches. The generalized structure of the proposed multilevel inverter is given in Fig. 2. It is shown that this structure consists of two basic parts. The first is the side of level module units producing DC voltage levels. The second is H-bridge topology, which generates both of the positive and the negative output voltages.

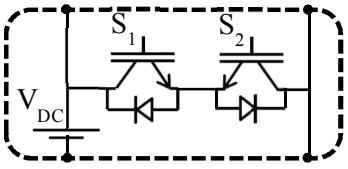

Fig. 1. A level module unit

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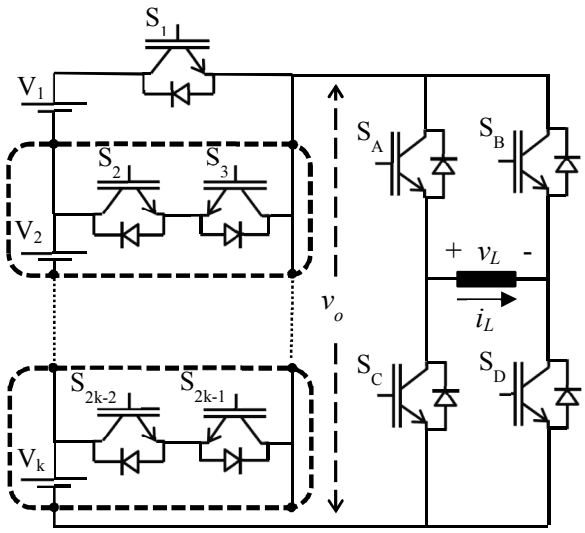

Fig. 2. The proposed structure of multilevel inverter

It is clear that system can be easily expanded by adding level module units and the voltage level number in the multilevel inverter can be increased.

Considering that k is the number of discrete DC voltage sources, the maximum and minimum values of output voltage of level module units are

$$V_{o\_max} = kV_{dc} \quad (1)$$

$$V_{o\_min} = 0 \quad (2)$$

and if the power switches is turn on and turn off, $S_i(t) = 1$ and $S_i(t) = 0$ for $i = 1,2,\dots,(2k-1)$, respectively. So, the output voltage of level module units can be expressed by

$$v_o(t) = V_1 S_1(t) + [V_2 S_2(t) + V_3 S_4(t) \dots + V_k S_{2k-2}(t)] \quad (3)$$

The positive output voltage on the load is

$$v_L(t)^+ = [V_1 S_1(t) + V_2 S_2(t) + \cdots + V_k S_{2k-2}(t)][S_A(t) \,\&\, S_D(t)] \quad (4)$$

and the negative output voltage on the load is

$$v_L(t)^- = [V_1 S_1(t) + V_2 S_2(t) + \cdots + V_k S_{2k-2}(t)][S_B(t) \,\&\, S_C(t)] \quad (5)$$

As a result, the overall output voltage of the proposed multilevel inverter can be given as follows:

$$v_L(t) = v_L(t)^+ + v_L(t)^- \quad (6)$$

The maximum and minimum values of the generated output voltage are respectively

$$V_{L\_max} = kV_{dc} \quad (7)$$

$$V_{L\_min} = -kV_{dc} \quad (8)$$

If all discrete DC voltage sources V_k in Fig. 2 are equal, the number of the output voltage levels N_{level} is

$$N_{level} = 2k + 1 \quad (9)$$

The number of switches used is

$$S_{number} = 2k + 3 \quad (10)$$

This value is 4k in the H-bridge cascaded multilevel inverter.

III. The Control Strategy of Proposed Topology

In this paper, the number of switching angles N_α which need to be calculated has been changed according to the number of output voltage levels. This quantity is also same as the number of DC voltage sources as seen in (11). The used switching angles have been calculated by (12).

$$N_\alpha = k = \frac{N_{level}-1}{2} \quad (11)$$

$$\alpha_j = arcsin\left(\frac{2j-1}{N_{level}-1}\right) \quad j = 1,2,..,k \quad (12)$$

In Fig. 3, the angles required are illustrated to obtain a full period of the output voltage in 5-level multilevel inverter. It is clear that the other angles can be easily derived from α_1 and α_2.

The states of switches which cannot be on simultaneously are given in Table I in order to avoid a short circuit as understood from Fig. 2.

There are ten different switching states to obtain a full period of the output voltage in 5-level multilevel inverter. The used switching state quantities can be expressed by $N_{level} + 5$ according to the number of output levels or by $2k + 6$ according to the number of DC voltage sources. All states of switches are presented for 5-level multilevel inverter in Fig. 4.

The output voltage is 0 for states in Fig. 4(a) and 4(b). While the direction of load current is positive, the current flows through D_B and S_A. While it is negative, it flows through S_C and D_D.

The load voltage for states in Fig. 4(c) and 4(d) is $+V_{DC}$. If the direction of load current is positive, it is used the state in Fig. 4(c). If it is negative, which this is the regenerative mode, it is used the state in Fig. 4(d).

The voltage for states in Fig. 4(e) and 4(f) is $-V_{DC}$. If the direction of current is positive, the current flows through D_B, S_3, D_2, V_2 and D_C, where the energy regeneration has been done to source as shown in Fig. 4(e). If the direction of current is negative, the current flows through S_2, D_3, S_B and S_C as shown in Fig. 4(f).

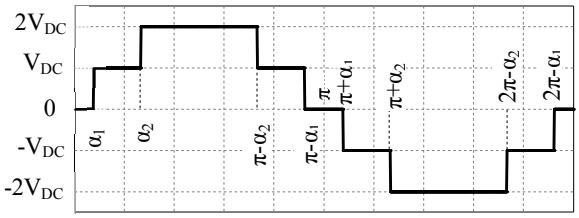

Fig. 3. The output waveforms of 5-level

TABLE I. Inconvenient Switch States in the Proposed Multilevel Inverter

Switches cannot be on simultaneously						
1	S_A	S_C				
2	S_B	S_D				
3	S_1	S_3	S_5	S_7	…	S_{2k-1}

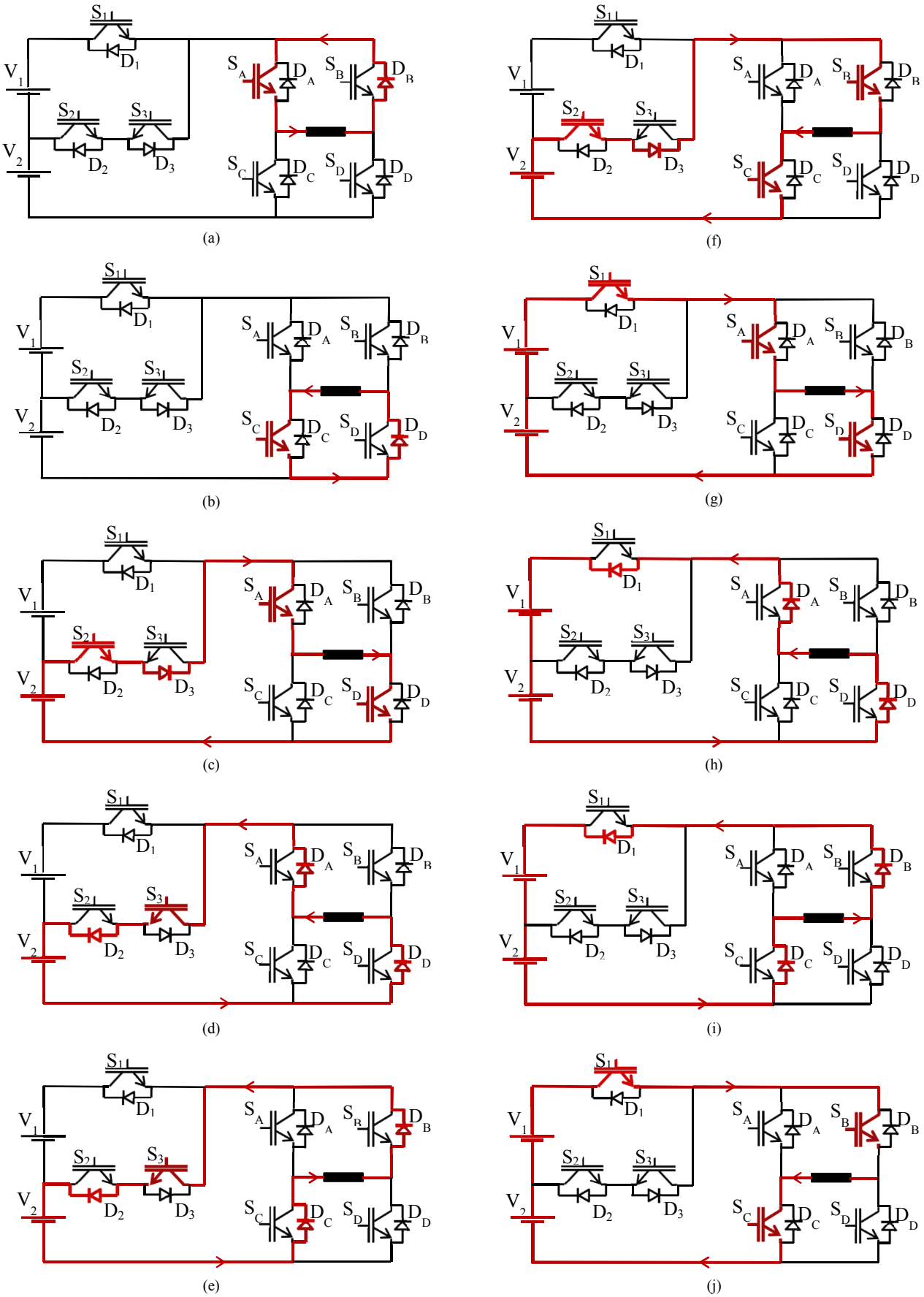

Fig. 4. The working topologies of 5-level multilevel inverter

a) $v_L = 0,\ i_L = +$ b) $v_L = 0,\ i_L = -$ c) $v_L = V_2,\ i_L = +$ d) $v_L = V_2,\ i_L = -$ e) $v_L = -V_2,\ i_L = +$
f) $v_L = -V_2,\ i_L = -$ g) $v_L = V_1 + V_2,\ i_L = +$ h) $v_L = V_1 + V_2,\ i_L = -$ i) $v_L = -(V_1 + V_2),\ i_L = +$ j) $v_L = -(V_1 + V_2),\ i_L = -$

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Fig. 4(g) and 4(h) is $+(V1+V2)$. The direction of current is positive in Fig. 4(g) and it flows from S_1, S_A and S_D. The direction of current is negative in Fig. 4(h) and it flows from D_A, D_1, V_1, V_2 and D_D.

The voltage for states in Fig. 4(i) and 4(j) is $-(V1+V2)$. The direction of load current is positive in Fig. 4(i) and it flows from the load to the source (regenerative mode). The direction of load current is negative in Fig. 4(j). All working states of power switches of the proposed 5-level multilevel inverter are summarized in Table II.

TABLE II. THE OUTPUT VOLTAGE AND CURRENT VALUES FOR STATE OF POWER SWITCHES IN THE PROPOSED 5-LEVEL MULTILEVEL INVERTER

	States of power switches							*voltage current*	
	S_1	S_2	S_3	S_A	S_B	S_C	S_D	V_L	i_L
1	off	off	off	on	off	off	off	0	+
2	off	off	off	off	off	on	off	0	-
3	off	on	off	on	off	off	on	V_1	+
4	off	off	on	off	off	off	off	V_1	-
5	off	off	on	off	off	off	off	$-V_1$	+
6	off	on	off	off	on	on	off	$-V_1$	-
7	on	off	off	on	off	off	on	V_1+V_2	+
8	off	off	off	off	off	off	off	V_1+V_2	-
9	off	off	off	off	off	off	off	$-(V_1+V_2)$	+
10	on	off	off	off	on	on	off	$-(V_1+V_2)$	-

IV. RESULTS

Since the aim of this study is to introduce a novel multilevel inverter, it has not been mentioned about the improving of total harmonic distortion. Some simulation results for 5-level and 7-level inverters have been given to evaluate the performance of the proposed novel multilevel inverter in the synthesis of a requested load voltage waveform. In this study, a 5-level inverter and a 7-level inverter can generate staircase voltage waveform respectively with maximum 200 V and 300 V, due to the values of the used DC voltage sources are 100 V. The simulated multilevel inverters have been loaded by two different loads. The previous load is a pure resistive; its value is 5 Ω. The next one is a series connected resistance and inductance; their values are 1 Ω and 15 mH. In this study, the fundamental frequency switching pattern has been utilized. This switching pattern causes less switching losses from other patterns due to its low switching frequency [11]-[15].

In Fig. 5, the gate signals of all switches in 5-level multilevel inverter are clearly shown. While the staircase output voltage is synthesized, the power flow in this switching structure is bidirectional, both from source to load and from inductive load to source.

Fig. 6 shows the voltage and current of 5-level multilevel inverter for pure resistive load. It is shown that the waveform of the load current is the stepped. Also, it has a unity power factor. The voltage and current of 5-level multilevel inverter for R-L load is illustrated in Fig. 7. The output voltage is same as in Fig. 6, but the output current has sinusoidal waveform with a fundamental frequency due to inductive load. Also, the power factor is not unity.

However, the number of the output voltage levels should be enhanced to obtain the load voltage and current with lower harmonic contents. The output voltage and current waveforms of 7-level multilevel inverter are given for pure resistive and R-L loads in Fig. 8 and Fig. 9, respectively.

It is understood that the more the number of levels are increased, the more the output waveforms are similar to the pure sinusoidal. The number of output levels in the proposed multilevel inverter can be easily increased by connecting the level module units.

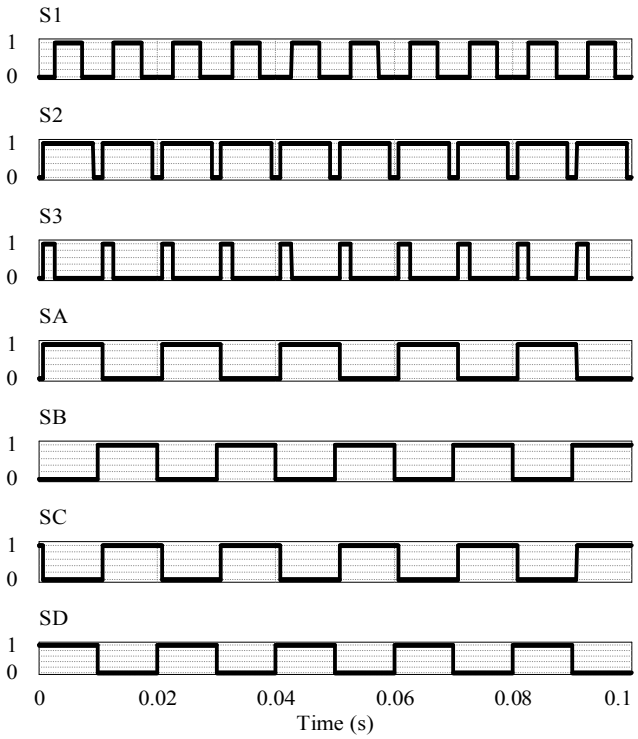

Fig. 5. Gate signals of all switches in 5-level multilevel inverter

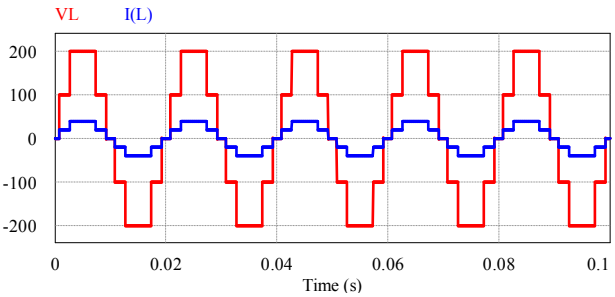

Fig. 6. The output voltage and current of 5-level multilevel inverter for pure resistive load

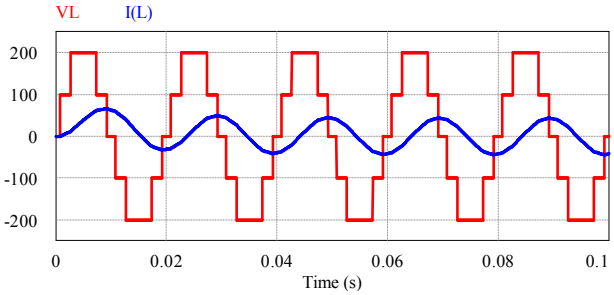

Fig. 7. The output voltage and current of 5-level multilevel inverter for series R-L load

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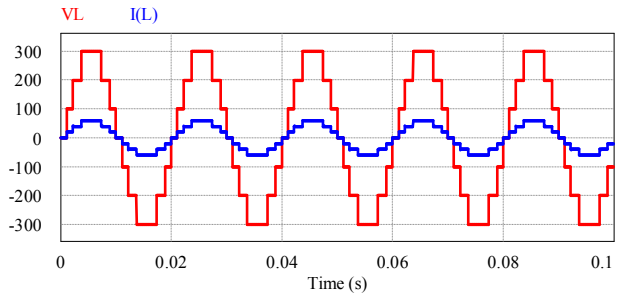

Fig. 8. The output voltage and current of 7-level multilevel inverter for pure resistive load

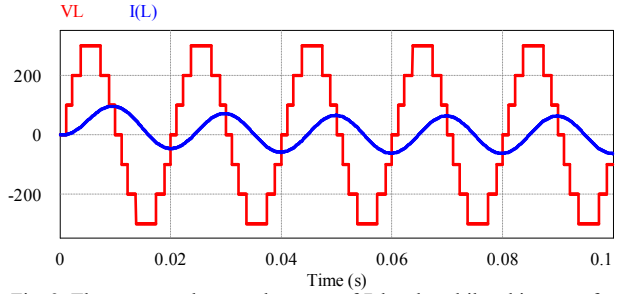

Fig. 9. The output voltage and current of 7-level multilevel inverter for series R-L load

V. Conclusion

A novel structure of multilevel inverter which needs the minimum number of switches has been proposed. The modulation technique and calculation of conducting angles for the proposed topology has been introduced. The additional level module units have been use to increase the output levels. Since the devices in the level module units are common emitter back to back, each unit has been required only one isolated power supply for driver. Therefore, construction cost of the proposed multilevel inverter is lower and it is not bulky. The operation and performance of the proposed structure has been proved by simulations of 5-level and 7-level multilevel inverter.

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