Error Analysis of Trigonometric ADC

Hui Fang

***Abstract*—In order to fabricate high speed and low cost ADC, a new type Analog-to-Digital converter (ADC) was presented on the basis of the periodicity of trigonometric function. This kind of ADC is defined as T-ADC. Each bit conversion of T-ADC is performed nearly in parallel. An N-bit T-ADC consists of a trigonometric function circuit, N□1 groups of analog multipliers and operational amplifiers, N comparators, and a decoder. The input voltage is mapped to cosine of the corresponding angle first. Then the angle in cosine function is doubled N −1 times. All the cosine function voltages of the doubled angles are used to generate the result of A/D conversion. Theoretically, T-ADC can achieve the conversion speed of flash ADC. In this paper, the sources of error in T-ADC and their influences on T-ADC are analyzed. Based on it, an error reduction approach in T-ADC is presented.**

***Index Terms*—trigonometric ADC, error analysis, INL, DNL**

I. Introduction

HIGH speed analog-to-digital converter (ADC) is required for digital X-ray image capture, communication, etc [1], [2]. In the existing high speed ADC architectures, the analog input voltage is compared against reference voltages. By investigating the successive approximation ADC [3], flash ADC [4], pipeline ADC [5] and folding ADC [6], we found comparison of each bit in parallel accelerates the ADC process, and grouping the compared bits reduces circuit area and power consumption [7]. If the different groups of bits are transformed in parallel, such as in the folding architecture, ADC can achieves a better balance among power dissipation, clock frequency, resolution, and chip area.

An N-bit n-group ADC needs $n\times(2^{N/n}-1)$ comparators. If n is equal to N, it only requires N comparators. In other words, if the N bits are produced in parallel (or nearly in parallel), it can realize an optimum ADC with low chip area, power consumption and high conversion resolution and speed.

Based on this, we presented a new type of ADC utilizing the periodicity of trigonometric function [7]. It is referred as trigonometric ADC, or T-ADC in brief. Because of parallel operation among each bit and simplicity of its decoder, the convention time of T-ADC is almost same as that of flash ADC. In this work, we analyze the sources and features of error in the T-ADC in order to guide further study on its design and associated applications.

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II. The Principle of ADC Based on Periodicity of Trigonometric Function

Suppose the input voltage v_i of ADC is in the range of $[V_l, V_u]$. It is mapped to $v_0 = \cos\varphi$ by a trigonometric function circuit [7] first, where $\varphi \in [0, \pi]$, and

$$\varphi = \frac{\pi}{(V_u - V_l)}(v_i - V_l) \tag{1}$$

When $\varphi = \pi/2$, i.e. $v_i = (V_l + V_u)/2$, $v_0 = 0$.

The T-ADC circuit also generates signal $v_1 = \cos2\varphi$ according to the following equation,

$$\cos2\varphi = 2\cos^2\varphi - 1 \tag{2}$$

v_1 has two zero-crossing points at $\varphi_{010} = \pi/4$ and $\varphi_{011} = 3\pi/4$, corresponding to $v_i = V_l + (V_u - V_l)/4$ and $v_i = V_l + 3(V_u - V_l)/4$.

Equation (2) is further applied repeatedly to produce signals $v_n = \cos2^n\varphi$ (where, n = 2, 3, …, N −1). v_n has 2^n zero-crossing points at $\varphi_{0nk} = (2k+1)\pi/2^{n+1}$ (where, k = 0, 1, …, 2^n-1), corresponding to $v_i = V_l + (2k+1)(V_u - V_l)/2^{n+1}$. The period of v_n is $2\pi/2^n$, and there are two zero-crossing points in every period. Each period of v_{n-1} is folded into 2 segments in v_n.

N comparators with the threshold of 0V are needed to translate v_n (n = 0, 1, …, $N-1$) to digital signal b_n. The combination of b_n are different for various input voltage v_i. A N-to-N decoder transforms b_n to binary code, D_n, which is commonly employed to reflect the value of input voltage in digital system.

Fig 1 exemplifies the principle of the T-ADC with N = 3, where the range of input voltage is [0, 1]. The range of input signal is folded 2^{N-1} times.

In T-ADC, all the N bits are converted in parallel, as shown in Fig 2. The trigonometric function circuit CC maps the input signal v_i to cosine function $v_0 = \cos\varphi$. The cosine function can be fitted by the following polynomial

$$\cos\varphi = \sum_{m=0}^{M} w_m {v_i}^m \tag{3}$$

Where, M is the highest order of power of v_i, w_m is the coefficient of the m-th power. The more items are on the right side of (3), the more precise of $\cos\varphi$ would be, although more circuits are needed in implementation. There is a tradeoff between precision of (3) and simplicity of circuit. Multipliers and operational amplifier are used in CC to implement the function in Equation (3).

$N-1$ groups of analog multipliers (Mul_n) and operational amplifiers (OP_n) generate $v_n = \cos2^n\varphi$ (n = 1, 2, …, $N-1$) according to double angle formula of cosine function (2). Square of $\cos2^{n-1}\varphi$ is produced by the Mul_n. The OP_n implements function of doubling and subtracting 1. The shaping circuit SC_n (n = 0, 1, …, $N-1$) converts $v_n = \cos2^n\varphi$ to

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digital signal b_n as shown in Fig 1. In Fig 1 N is supposed to be 3 and the input range is supposed to be [0, 1]. The range of input signal is folded 2^{N-1} times. Table I lists all the combinations of b_0, b_1, b_2 corresponding to the various value of input voltage. The values of binary code D_0, D_1, D_2 are also list. It can be seen that b_0 corresponding to the MSB and b_2 to the LSB of the binary code.

Each SC_n is a comparator with threshold of 0V. The decoder transforms the results of N comparators, b_0, b_1, …, b_{N-1}, to binary code D_0, D_1, …, D_{N-1} according to the periodicity of trigonometric function. The combinational logic circuits can be used in this purpose. However, the irregular structure of combinational logic circuits may consume larger silicon area [8]. Fortunately, in T-ADC, the numbers of input and output of the decoder are N, not as large as those of flash ADC. When $N > 5$, a T-ADC has less area and power consumption than a flash ADC of same resolution [7]. The simple decoder circuit and simultaneity of analog and digital transformation in T-ADC makes its total conversion time be about the same as the delay time of decoder in flash ADC [7].

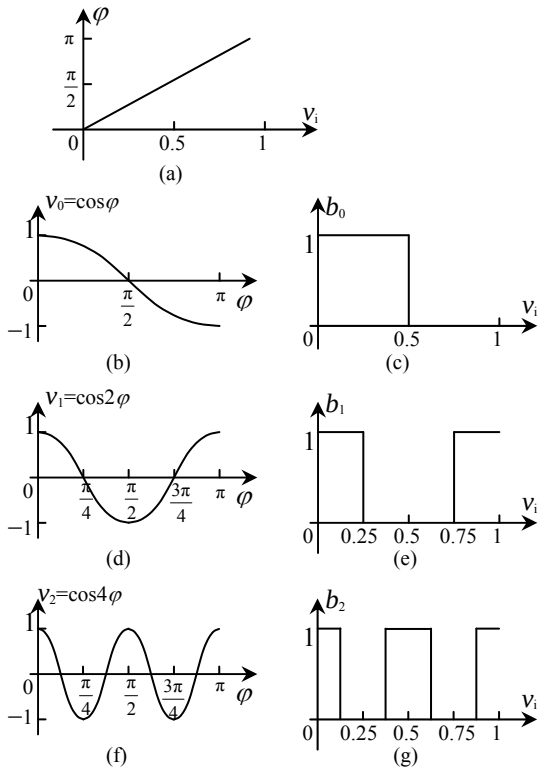

Fig 1. The principle of a 3-bit T-ADC. (a) Mapping input v_i to angle φ; (b) $\cos\varphi$, (c) b_0 corresponding to $\cos\varphi$; (d) $\cos2\varphi$, (e) b_1 corresponding to $\cos2\varphi$; (f) $\cos4\varphi$, (g) b_2 corresponding to $\cos4\varphi$.

III. The Theoretical Error

The errors of T-ADC come from its operation principle and non-ideality of actual circuit. In Equation (3), M needs to be ∞ in order to have the left side be equal to the right side strictly. But, with the limit of circuit, M is a finite integer. This leads to the theoretical error of T-ADC. The non-ideality errors stem from analog multipliers and operational amplifiers. The non-ideality error of operational amplifiers is less severe than that of analog multipliers. Thus we only discussed the impact of the non-ideality error of analog multipliers and the way to suppress such kind error here.

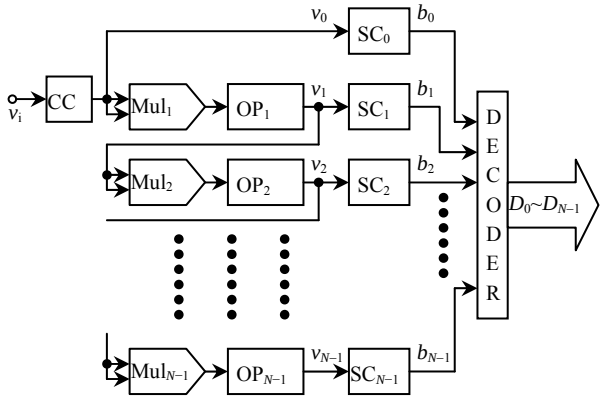

Fig 2. The structure of T-ADC.

TABLE I
COMBINATIONS OF OUTPUT OF COMPARATORS WITH DIFFERENT VALUE OF INPUT SIGNAL, AND CORRESPONDING BINARY CODE

v_i	b_0	b_1	b_2	D_2	D_1	D_0
(0V, 0.125V]	1	1	1	0	0	0
(0.125V, 0.25V]	1	1	0	0	0	1
(0.25V, 0.375V)	1	0	0	0	1	0
[0.375V, 0.5V]	1	0	1	0	1	1
(0.5V, 0.625V]	0	0	1	1	0	0
(0.625V, 0.75V)	0	0	0	1	0	1
[0.75V, 0.875V)	0	1	0	1	1	0
[0.875V, 1V]	0	1	1	1	1	1

Note: $b_n = 1$ if $v_n \geq 0$ (n = 1, 2, 3), otherwise $b_n = 0$.

According to Taylor's series, the larger M is, the less error of Equation (3) would be. However, the increase of M enlarges circuit area and the signal delay between v_i to v_0 in CC. To reduce the error from the terms higher than v_i^M, the weights of the terms left should be adjusted from those in standard Taylor's series of trigonometric function. These weights could be obtained by curve fitting Equation (3).

When $M = 8$, $N = 12$ and the weights are taken as in Table II, the integral nonlinearity (INL) keeps less than 2LSB, as shown in Fig 3.

TABLE II
VALUES OF COEFFIENTS IN EQUATION (3) WHEN $M = 8$ AND $N = 12$

Coefficient	w_2	w_4	w_6	w_8	Others
Value	–4.933	4.043	–1.289	0.179	0

IV. The Error form Analog Multipliers

T-ADC utilizes analog multipliers to map v_i to $\cos\varphi$ and to double angles in cosine function. The non-ideality of analog multipliers is discussed here. Since the angle in v_n are used to calculate the angle in v_{n+1}, this kind error is cumulative from n = 1 to $N-1$.

The output of analog multipliers in T-ADC is either positive or zero. Suppose the ideal output of analog multiplier is v_{coi}. The actual output v_{co} may deviate from it, as shown in Fig 4. The larger the absolute value of ideal output is, the more deviation will be [9], [10]. To simplify illustration, we assume the non-ideality of the analog multiplier is αv_{coi}, as shown in Equation (4).

$$v_{co} = v_{coi}(1 - \alpha v_{coi}) \quad (4)$$

where, α reflects deviation level of actual output. In our

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T-ADC, the maximum of v_{coi} is 1, α is the maximum deviation of the actual output when $v_{coi} = 1$.

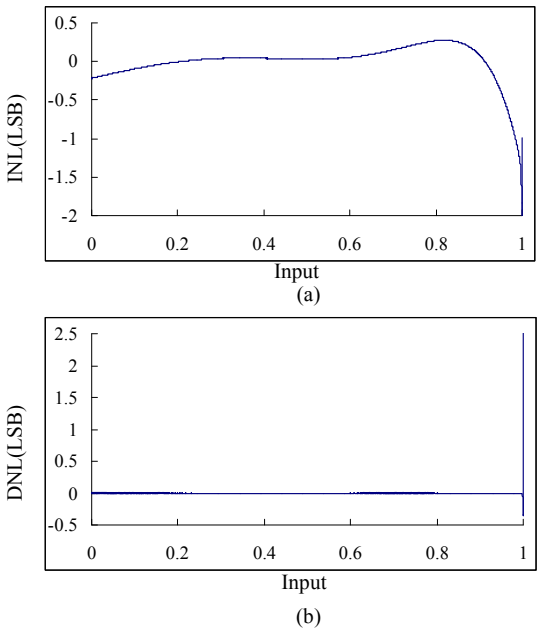

Fig 3. INL and DNL of 12-bit T-ADC when only theoretical error is considered. (a) INL for $M = 8$; (b) DNL for $M = 8$.

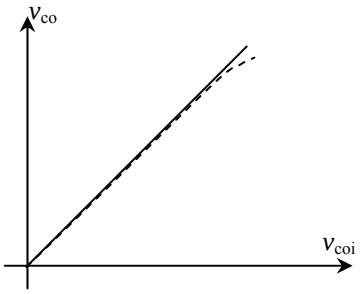

Fig 4. The output of analog multiplier. Solid line is the ideal output, dashed line is actual output.

Fig 5 shows INL and DNL with $\alpha = 0.005$. Main and larger errors occurs at zero cross points of $\cos 2n\varphi$ and two ends of input range.

To eliminate the errors induced by the non-linearity in analog multipliers, each Mul in Fig 2 is replaced by the circuit shown in Fig 6(b). The output of circuit in Fig 6(b) is:

$$v_{co}' = v_{co} / (1 - \alpha) = v_{coi}(1 - \alpha v_{coi}) / (1 - \alpha) \quad (5)$$

When $v_{coi} = 1$V, $v_{co}' = v_{coi}$. The term $1/(1 - \alpha)$ is realized by the Amplifier (A). The resistance of the FET in the feedback path is controlled by V_c which is generated by the circuit shown in Fig 6(a). In Fig 6(a), the feedback control circuit (FBCC) adjusts the V_c to maintain the output of the Amplifier (v_c) at 1V, which is the ideal output of the Mul. T-ADC can be implemented one set of circuit shown in Fig 6(a) to produce V_c, which is used by all the modified MUL circuits.

Fig 7 (a) and (b) show INL and DNL of T-ADC when each Mul in Fig 2 is modified by the circuit show in Fig 6(b) with $\alpha = 0.005$. Compared with Fig 5 (a) and (b), the error of T-ADC caused by the non-linearity of Mul has been reduced by roughly about 10 times after modification. When the non-linearity of MUL is mended to $\alpha = 0.001$, the INL and DNL of T-ADC outperform its theoretical limits, as shown in Fig 7 (c) and (d).

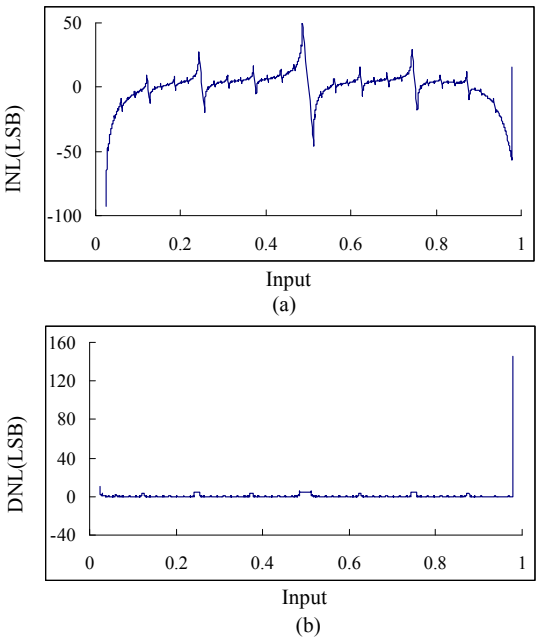

Fig 5. INL and DNL of 12-bit T-ADC when analog multiplier linear error is considered. (a) INL and (b) DNL for $\alpha = 0.005$; $\cos\varphi$ is generated by Equation (3) with $M = 8$ and the weights in Table II.

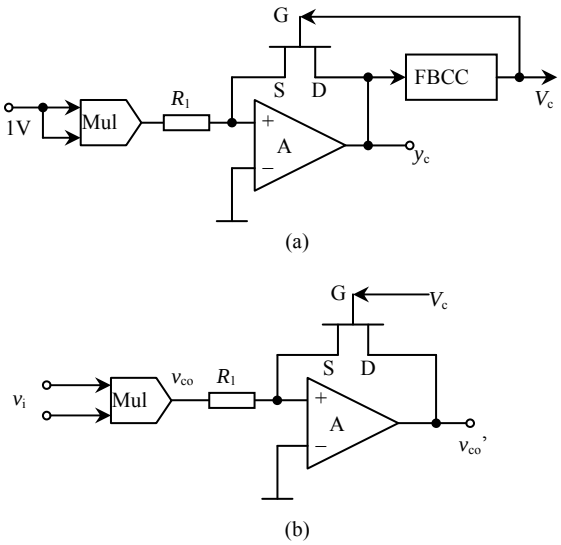

Fig 6. Modification for each Mul in Fig 1 to eliminate the negative effect of non-linearity of Mul.

V. Conclusion

The periodicity of trigonometric function can be utilized in ADC to realize N-bit conversion almost in parallel with only N circuit units [7]. In each circuit unit of this T-ADC, signals in the form of cosine function of angle are compared against a fixed zero voltage. The role of periodicity of trigonometric function is to avoid the signal in each circuit unit exceed the preset range when the signals represented by angles are doubled from one unit to the next.

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In this work, the theoretical errors of T-ADC are analyzed. T-ADC may provide potential solution to reduce circuit area as well as power consumption of ultra-high speed ADC. To achieve this goal, it requires more precise multiplier first. We will design and simulate T-ADC with HSPICE in further work.

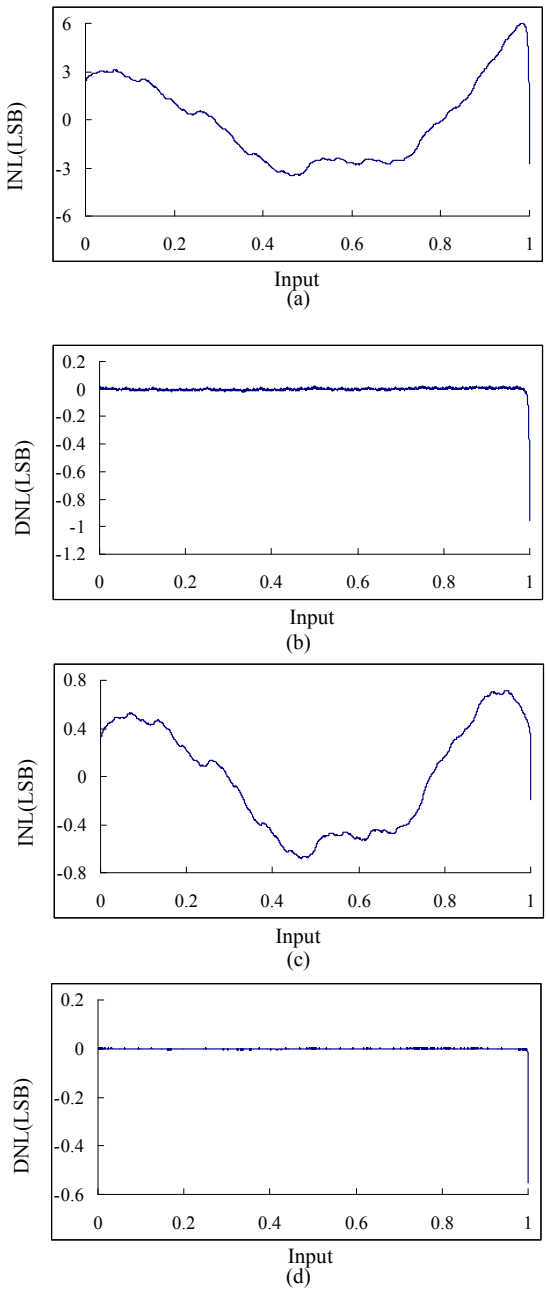

Fig 7. INL and DNL of 12-bit T-ADC when analog multiplier linearity error is corrected with the circuit in Fig 6. (a) INL and (b) DNL when $\alpha = 0.005$, (c) INL and (d) DNL when $\alpha = 0.001$. In (a) to (d), $\cos\varphi$ is generated by Equation (3) with $M = 8$ and weights in Table II.

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