CMOS Differential Amplifier Area Optimization with Evolutionary Algorithms

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***Abstract*—This work presents efficient constrained optimization methods for sizing of a differential amplifier with current mirror load. The aim is to minimize MOS transistor area using three evolutionary algorithms, differential evolution, artificial bee colony algorithm and harmony search. Simulation results demonstrate that proposed methods not only meets design specifications and accommodates required functionalities but also accomplishes the design objective and improves some design specifications in a shorter computational time with respect to previous method.**

Keywords—; analog integrated circuit sizing; differential evolution; harmony search; artificial bee colony; constrained optimization

I. Introduction

Analog circuit synthesis is the process of designing and constructing a network to meet the multiple and complex performance specifications by the large number of design variables. Robust analog circuit design which fulfill the design constraints in several different operating environments and under the influence of manufacturing process variations is a very important, complex and time consuming task [1,2]. Optimal CMOS transistor sizing for minimum area oriented optimization, which is only a part of a complete analog circuit CAD tool remains between topology selection and actual circuit layout [3]. Those two tasks are beyond the scope of this work.

An evolutionary algorithm (EA) based transistor sizing approach of a differential amplifier with current mirror load for minimum occupied MOS transistor area is presented. Here, population based nature–inspired three EA methods are used to synthesize a CMOS differential amplifier where bias current and MOS transistor sizes are optimized for minimum area requirement while fulfilling particular design specifications such as gain, power dissipation, slew rate, phase margin, common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), input common-mode range (ICMR) considering design objective. EA methods have been successfully utilized for various analog integrated circuit design schemes [4]. In literature, particle swarm optimization (PSO) [3,5], genetic algorithm (GA)[6], differential evolution (DE) [7,8], non-dominated sorting genetic algorithm NSGA [8,9] techniques have been used for optimizing analog circuits such as a operational transconductance amplifier, differential amplifiers, analog active filter and operational amplifier, low noise amplifiers.

In [6], GA method is used for active filter transfer function providing desired feature implemented with adjusted component instead of standard resistance.

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Besides, gain maximization [10] objective of a two stage operational amplifier are accomplished with GA. Seven real world cases such as buffer, amplifiers, delay, NAND of IC design were evaluated by DE algorithm considering circuit area as design goal in [7]. DE method is utilized for sizing of operational transconductance amplifier considering power minimization and gain maximization and results are compared with NSGA in [8]. In [3,5] PSO is applied for transistor area minimization of two stage operational amplifier and differential amplifier while fulfilling particular design specifications. Optimum device sizes are obtained by NSGA for low noise amplifiers using in RF receivers.

In this work, DE, HS and ABC algorithms are applied for automated sizing of CMOS differential amplifier. Among them, ABC algorithm has not been used for analog sizing beforehand. The comparative performances of the optimizing circuit using these algorithms have been evaluated in terms of design criteria and computational efforts.

Rest of the paper is organized as follows. Brief information about differential evolution, harmony search and artificial bee colony methods is given in section II. Section III describes design procedure for differential amplifier. Simulation results of EA based sizing methodology are presented in section IV. Finally, concluding remarks and comments are given in section V.

II. Evolutionary Algorithms

Evolutionary algorithms (EA) are iterative in nature and may move to not-necessarily improving solutions which avoids being stuck at local minima [11]. DE, HS and ABC algorithms are three evolutionary methods used for CMOS differential amplifier sizing. All of them utilize constrained procedures where new solutions are not generated unless constraints are satisfied. Details of those are provided in the following.

A. Differential Evolution

DE is a real coded population-based optimization technique based on parallel direct search method and diverges from GA by adding the weighted difference between two chromosomes to the third in order to generate new ones [12].

DE uses a population P having NP individuals that evolves over G generations to reach the optimal solution. Each individual Xi is a vector that features a dimension size of D. Each vector in population matrix is assigned as follows.

$$X_j=X_j^{min}+\eta_j(X_j^{max}-X_j^{min}),\ j=1,\ldots,D \qquad (1)$$

where X_j^{max}, X_j^{min} are the upper, lower bounds, respectively and η_j is a uniformly distributed random number within [0,1] of the j^{th} feature. The optimization process in DE

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is carried out using three operations; mutation, crossover and selection. Mutation operator generates mutant vectors ($X_i^{'}$) according to (2)

$$X_i^{'(G)} = X_a^{(G)} + F(X_b^{(G)} - X_c^{(G)}),\ a \neq b \neq c \neq i \tag{2}$$

where X_a, X_b and X_c are randomly selected vectors among population matrix including NP different vectors. F is the scaling constant used to improve algorithm convergence. The crossover operation is employed to create trial vectors ($X_i^{''}$) by mixing the individuals of the mutant vectors ($X_i^{'}$) with the target vector (X_i) according to (3)

$$X_{i,j}^{''(G)} = \begin{cases} X_{i,j}^{'(G)}, if\ (\eta_j^{'} \leq C_R) or (j = q) \\ X_{i,j}^{(G)}, otherwise \end{cases} \tag{3}$$

where q is a randomly chosen index within [1,NP], guaranteeing that trail vector employs at least one individual from the mutant vector. C_R is the crossover constant within [0,1] that controls the population diversity. Finally selection operator compares the fitness values of trial vectors and target vectors. If trial vectors yield better fitness values then they replace the target vectors with which they were compared, otherwise predetermined population member is retained. The above procedure restarts until the chromosomes have been successfully updated to improve their fitness values to a specified value [12].

B. Harmony Search

HS is based on the improvisation process of jazz musicians [13]. HS searches an optimal combination of inputs by usage of harmony memory, pitch adjusting and randomization just as musicians seek a fantastic harmony by playing any known tune from their memory, playing a similar tune or composing new and random notes.

Initial population structure of HS is very similar to that of DE as explained in the previous subsection. Here, the total number of individuals is equal to harmony memory size (HMS) and individuals are stored in harmony memory (HM). Following, a new solution is improvised according to harmony memory considering rate (HMCR). A stored value is chosen from HM with probability of HMCR (0≤HMCR≤ 1) and 1-HMCR is the probability of generating it randomly. If the solution is picked from HM, it is mutated according to the pitch adjust rate (0≤PAR≤ 1). After HM is updated the fitness values are evaluated. If the improvised solution yields a better fitness than that of the worst member in HM, it replaces the worst one. Otherwise the improvised one is eliminated. The above procedure is repeated until a preset termination criterion (maximum iterations or a target fitness value) is met [13].

C. Artificial Bee Colony

ABC algorithm is a recently introduced optimization algorithm and simulates the foraging behavior of bee colony [14]. Position of a food source represents a possible solution to the optimization problem and the nectar amount of a food source corresponds to the quality (fitness) of the associated solution. First of all, the food source positions are randomly initialized as x_i (i=1,…,SN) where SN is the maximum number of the food sources. Each employed bee, whose total number equals to the the number of food sources, produces a new food source in her food source site as given in (4).

$$v_{ij} = x_{ij} + \varphi_{ij}(x_{ij} - x_{kj}) \tag{4}$$

where φ_{ij} is a uniformly distributed real random number within the range [-1,1], k is the index of the solution chosen randomly from the colony and j is the index of the dimension of the problem. After producing v_{ij}, this new solution is compared to x_{ij} solution and the employed bee exploits a better source while each onlooker bee whose total number is equal to the number of employed bees selects a food source with the probability as given in (5).

$$p_i = \frac{fit_i}{\sum_{j=1}^{SN} fit_j} \tag{5}$$

where fit_i is the fitness of the solution x_{ij} and produces a new source in selected food source site by (4). After all onlookers are distributed to the sources, sources are checked whether they are to be abandoned. The employed bee associated with the abandoned source becomes a scout and makes random search in problem domain by (6). The best food source found so far has been memorized and the production steps are repeated until the stopping criterion is met [14].

$$x_{ij} = x_j^{\min} + (x_j^{\max} - x_j^{\min}) * rand \tag{6}$$

III. Design Procedure for Differential Amplifier

The differential amplifier is one of the most versatile analog circuits and serves as the input stage to most operational amplifiers [3,15-16]. The problem considered here is the optimal selection of CMOS transistor dimensions and bias current for differential amplifier with current mirror load (Fig.1), which is only a part of a complete analog circuit CAD tool.

It can be characterized by a number of specifications [15,16] such as common mode rejection ratio (CMRR), slew rate (SR), power dissipation (P_{diss}), small signal characteristics (A_v , f_{-3dB}), input common mode range (ICMR), power supply rejection ratio (PSRR)

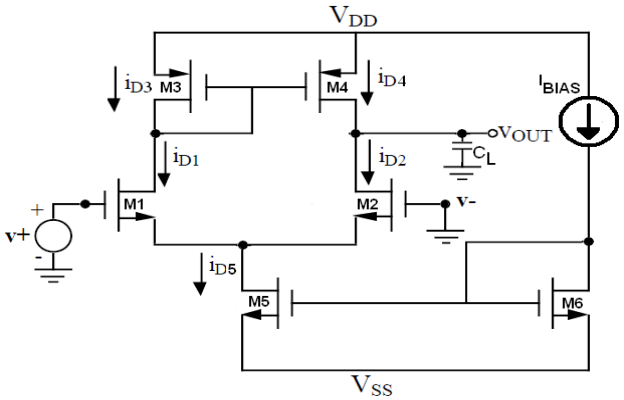

Fig. 1. Differential amplifier with current mirror load [3,15-16]

In this work, performance metrics as well as design objective which can be defined as CF is the minimization of the occupied MOS transistor area as in (7).

$$CF = \sum_{i=1}^{T} \left(W_{(i)} x L_{(i)} \right) \tag{7}$$

In order to ensure that all design constraints of small-signal differential voltage gain (A_v), cutoff frequency (f_{-3dB}), maximum and minimum input common mode voltages ($V_{IC(max)}$, $V_{IC(min)}$), slew rate (SR), power dissipation (P_{diss}) and design variables of output capacitance (C_L) and MOS device sizes meet the desired bounds, general design procedure can be summarized below [15]:

- Determine range of I_{d5} (I_{ss}) to satisfy the slew rate (SR) and power dissipation (P_{diss}).

$$I_{dmin}<I_{d5}<I_{dmax} \quad (8)$$

$$I_{dmax}=P_{diss}/(V_{DD}+|V_{SS}|) \quad (9)$$

$$I_{d\min} = \max\left(SRxC_L, \left(2/\left(\left(\lambda_n+\lambda_p\right)\ x\left(1/\left(2\pi f_{-3dB}C_L\right)\right)\right)\right)\right) \quad (10)$$

- Design W_1/L_1 (W_2/L_2) to satisfy A_v

$$A_v = \frac{v_{out}}{v_{id}} = \frac{g_{md}}{g_{ds2}+g_{ds4}} = \frac{(K_1' I_{ss} W_1/L_1)^{1/2}}{(\lambda_2+\lambda_4)(I_{ss}/2)} = \frac{2}{(\lambda_2+\lambda_4)}\left(\frac{K_1' W_1}{I_{ss} L_1}\right)^{1/2} \quad (11)$$

- Design W_3/L_3 (W_4/L_4) to satisfy the upper ICMR

$$V_{IC\,(max)} = V_{DD} - V_{SG3} + V_{TN1} \quad (12)$$

- Design W_5/L_5 (W_6/L_6) to satisfy the lower ICMR

$$V_{IC\,(min)} = V_{SS} + V_{DS5\,(sat)} + V_{GS1} = V_{SS} + V_{DS5\,(sat)} + V_{GS2} \quad (13)$$

- Obtain exact values of design variables and iterate if constraints have not been satisfied and design objective(s) has (have) not been met.

IV. Simulation Results

The aim of this study is to minimize total CMOS transistor area while satisfying design criteria and design variable constraints. Establishing design criteria and design variables to EA methods, the optimal circuit sizing was aimed to be determined the algorithm. Design problem has been introduced by composing an equation consists of input variables and design variables as a CF. The starting point of design consists of two types of information. First type of information such as the technology and the power supply is set by the designer. The other type is the design criteria. The range of each criteria and design variable, power supply values and technology information is set as an input to EA methods and DE, HS and ABC should obtain the solution set that consists the exact values of design variables $(W/L)_i$ where (i=1,…,6) and design criteria (f_{-3dB}, V_{IC}(max), V_{IC}(min), SR, P_{diss}, A_v) for given ranges. The design is implemented with the relationships that describe design specifications to solve for DC currents and W/L values of all MOS transistors. The appropriate relationships were provided in the previous section. Simulations are performed with TSMC 0.35 µm technology parameters.

DE, HS and ABC are utilized for a differential amplifier with current mirror load having design specifications of SR≥10V/µs, f_0≥100kHz (C_L=5pF), -1.25V≤ICMR≤1.25V, A_v>100 V/V, P_{diss}≤2mW, with PSO inputs of V_{DD}=-V_{SS}=2.5V, V_{tn}=0.4761V, V_{tp}=-0.6513V, K'_n=181.2µA/V^2, K'_p= 65.8µA/V^2. Constraints for design variables are set as, 100≥$(W/L)_i$≥1.5 MOSFET length values are chosen as L_i=1.4 µm where (i=1,…,6).

All design constraints can be employed as a vector in HS, DE, ABC given in (14).

$$x = [SR,\ A_v, f_{-3dB},\ V_{icmin},\ V_{icmax,}\ P_{diss}] \quad (14)$$

Simulations are performed in MATLAB environment with Intel Core 2 Duo CPU, T7300 @ 2.00GHz. Target value of CF is aimed to be smaller than 3x10^{-10}m^2. DE based design method resulted in a total MOS transistor area of 0.767x10^{-10} m^2 along with exact values of design parameters (W_i/L_i, I_{bias}) as given in Table I. Design parameters obtained with each EA method are them used for sizing of CMOS differential amplifier. SPICE simulation results of EA based CMOS differential amplifier design are given in Figs. 2-4.

Algorithm parameters and computational performance for EA methods are shown in Table II. Despite the fact that DE resulted in shortest computation time, minimum MOS transistor area is obtained with HS method when compared with DE, ABC and previous work. Among the EA methods, ABC provides better performances in terms of gain and power dissipation as given in Table III. Simulation results show that DE, HS and ABC resulted in shorter computational time than PSO. ICMR and cut-off frequency values of DE and ABC based design method are also improved when compared to that of PSO.

TABLE I. Design Parameters obtained with EA Methods

Design Parameters	PSO [3]	HS	DE	ABC
I_{bias} (µA)	125	88	99	83
$W_1/L_1, _2/L_2$ (µm/µm)	29.4/3.5	17.5/1.4	21.3/1.4	23/1.4
$W_3/L_3, W_4/L_4$ (µm/µm)	11.3/3.5	2.8/1.4	2.8/1.4	2.6/1.4
$W_5/L_5, W_6/L_6$ (µm/µm)	4.2/1.4	2.8/1.4	3.3/1.4	2.5/1.4

TABLE II. Comparison of Computational Performance

	PSO [3]	HS	DE	ABC
Time	25.02 s	0.25 s	**0.026 s**	0.438 s
Iterations	582	1000	**6**	500
Algorith Parameters	**NP**=10	**HMS**=6	**NP**=10	**NP**=20
	$\mathbf{c_1}$=$\mathbf{c_2}$=1.7	**HMCR**= 0.9	**CR**=1	**FN**=10
	w = 0.9	**PAR**= 0.4-0.9	**F**=0.85	**Limit** = 100

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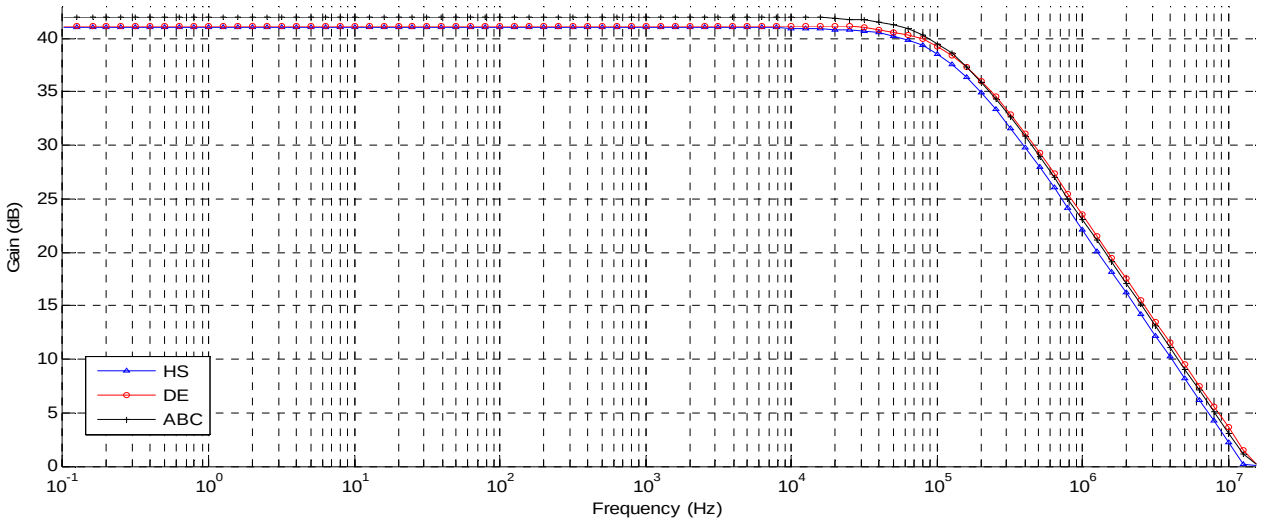

Fig. 2. Gain of EA based CMOS Differential Amplifier designs

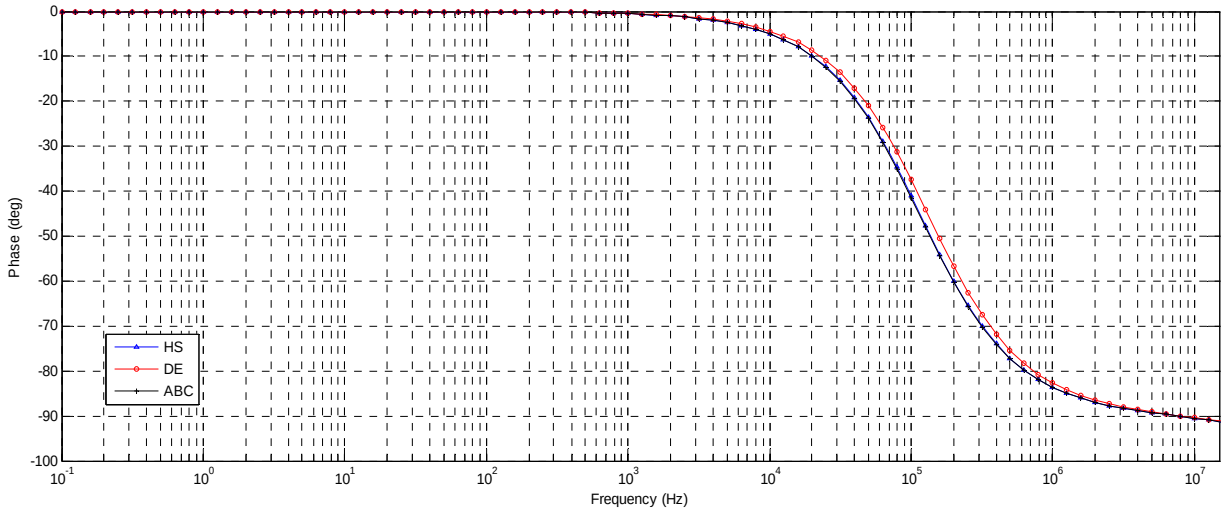

Fig. 3. Phase margin of EA based CMOS Differential Amplifier designs

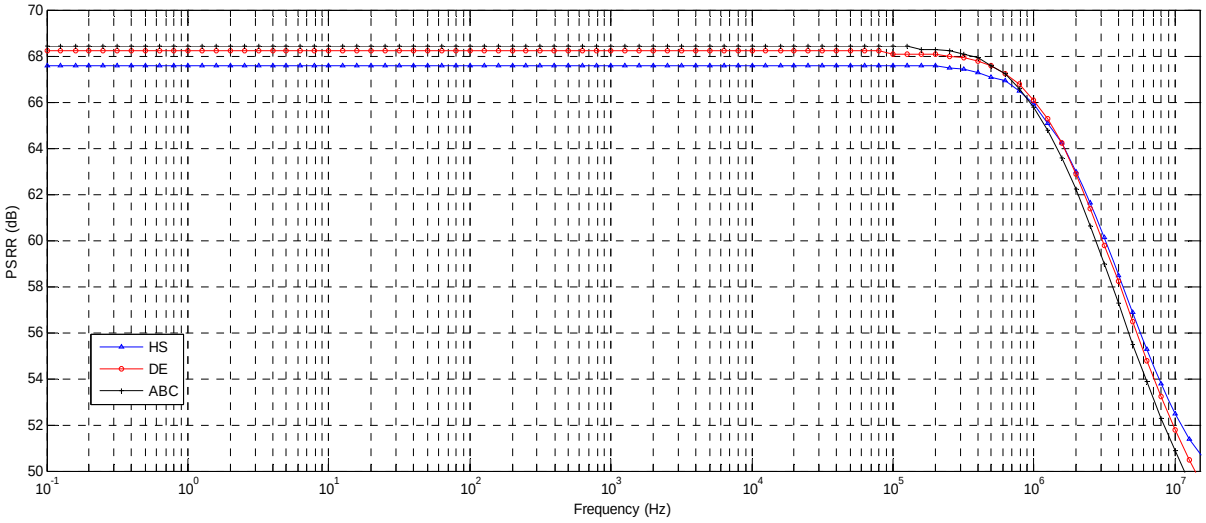

Fig. 4. PSRR of EA based CMOS Differential Amplifier designs

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TABLE III. COMPARISON OF PREVIOUS METHODS WITH DE AND HS BY MEANS OF DESIGN CRITERIA

Design Criteria	**Specifications**	**PSO [3] SPICE)**	**HS (SPICE)**	**DE (SPICE)**	**ABC (SPICE)**
Slew Rate (V/μs)	≥ 10	22.4	14.916	18.451	15.67
Power Dissipation (μW)	≤ 2000	1260	886	990	830
Phase Margin (^{o})	>45	83.8	89.1	88.81	91.248
Cut-off Frequency (KHz)	≥100	100	114	129.7	112.367
Gain (dB)	> 40	42	40.98	41.23	42.045
Vic_{min} (V)	≥-1.25	-0.8	-0.7	-0.92	-0.97
Vic_{max} (V)	≤1.25	1.4	1.2	1.15	1.2
CMRR (dB)	> 40	84.2	78.5	78.39	79.67
$PSRR^+$ (dB)	>40	40.1	42.93	43.14	43.857
$PSRR^-$ (dB)	>40	68	67.64	68.175	68.423
MOS Area ($x10^{-10}$ m^2)	**<3**	**2.96**	**0.65**	**0.767**	**0.788**

V. CONCLUSION

In this work, particular specifications for a specified topology of a differential amplifier are aimed to be met by adjusting design variables such as device sizes and bias currents by DE, HS and ABC methods. Design equations are utilized for cost function of EA methods, considering that numerous conflicting design criteria are of concern. Resulting design variables are utilized for redesign in SPICE simulator in order to validate the exact values of design specifications obtained with EA methods. Simulation results proved that DE, HS and ABC based design not only meets all design specifications but also minimizes total MOS area with respect to the previous methods. While minimum occupied MOS transistor area is obtained with HS. DE is superior in computation time and also improved ICMR and cut-off frequency with respect to others. ABC provides better performances in terms of gain and power dissipation than other EA methods. As further work, these methods would be investigated in mixed signal circuit optimization.

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