A Built in Self Test System for Dynamic Performance Parameter Evaluation of Pipelined Analog to Digital Converter

Alok Barua and Dhanunjay Nalla

Abstract — This paper presents a built-in-self-test (BIST) system to evaluate dynamic parameters of Pipelined Analog to Digital converters (ADC). A stimulus generation scheme with low harmonic content is also reported here. To generate an On-Chip ac signal a filter based approach has been presented. A square wave with variable frequency is applied to the second order low pass filter through a wave shaping circuit which makes the square wave into a harmonic free digital sine wave. The filter is implemented with an Operational Trans-conductance Amplifier-Capacitive filter with On-Chip automatic tuning facility which has less area overhead and variable (programmable) cut-off frequency to introduce higher reliability in the testing circuit. With the help of this BIST system some of the most commonly occurred faults were simulated, and their effect on dynamic performance parameters has been studied. The layout of the entire system is prepared. The area occupied by the total system is 0.1666mm^2. The system is designed in 180nm CMOS technology with 1P4M TSMC process.

***Index Terms* — ADC, automatic tuning, dynamic testing, faults, OTA-C filter.**

I. Introduction

Analog to digital converter (ADC) is a very important component of mixed signal circuits. Design of high performance ADCs is a hot research topic today. Efforts are being made to develop new ADC designs which will ensure high sampling speed, high accuracy and also low power. Hence new test algorithms should also be developed to test the high performance ADCs. A BIST system is being developed for these high performance ADCs with different architectures. The testing of ADCs can be classified as static testing and dynamic testing. Through static testing one can measures these parameters such as Offset error, Gain error, DNL, INL, Missing Code Error, and Monotonicity Errors [1]-[4]. Dynamic testing is used for measurement of Signal to Noise Ratio (SNR), Total Harmonic Distortion (THD), Spurious free Dynamic Range (SFDR), Effective number of bits, and Signal to Noise plus Distortion Ratio (SINAD)[4]-[6]. To generate the test stimulus an oscillator circuit can be used [7]. The Operational Transconductance Amplifier and Capacitor (OTA-C) filter is very much useful in On-Chip applications because of its small area overhead and it can be used as programmable cut-off frequency filter with the use of automatic tuning [8]-[10].

In this paper a BIST system has been designed for the dynamic testing of a 1.8V 8-bit 100MSPS Pipelined ADC. In this test scheme a 1V peak to peak signal with the frequency range of 1 KHz to 1MHz has applied to the ADC under the test. The output of the ADC is reconstructed by using a DAC algorithm. A 1024 point Fast Fourier Transform (FFT) has applied to the reconstructed signal to analyze the dynamic performance parameter as mentioned earlier.

Some of the most common faults in the pipelined ADC were created, and their effect on the dynamic performance parameters has been studied.

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II. Basic Built In Self Test Structure

Analog test stimulus generation for BIST applications continue to be a hot topic in the test research community, and a number of different strategies for analog signal generation have been published for the last couple of years. Fig. 1 shows the typical bloc k diagram of the BIST circuit, which is entirely monolithic on the same chip of the main circuit for which one want to test or measure the performance, and hence it allows high-speed testing with reduced need for external test equipment, test development time and effort, along with reduced manufacture test time and cost.

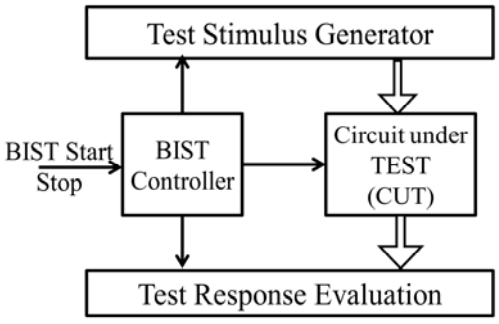

Fig. 1: Basic BIST architecture

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A. Principle of On-Chip Signal Generation

A classical solution for the generation of sine wave signals is the closed-loop oscillator [11], which consists of a filtering section with a non-linear feedback mechanism in the arrangement shown in Fig. 2a. The quality of the generated signal depends on the linearity and selectivity of the filter and the shape of the non-linear function. Highly selective filters and smooth non-linear functions are needed for the generation of high-accuracy, low distorted waveforms.

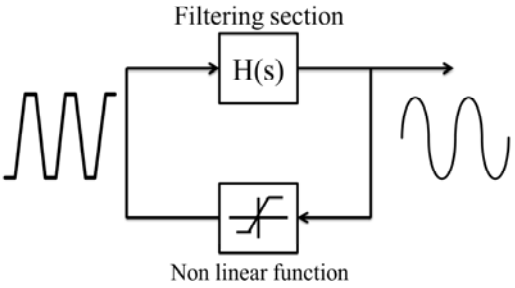

Fig. 2.a: Typical closed-loop signal generator

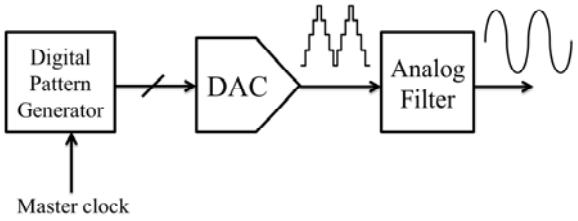

Fig. 2.b: Typical open-loop signal generator

Most of the proposed strategies for on-chip generation of test signals adopt the open-loop scheme in Fig. 2b. These waveform generators are usually based on a digital pattern generator followed by a D/A conversion [11]. The digital pattern generator outputs a digital sequence, the D/A converter translates the digital pattern to the analog domain, and finally the signal is fed to an analog filter that attenuates all the non-desired components in the output signal. It has the advantages of a digital interface for control and programming tasks, and it also offers the characteristics of robustness which is common to the digital circuitry.

It is observed that in closed loop oscillator the frequency and amplitude of output depends upon the filter time constant and its gain, moreover only band pass filter is suitable for this kind of oscillators. On the other hand in open loop oscillators, low pass filter is sufficient with lower order. One key important factor for BIST applications is the area overhead hence the filter order is limited, and the area occupied by the digital pattern generator and DAC should be as least as possible. To reduce the area overhead on silicon a new digital pattern generator is proposed which can generate digitized sine wave without using the DAC.

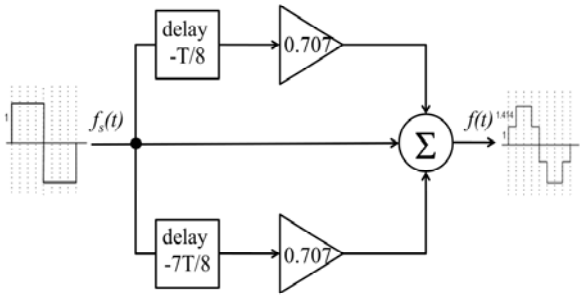

Fig. 3.a: Implementation of a four-level square wave generator

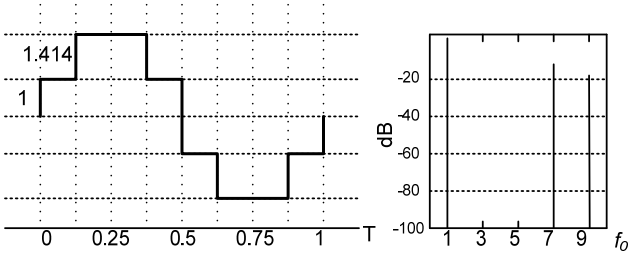

Fig. 3.b: Frequency response of a four-level square wave generator

The proposed digital pattern generator uses simple delay element and an amplifier as shown in Fig. 3a. [12]. By properly adjusting the delay from the delay element and gain of the amplifier the harmonic contents in the square wave are made to vanish except *8n ±1* harmonics which are far away from the cut off frequency of the filter, as shown in Fig. 3b. The delay is incorporated by a D Flip-Flop and an amplifier is by a source follower which does not consume much area on silicon.

The main filter is first implemented by an active RC filter [10]. For a filter with cut-off frequency of 1 KHz requires a high value of resistances and capacitances. In the CMOS technology the value of resistance/capacitance is directly proportional to the area occupied by it, so the filter topology has to be changed. A solution for this problem is that the resistances can be replaced by a combination of switches and a capacitor. So the topology is now changed into a switched capacitor filter where the time constant/cut-off frequency can be set by a ratio of capacitors. This is an added advantage of CMOS technology, and the switch can be implemented by a CMOS pass transistor, and is controlled by a clock pulse. Switched capacitor state variable filter with second order was implemented with less area [10], but later it was found that switched capacitor filter is introducing distortions in the output due to its operation was phase wise, i.e. it operates as sampler and stays at the same potential in one phase and as amplifier in next phase. This phenomenon is causing degradation of the SNR/SNDR of the signal.

To overcome these problems the remaining choice is the use of trans- conductance amplifier and capacitive filters which are implemented by simple transconductance amplifiers (voltage to current converters) and capacitors [13], [14].

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III. OTA-C Filter

The transconductance of the OTA can be adjusted by using the bias current through the input differential stage; hence there is a possibility of On-Chip tuning. These types of filters, can be operated in open loop conditions [13], has very high operating ranges (0.1 Hz to 10GHz) with very low area overhead, but have very low range of linearity and prone to parasitic effects. Parasitic effects can be reduces by using the On-Chip tuning, and the linearity can be enhances by using one/more of the following techniques [15].

- ❖ Source degeneration
- ❖ Current division
- ❖ Using floating gate transistors
- ❖ Bulk driven trans-conductance amplifiers

The bulk driven OTAs are much advantageous in low voltage application but are limited by their small transconductance. Therefore in this case to improve the linearity of the OTA, source degeneration technique was used. The performance of OTA-C filters depends on: (i) the OTA circuit, which is the main noise and distortion contributor in the filter, and (ii) the OTA-C filter structure. The later one is a second order Butterworth, realized by biquad and is implemented with four OTAs and four capacitors. The fully-differential trans-conductor capacitor filter is shown in Fig. 4. All transconductors are identical. The distortion introduced by the OTA depends upon the linearity of that OTA; hence good design of OTA ensures the better performance.

The differential transconductance circuit is shown in Fig. 5. It comprises a source-coupled pair with poly-silicon degeneration resistors and a cross-coupled high-impedance load. The linearity is enhanced by the degenerated resistors [13]. Transistors M_4, M_5, M_6 and M_7 are matched. M_8 and M_9 operate in the triode region, acting as degeneration resistors to provide different operating points at nodes v_p and v_n. M_4 and M_7 act like a pair of positive resistors R_+, while M_5 and M_6 function as negative resistors R_-.

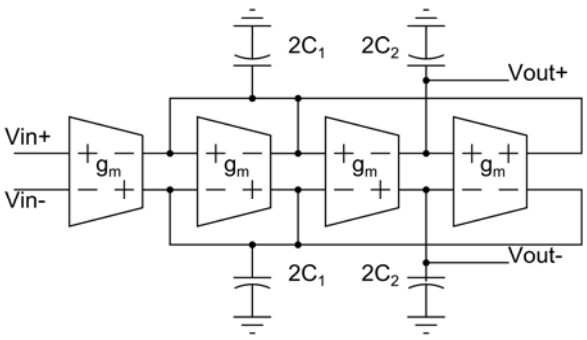

Fig. 4: OTA-C 2nd order Butter-worth low pass filter

The output impedance of the transconductor depends on the parallel combination of R_+ and R_-. The values of these resistors can be controlled by voltages v_{cp} and v_{cn} respectively. As a result, the output impedance, and therefore, the Q (Quality factor) of the integrator, can be maximized with proper combinations of v_{cp} and v_{cn}. With this transconductor, a tunable integrator for very-high-frequency integrated filters can be realized by adjusting the voltage v_{ba}, which controls the tail current, and thus, G_m. Good high-speed properties can be achieved from the absence of internal high impedance nodes, which pushes non-dominant poles to the gigahertz range.

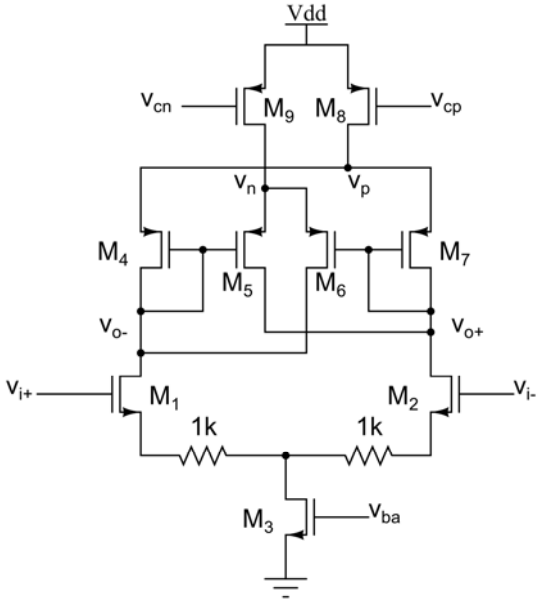

Fig. 5: Fully differential CMOS implementation of OTA [13]

IV. On-Chip Automatic Tuning

As mentioned earlier, the advantage of the OTA-C filters is the facility of On-Chip tuning [9]-[10], which can adjusts the cut-off frequency of the filter without varying the physical dimensions of the elements. Here the On-Chip tuning procedure uses the concept of PLL (Phase Locked Loops) where the cut-off frequency of the filter can be adjusted by an external clock pulse or reference clock. Instead of using conventional tuning method which requires a master filter and slave filter where the master is used for the tuning and slave is for filtering, a digital tuning procedure has presented to help in very accurate tuning. Digital tuning method is not only accurate but also has less area overhead (absence of slave filter) and the master filter is switched between the circuit and tuning loop through the use of an Analog Multiplexers.

The total control circuit is shown in Fig. 6. Due to the digital control of the tuning loops, only one loop is active at a given time interval, which eliminates the need for a slow tuning loop. And it improves stability and reduces tuning time. The cut-off frequency of the filter is set to match the reference frequency with the help of PLL. Phase-frequency detector (PFD) and charge pump (CP) circuits are designed with a conventional structure. The VCO is accomplished by the cascade connection of four fully differential OTAs, which can provide a phase shift of 45° per stage. Tuning can be controlled from the comparison of phase response[9] of the filter with $V_{45°}$ and $V_{135°}$ which are directly generated from the VCO and are 45° and 135° delayed signals respectively with respect to V_0.The tuning circuit is realized by simple digital logic as shown in Fig. 7, which requires D Flip-Flops, AND logic and up-down ramp generators. The up-down ramp

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generators allow the tuning process to operate more stable, and also it requires very small area overhead.

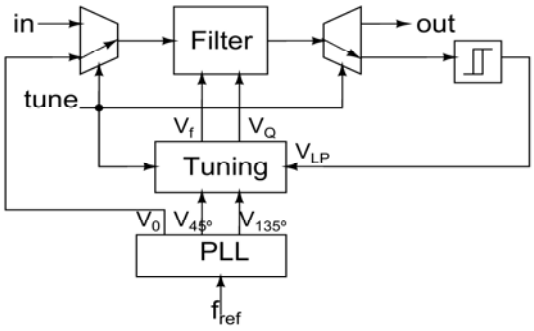

Fig. 6: Total control circuit for automatic tuning [9]

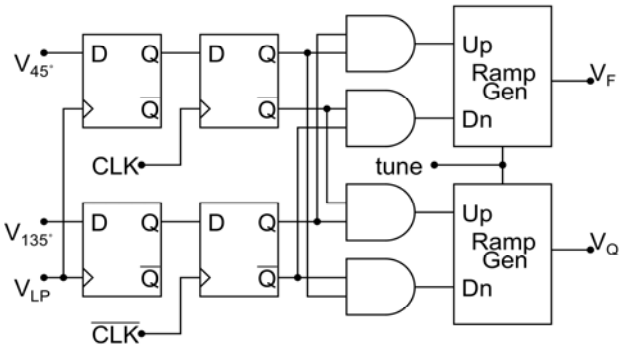

Fig. 7: Tuning Circuit [9]

V. The Circuit Under Test (CUT)

A pipelined A/D converter is inherently a multi-step amplitude quantizer in which the digitization is performed by a cascade of many topologically similar or identical stages of low-resolution analog-to-digital encoders [16]-[18]. Pipelining enables high conversion throughput by inserting analog registers, i.e., sample-and-hold amplifiers (SHAs), in between stages that allow a concurrent operation of all stages. This is done at the cost of an increased latency. An 8-bit pipelined ADC has been designed, whose block diagram is shown in Fig.8 and has been utilised as the CUT in the BIST system. Pipelined ADCs provide an optimum balance of size, speed, resolution, power dissipation, and analog design effort, they have become increasingly attractive to major data-converter manufacturers and their designers. The pipelined ADC is the architecture of choice for sampling rates from a few Msps up to 100Msps+. Design complexity increases only linearly (not exponentially) with the number of bits, thus providing converters with high speed, high resolution, and low power at the same time. Pipelined ADCs are very useful for a wide range of applications, most notably in digital communication where a converter's dynamic performance is often more important than traditional DC specifications like differential nonlinearity and integral nonlinearity.

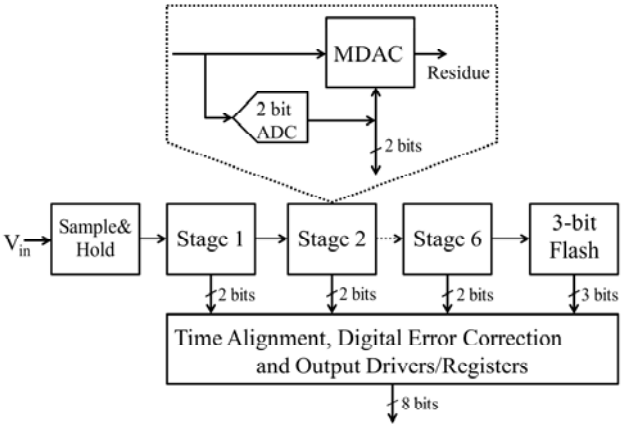

Fig.8: Block diagram of the circuit under test (pipelined ADC)

VI. Dynamic Parameter Evaluation

The signal obtained from the OTA-C filter has a better THD of 0.0037%, which is more than sufficient to test the pipelined ADC. Now this signal is fed to the Pipelined ADC which generates an 8-bit digital code for corresponding input. The code obtained from the ADC is passed through an algorithm to reconstruct the digital code, and a 1024-point FFT has been calculated from the reconstructed signal. The dynamic performance parameters have been evaluated from the spectrum thus obtained [19].

The Dynamic performance parameters were calculated from the 1024 point FFT plot/Data at different frequencies of input signal in the range of 1KHz – 1MHz for the healthy ADC are shown in Table I below.

TABLE I
Dynamic Parameters of the ADC

Parameter	At 1 KHz	At 10KHz	At 100KHz	At 1MHz
SNR (dB)	53.3379	53.0932	49.8055	46.3169
SINAD (dB)	50.7227	50.3843	48.3569	44.2613
SFDR (dB)	55.4103	55.4178	56.8276	48.4972
THD (dB)	53.3282	53.4138	53.8292	48.4972
ENOB	8.0669	8.0435	7.7403	7.3989

VII. Fault Analysis Using BIST System

The linearity of a pipelined analog-to-digital converter (ADC) is primarily degraded by the linearity errors in its pipeline stages. In a switched-capacitor circuit implementation, the primary sources of linearity errors are: 1) the gain errors in the residue amplifier, due to the finite gain and dynamic effects of its operational amplifier; and 2) the nonlinearity in the digital-to-analog sub-converter (sub-DAC), due to capacitor-mismatch errors. Compared to gain errors, capacitor-mismatch errors have a significantly more degrading effect on the overall linearity of the pipeline stage [20]-[21]. The offset error in the sub ADC is also the common error, but its effect will be nullified by employing the digital correction. At most 25% of the full scale range offset error can also be possible to eliminate with digital correction.

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The above stated faults were created in the system in order to evaluate their effect on the system. The offset error was introduced by putting a DC voltage source of 50mv magnitude (5% of FS) at the negative input terminal of the dynamic comparator. To introduce capacitor mismatching, the capacitor values are changed such that these values differ from the actual healthy system with 4.8% and -5.7% i.e. one capacitance value is reduced by 23*fF* (femto Farads) and other one is increased by 27*fF* from the actual value of 473*fF*. The values are changed in opposite direction to simulate the worst case changes. The gain of the OTA which is used in ADC stages for multiplying and digital to analog conversion operation has decreased from 63 dB to 51 dB to create the gain error [22] - [23], since with changes in supply voltage and temperatures the gain can easily be degrades in submicron technologies. The offset error for the OTA has been created by again a dc source of 50mv magnitude. These four types of faults were created and simulated individually to study their individual behaviour on the system. The effects of the capacitor mismatch error and gain error of the OTA on the dynamic performance parameters of the ADC have been evaluated. The dynamic parameters are obtained from the FFT plots, and are shown in Table II.

Table II: Dynamic performance parameters for various faults

Parameter	*Capacitor mismatch error*	*Gain error of OTA*	*Offset error of OTA*	*Offset error*
SNR (dB)	35.5281	35.5399	29.2337	46.3169
SINAD (dB)	35.6356	35.6356	29.3410	44.2613
SFDR (dB)	1.0937	4.0729	1.3945	48.4972
THD (dB)	19.5174	19.0180	13.2130	48.4972
ENOB	5.6272	5.6272	4.5816	7.3989

VIII. Preparation of Layout and Post Layout Simulation

The layout for the entire BIST system has been prepared by utilizing four metal layers and a poly silicon layers in CMOS9T standard 180*nm* technology process. While preparing the layout each transistor has been prepared from the fundamentals by making all individual layers instead of using the templates of the transistors which are designed for particular technology such that the area occupied by the system is optimized, and all the lengths, widths and spacing between alike layers are maintained as the minimum dimensions allowed by the technology. As by maintaining the minimum dimensions the parasitic resistances and capacitances will also reduces and hence better performance will be assured.

The total chip including BIST and CUT have area of $534\mu m$ X $312\mu m$ = $0.1666mm^2$, where as the circuit under test (CUT) i.e. the pipelined ADC is occupying $454\mu m$ X $280\mu m$ = $0.1271mm^2$. The layout is shown in Fig. 9. The testing circuit and the CUT are occupying 23.7% and 76.3% of the total area respectively. The testing circuit consist of the stimulus generator and analog multiplexers and required clock generation to operate the multiplexers for switching between actual running mode and testing mode. The output response analyser (ORA) has not designed, because of its area overhead, and the spectre simulator was used as the ORA. After preparing the layout the post layout simulations are also done to verify its functionality once again, from the post layout simulations it is observed that because of parasitic elements, there is a slight variations in the functionality of the system. The post layout simulation for the pipelined ADC has been done and the output code through a 10-bit resolution DAC is found to be satisfactory.

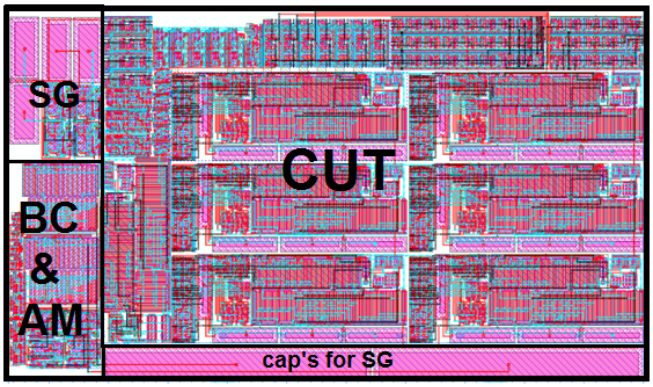

Fig. 9: Layout for the total BIST system

IX. Conclusions

In this paper a built in self test system for measuring dynamic performance parameters of the pipelined ADC is reported. A stimulus generation scheme with low harmonic content (THD = 0.0037%) for BIST system to evaluate dynamic parameters of 1.8V 100MSPS Pipelined ADC has also been presented. The work was done in CADENCE environment of 180nm CMOS technology. An On-Chip signal generation procedure is presented through the use of On-Chip automatic tunable operational transconductance-capacitive, second order Butterworth filter with less area overhead, and with low power (1076µW including tuning-circuit). Some most common faults in the system were created and successfully tested by using the BIST system. Finally the layout for the whole BIST system has been prepared in TSMC 1P4M CMOS process, and the post layout simulations are also has been performed. The total area occupied by the chip is $0.1666mm^2$.

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