

Maximizing the Power Efficiency of Integrated High-Voltage Generators

Jan Doutreloigne

Abstract—This paper describes how the power efficiency of fully integrated Dickson charge pumps in high-voltage IC technologies can be improved considerably by implementing charge recycling techniques, by replacing the normal PN junction diodes by pulse-driven active diodes, and by choosing an appropriate advanced smart power IC technology. A detailed analysis reveals that the combination of these 3 methods more than doubles the power efficiency compared to traditional Dickson charge pump designs.

Index Terms—Charge recycling, Dickson charge pump, high-voltage generator, power efficiency optimization, smart power technology.

I. INTRODUCTION

Fully integrated charge pumps are used in a wide variety of applications, going from flash memories over dedicated display drivers to MEMS actuator drivers. Some applications ask for specific features, such as high current drive capability or a very good output voltage stability, but for all of them a good overall power efficiency is of the utmost importance.

Achieving high power efficiency in fully integrated Dickson charge pumps is not straightforward due to the fact that integrated capacitors exhibit considerable parasitic capacitance to the substrate, resulting in a dramatic efficiency drop. In this paper charge recycling techniques are presented to substantially reduce this negative effect. Replacing the standard PN junction diodes by pulse-driven DMOS transistors acting as almost ideal active diodes is another method to enhance the power efficiency. Finally, the choice of an appropriate smart power IC technology with superior transistor and integrated capacitor performance also helps to boost the efficiency. In this paper, these 3 methods are described and compared.

II. BASIC DICKSON CHARGE PUMP DESIGN

The basic configuration of a Dickson charge pump [1] is shown in Fig. 1. It consists of a large number of identical stages, each containing a diode and a capacitor, where the bottom plates of the capacitors in consecutive stages are driven by 2 complementary clock signals. Charge is

transferred from one capacitor to the next at the rhythm of the clock, yielding an output voltage that can be much higher than the input voltage. In a real application, a feedback control loop is added to the circuit in order to maintain the output voltage very stable and independent of system parameters or load characteristics. This can be achieved by continuously adjusting the clock frequency of the charge pump.

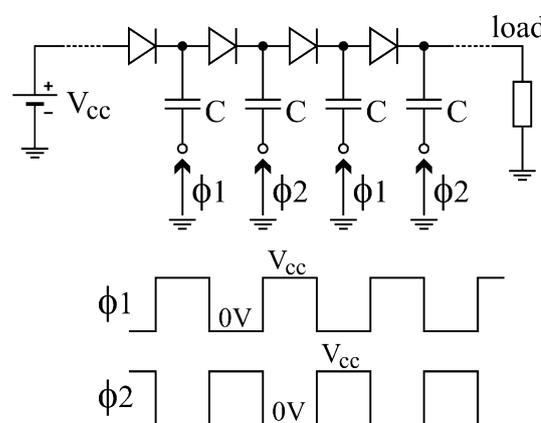


FIG 1. BASIC DICKSON CHARGE PUMP.

A major issue in integrated Dickson charge pumps is the fact that the integrated capacitors exhibit a large parasitic capacitance between their bottom plate and the normally grounded substrate of the chip, as illustrated in Fig. 2:

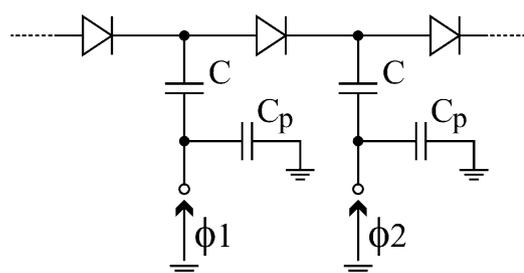


FIG 2. PRESENCE OF PARASITIC CAPACITANCE.

The parasitic capacitance C_p does not contribute to the useful operation of the circuit, but it does affect the power consumption in a negative way. Indeed, the parasitic capacitance C_p is connected directly to the output of the clock buffers, and these buffers have to charge and discharge this parasitic capacitance constantly, resulting in additional power losses inside the transistors of the clock buffers, without having any useful impact on the circuit operation. The consequence is an extremely poor power efficiency of typically 10 to 20% in case of a voltage transformation ratio of 20, even when conventional design strategies for efficiency improvement are applied [2,3,4]. It is obvious that special

Manuscript received June 15, 2014.

Jan Doutreloigne is with the Centre for Microsystems Technology (CMST), affiliated to the Interuniversity Microelectronics Centre (IMEC) and the University of Gent, Technologiepark 914A, 9052 Zwijnaarde, Belgium (phone: +32-(0)9-264-53-56; fax: +32-(0)9-264-53-74; e-mail: jdoutrel@elis.ugent.be).

measures have to be taken in order to boost the efficiency to a more acceptable level. The following 3 sections describe the 3 proposed techniques to achieve this goal.

III. CHARGE RECYCLING

A first approach to mitigate the power losses related to the parasitic capacitance C_p is to employ the dedicated charge recycling technique of Fig. 3:

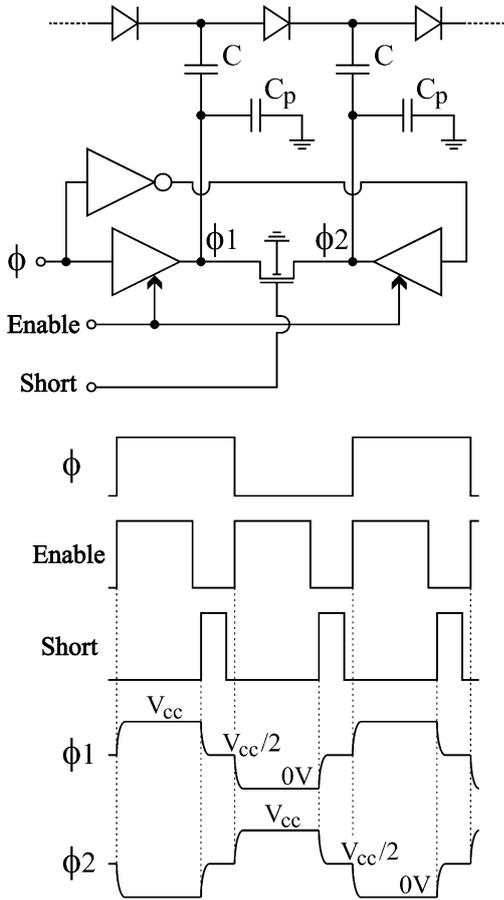


FIG 3. CHARGE RECYCLING PRINCIPLE.

In this configuration, the normal clock buffers are replaced by 3-state buffer circuits. Before switching the clock buffers from one state to the next (from 0V to the supply voltage V_{cc} , or vice versa), their outputs are disabled (high-impedance output) during a very short time interval and the buffer outputs are short-circuited by means of an additional MOSFET. As a result, half of the charge that was stored on the parasitic capacitance C_p of a particular stage will be transferred to the parasitic capacitance of the next stage. Consequently, this parasitic capacitance of the next stage does not have to be charged anymore from 0V to V_{cc} when its clock buffer is again enabled, but only from $V_{cc}/2$ to V_{cc} . This technique yields a 50% reduction of the clock buffer power consumption that is related to the parasitic capacitance in each stage, and hence, it boosts the power efficiency effectively.

IV. PULSE-DRIVEN ACTIVE DIODES

A second approach focusses on the diodes that take care of the correct energy flow in each stage of the Dickson charge

pump. Their threshold voltage V_T (typically 0.5V for a standard PN junction diode) causes additional power losses during the energy transfer from stage to stage, and hence, it negatively impacts the power efficiency. But there is also a combined effect of the threshold voltage V_T of the diodes and the parasitic capacitance C_p of the integrated capacitors. Indeed, a large value of V_T results in a low voltage gain per stage (equal to $V_{cc} - V_T$ under zero-load conditions), meaning that more stages are needed to obtain a predefined output voltage. As a consequence, the total parasitic capacitance to be charged and discharged by the clock buffers increases, and the power efficiency drops. So, trying to reduce the threshold voltage V_T of the diodes also mitigates the effect of the parasitic capacitance, and that is exactly the basis of this second technique.

A first possibility would be to replace the standard PN junction diodes by Schottky diodes that exhibit a much lower threshold voltage. Unfortunately, high-performance Schottky diodes are not readily available in most smart power IC technologies. An interesting alternative is to replace the diodes by properly driven transistors that provide a low-resistance path during the charge transfer between capacitors of consecutive stages. In the ideal situation, the charge transfer can be completed to its full extent during the conduction time of the transistor, meaning that the equivalent V_T value would simply be 0V, resulting in maximum power efficiency! A possible practical implementation of this active diode approach is shown in Fig. 4:

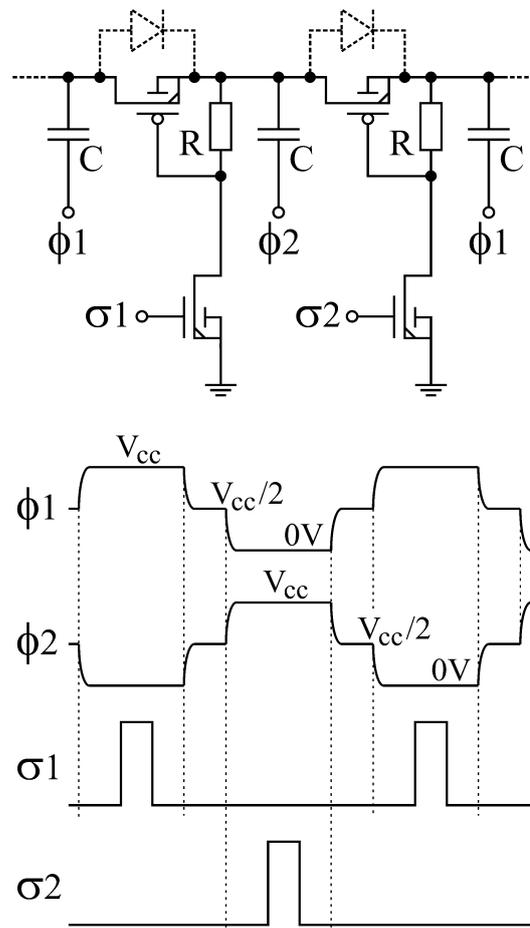


FIG 4. PULSE-DRIVEN ACTIVE DIODES.

The main charge transfer transistors are actually P-type high-voltage DMOS devices, whose built-in drain-bulk diodes are oriented in exactly the same way as the diodes in the original Dickson charge pump. The operation of the circuit is fairly straightforward. When the clock signal $\phi 1$ goes high and $\phi 2$ goes low, there will be some charge transfer from the $\phi 1$ -driven capacitor to the $\phi 2$ -driven capacitor through the built-in drain-bulk diode of the P-type DMOS transistor between them, but this charge transfer will not be complete due to the threshold voltage of the diode. But then the pulse $\sigma 1$ is applied to the gate of an auxiliary N-type DMOS device, being the driving transistor in a level-shifter circuit, producing a voltage drop of a few volts across resistor R , thereby activating the P-type DMOS transistor. Hence, the low-resistance channel of this device causes the charge transfer to continue until the top plates of the 2 capacitors reach exactly the same electric potential. This corresponds to the ideal situation of $V_T = 0V$, meaning that the P-type DMOS transistors act like almost ideal active diodes. The effect of this technique is clearly illustrated in the simulation result of Fig. 5, where V_{cap1} and V_{cap2} are the electric potentials of the capacitor top plates in consecutive stages. The reduction of the 0.5V voltage drop (the V_T of the built-in drain-bulk diode) to 0V when the P-type DMOS device is activated by the $\sigma 1$ pulse is very clear in this simulation. Also note the previously described charge recycling in the clock signals.

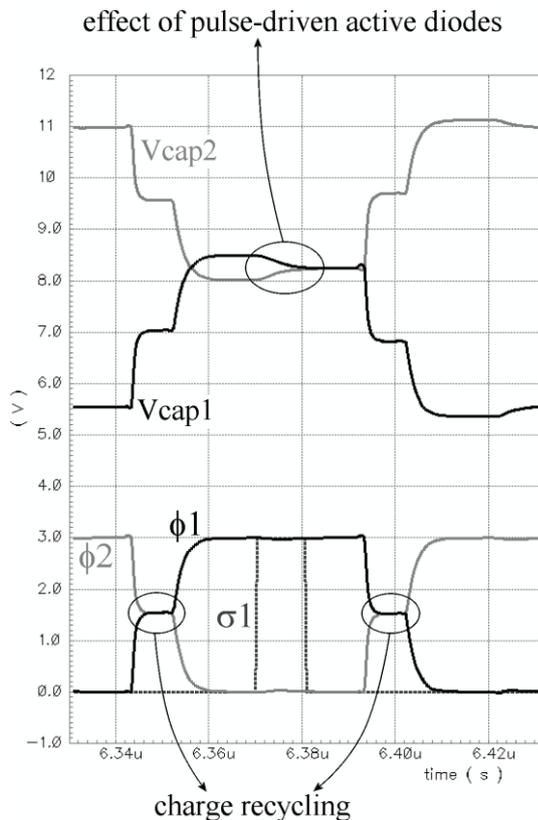


FIG 5. SIMULATION OF THE PULSE-DRIVEN ACTIVE DIODES.

Although this technique looks very simple and attractive, the practical implementation and the correct component dimensioning are not straightforward at all and require a careful optimization process.

V. PROPER IC TECHNOLOGY CHOICE

The third method to increase the power efficiency deals with a proper choice of IC technology. Of course, the specified maximum output voltage of the Dickson charge pump will set a lower limit for the high-voltage handling capability of the smart power IC technology, but also the performance of the integrated capacitors and transistors are very important selection criteria. Indeed, competitive technologies with similar voltage ratings may offer different capacitor structures with completely different values of the parasitic capacitance, resulting in significantly different power efficiency levels. Also the specific performance (on-state resistance as well as parasitic capacitance) of the P-type and N-type high-voltage DMOS transistors in the pulse-driven active diode circuit of Fig. 4 will largely affect the overall power efficiency.

To illustrate the importance of the capacitor structure, we'll consider the example of the 100V 0.7 μ m I²T technology (Intelligent Interface Technology) of ON Semiconductor. Figs. 6 to 8 show a vertical cross section of 3 different kinds of integrated capacitors in this technology. Fig. 6 depicts a capacitor between a poly-silicon layer at the top and a highly doped N⁺ implantation at the bottom, with a very thin dielectric in between. Fig. 7 represents a capacitor structure between 2 poly-silicon layers, with a somewhat thicker dielectric. Finally, Fig. 8 shows a sandwich structure where the shorted poly-silicon and metal2 layers form 2 capacitors in parallel towards the metal1 layer. The dielectric in this structure is considerably thicker than in the 2 previous cases.

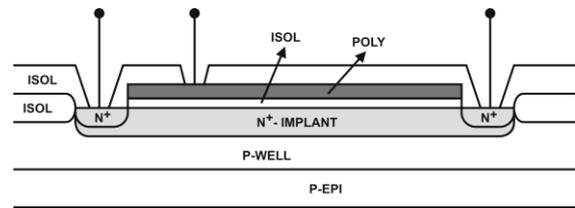


FIG 6. POLY-N⁺ CAPACITOR (PN CAPACITOR).

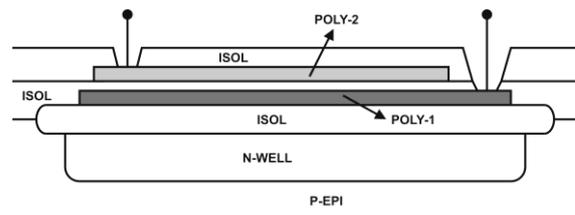


FIG 7. POLY1-POLY2 CAPACITOR (PP CAPACITOR).

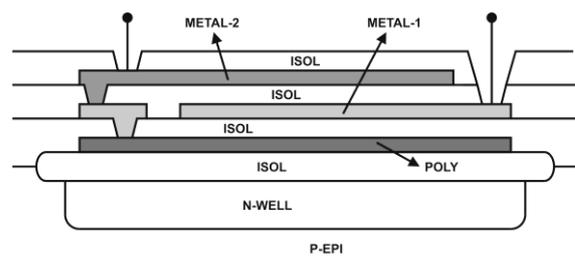


FIG 8. METAL1-METAL2-POLY CAPACITOR (MM CAPACITOR).

Depending on the thickness of the dielectric, these capacitor types have different values of the specific capacitance per unit silicon area and maximum operating voltage, but also the parasitic capacitance towards the substrate behaves differently. These data are gathered in Table I. Apparently, the PN capacitor has the highest specific capacitance per unit silicon area because of the thinnest dielectric, but at the same time also the lowest maximum operating voltage. At the other extreme, the MM capacitor has the highest maximum operating voltage at the expense of the lowest specific capacitance. The PP capacitor is settled somewhere in between. Regarding the percentual parasitic capacitance towards the substrate, the PP capacitor is undoubtedly the best option, and the MM capacitor clearly the worst.

TABLE I. COMPARISON OF DIFFERENT CAPACITOR TYPES IN THE 100V 0.7 μ m I²T TECHNOLOGY.

Capacitor type	Max. voltage (V)	Specific capacitance (fF/ μ m ²)	Parasitic capacitance (fF/ μ m ²)
PN	12	0,75	0,27 (36%)
PP	30	0,345	0,079 (23%)
MM	100	0,091	0,057 (63%)

Based on the information from Table I we can easily select the most appropriate capacitor type for every individual stage in the Dickson charge pump. In the first set of stages, where the capacitor operating voltage is limited to values below 30V, the PP capacitor is selected as it is superior in terms of percentual parasitic capacitance. However, for the last stages with operating voltages in excess of 30V, the MM capacitor is the only option because of the voltage rating. The very bad corresponding percentual parasitic capacitance towards the substrate is then something we have to live with and it means that for charge pumps with an output voltage much higher than 30V, the overall power efficiency will be very low!

For charge pumps with very high output voltages it is therefore advisable to compare several smart power IC technologies and to select the one that offers a type of high-voltage capacitor with the lowest possible percentual parasitic capacitance towards the substrate. Take for instance the 80V I³T technology (Improved Intelligent Interface Technology) of ON Semiconductor, which is much more advanced than the 100V I²T technology as it is based on a 0.35 μ m CMOS core process instead of the older 0.7 μ m process. Due to the fact that this 80V I³T technology allows much smaller metal track widths and spacings as well as 5 metal levels instead of only 2, it becomes possible to integrate multi-metal capacitors with a kind of staggered “finger”-structure design of the 2 electrodes as shown in the schematic view of Fig. 9:

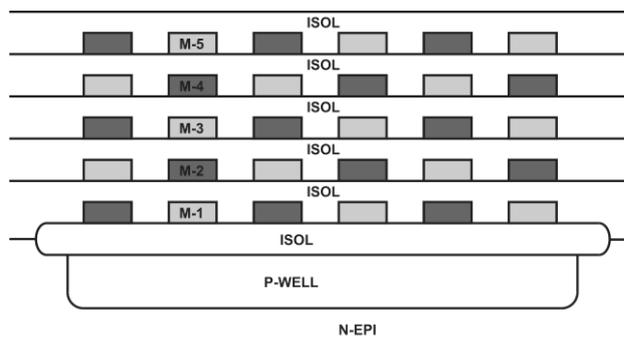


FIG 9. MULTI-METAL CAPACITOR WITH STAGGERED “FINGER”-STRUCTURE DESIGN (MF CAPACITOR).

This type of capacitor design makes optimal use of the horizontal and vertical dimensions (there is capacitance between neighboring metal stripes in horizontal and vertical direction) to get the maximum capacitance for a given amount of silicon area while keeping the parasitic capacitance towards the substrate to a minimum. This is clearly evidenced in Table II, comparing the performance of the metal1-metal2-poly capacitor (MM) in the 100V 0.7 μ m I²T technology and the multi-metal “finger” capacitor (MF) in the 80V 0.35 μ m I³T technology:

TABLE II. COMPARISON OF CAPACITOR PERFORMANCE BETWEEN THE 100V 0.7 μ m I²T AND 80V 0.35 μ m I³T TECHNOLOGIES.

Capacitor + technology type	Max. voltage (V)	Specific capacitance (fF/ μ m ²)	Parasitic capacitance (fF/ μ m ²)
MM 100V 0.7 μ m I ² T	100	0,091	0,057 (63%)
MF 80V 0.35 μ m I ³ T	80	0,32	0,047 (15%)

As could be expected, the high-voltage MF capacitors in the 80V 0.35 μ m I³T technology exhibit a 4 times lower percentual parasitic capacitance than the high-voltage MM capacitors in the 100V 0.7 μ m I²T technology. This makes the 80V 0.35 μ m I³T technology the preferred choice for integrating high-voltage Dickson charge pumps with maximum power efficiency.

When comparing smart power IC technologies, also differences in high-voltage transistor structures and transistor characteristics may be observed. As an example, Table III compares the same 100V 0.7 μ m I²T and 80V 0.35 μ m I³T technologies in terms of specific on-state resistance of the main high-voltage P-type and N-type DMOS transistors. It is clear from this table that the high-voltage DMOS devices in the 80V 0.35 μ m I³T technology have a roughly 3 times lower on-state resistance, which means that the duration of the control pulses σ_1 and σ_2 for activating the level-shifters in the pulse-driven active diode circuit of Fig. 4 can be chosen much shorter than in the case of the 100V 0.7 μ m I²T technology, resulting in less power dissipation inside the level-shifters, and hence, improved overall power efficiency.

TABLE III. COMPARISON OF HIGH-VOLTAGE TRANSISTOR PERFORMANCE BETWEEN THE 100V 0.7 μ m I²T AND 80V 0.35 μ m I³T TECHNOLOGIES.

Technology	Transistor type	Max. voltage (V)	Specific on-state resistance (Ω mm ²)
100V 0.7 μ m I ² T	N-type DMOS	100	0,76
	P-type DMOS	90	1,32
80V 0.35 μ m I ³ T	N-type DMOS	80	0,26
	P-type DMOS	80	0,47

From the discussions of Tables II and III we conclude that a careful comparison and selection of smart power IC technologies is of the utmost importance to achieve the maximum power efficiency in integrated high-voltage Dickson charge pumps!

VI. IMPACT OF THE 3 PROPOSED TECHNIQUES

To illustrate the effect of the 3 techniques we proposed for boosting the power efficiency of integrated high-voltage Dickson charge pumps, a comparison is made for 1 specific application: a monolithic driver chip for a 60V bistable nematic Liquid Crystal Display (LCD). For that purpose an integrated Dickson charge pump is needed, capable of transforming a 3V supply voltage into a 60V output voltage with a maximum output current rating of 200 μ A. In every design (i.e. for each implementation of the proposed techniques), a clock frequency of 10MHz and a capacitor of 12pF in each stage of the charge pump were assumed, and the number of stages was chosen in such a way that the specified 60V output voltage was within reach for the maximum output current value of 200 μ A. The results of this comparative study can be observed in Fig. 10, showing the power efficiency as a function of the output current for several design cases.

From this graph, the importance of the proposed efficiency boosting techniques becomes very clear. Combining the charge recycling feature, the pulse-driven active diode technique and the use of an advanced smart power technology with enhanced high-voltage capacitor and transistor performance more than doubles the power efficiency compared to the traditional Dickson charge pump configuration (no charge recycling, standard PN junction diodes and the use of an older IC technology with less performing high-voltage capacitors and transistors), and this over the whole useful output current range. It is in fact quite remarkable that a power efficiency of almost 50% can be reached at the optimal operating point for this very high voltage transformation ratio from 3V to 60V in a fully integrated high-voltage generator!

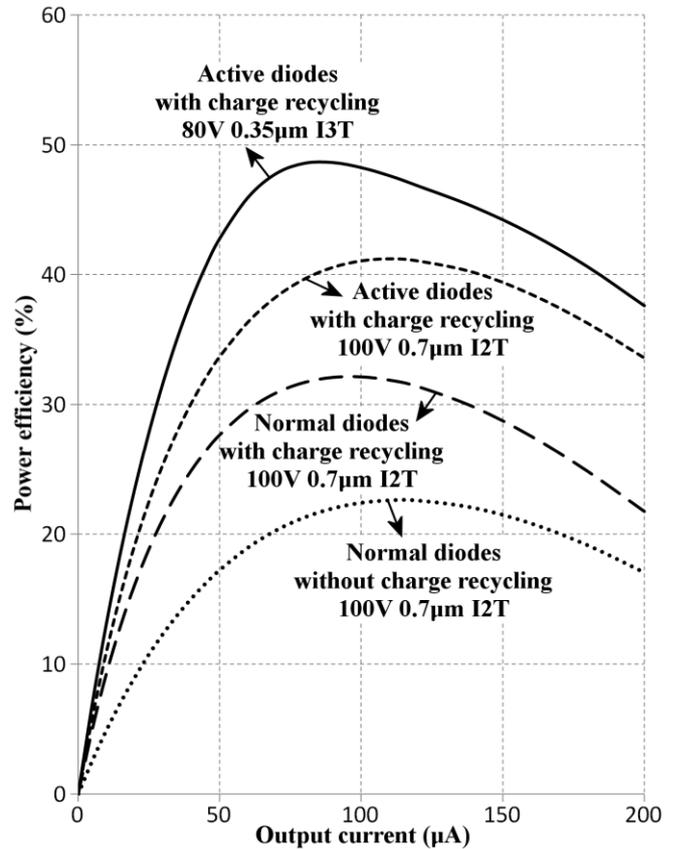


FIG 10. IMPACT OF THE 3 PROPOSED TECHNIQUES ON THE POWER EFFICIENCY VERSUS OUTPUT CURRENT CHARACTERISTIC.

VII. CONCLUSION

Three methods for increasing the power efficiency of fully integrated Dickson charge pumps were presented and analyzed in this paper: the use of charge recycling techniques, the replacement of standard PN junction diodes by pulse-driven active diodes, and the use of an advanced smart power IC technology with high-performance integrated high-voltage capacitors and transistors. Data from specific design cases provide a clear proof of the positive impact of these 3 methods. It was shown that the power efficiency is more than doubled compared to traditional Dickson charge pump configurations.

REFERENCES

- [1] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE Journal of Solid-State Circuits*, Vol. 11, No. 3, 1976, pp. 374-378.
- [2] G. Di Cataldo, and G. Palumbo, "Design of an n-th order Dickson voltage multiplier," *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications*, Vol. 43, No. 5, 1996, pp. 414-417.
- [3] G. Palumbo, D. Pappalardo, and M. Giabotti, "Charge-pump circuits: power-consumption optimization," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. 49, No. 11, 2002, pp. 1535-1542.
- [4] G. Palumbo, D. Pappalardo, and M. Giabotti, "Modeling and minimization of power consumption in charge pump circuits," *Proc. of the 2001 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2001, pp. 402-405.