Switch Box Configuration for Generic Embryonic Cells Routing

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***Abstract*—A generic embryonic fabric comprised of switch boxes to route signals between the cells is designed. The generic fabric can implement combinational as well as sequential design by selection. In earlier proposed structure of embryonic fabric the routing was directly between the cells in the fabric and thus was not flexible for new design. The switch box concept provide the fabric flexibility when adopting to new design. The proposed configuration of switch box has five directional buses for routing. It has four directed buses to route the signals with other cells within the fabric. The communication between the switch box and its associated cell is through a separate five bit dedicated bus. An 4-bit adder and a 4-bit counter is implemented on the generic fabric routed via switch boxes.**

***Index Terms*—Bio-inspired systems, embryonics, embryonic fabric, generic embryonic cell, switch box**

I. Introduction

EMBRYONIC is a bio-inspired computing architecture inspired from the multi-cellular organism development process. The cellular organism development process can be applied to digital integrated circuits on silicon [1]. This will enable to import the properties of living world like self-repair and self-replication to digital domain [2]. To achieve fault tolerant digital circuit self-repair and self-replication properties can be useful. Self-repair does partial reconstruction required in case of minor fault in the circuit, while self-replication does complete reconstruction in case of major fault in the design. The main feature of cellular division and cellular differentiation of biological systems got implemented in a novel embryonic fabric. The implementation of combinational and sequential logic independently on this embryonic fabric is already demonstrated [3][4].

The fabric got tested for regular structures of adder, multiplier and counter. The routing between the cells were through the fabric. In this paper the routing is performed using a separate module called switch box and also a generic embryonic structure is proposed. The generic structure is capable of implementing combinational as well as sequential logic based on mux selection. The mux select data and the routing data can be part of configuration data, in that case the data will be different for different cells. The cloning of configuration data needs that the data loaded is same for all the cells. In the proposed structure the configuration data contains clone number and LUT data and remain same for all cells for regular structure. The cellular differentiation if implemented, the mux select and the routing data then can be part of genome data.

Section 2 is about the generic embryonic fabric and implementation of 4-bit adder and 4-bit counter on it. The fabric includes switch boxes for routing the signals between the cells. Section 3 describes adder details, the switch box topology adopted and look up table (LUT) for it. The switch box for adder is having only forward direction routing. Section 4 describes counter details, the switch box topology adopted and LUT for it. The switch box for counter has both forward and backward routing directions. Section 5 shows the simulation results for designs implemented using verilog. A brief conclusion summarizes all the results and future scope.

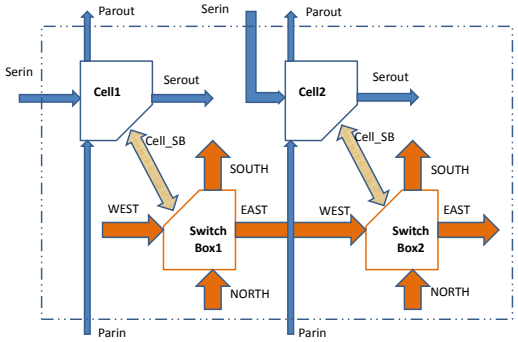

Fig. 1. Structure of generic fabric with two cells and two switch boxes

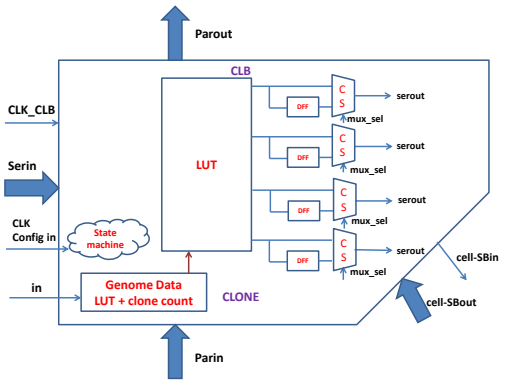

Fig. 2. Generic cell design

II. Design of Generic Embryonic Fabric

An embryonic fabric for implementing a digital design using cloning method is proposed. The cloning is tested for regular circuit structure of adder and counter. The cellular

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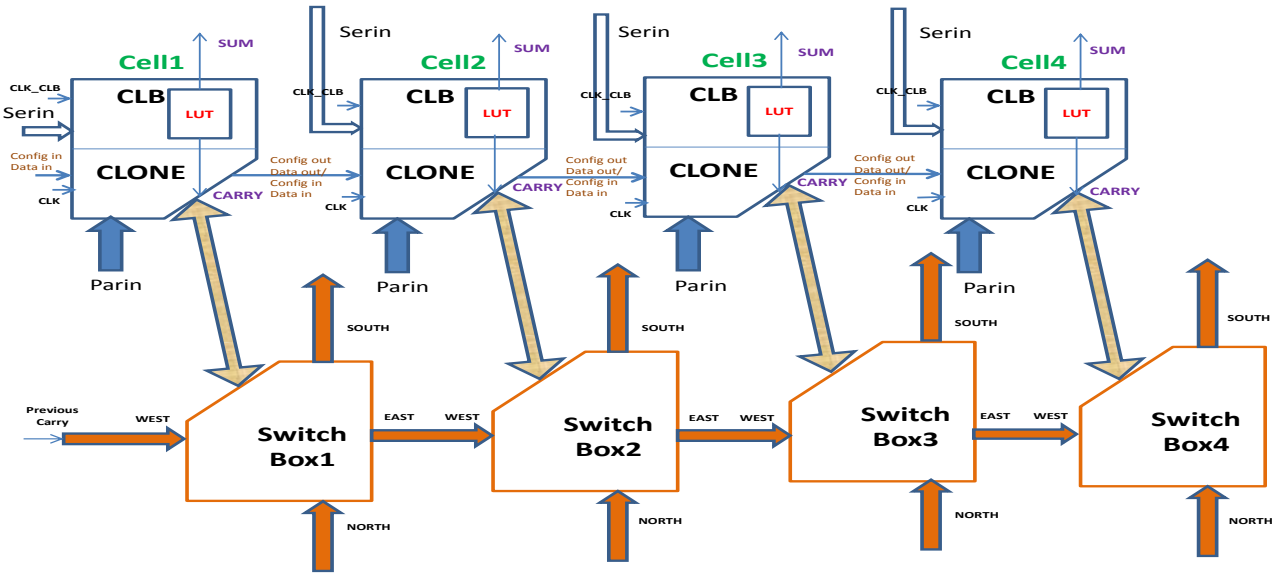

Fig. 3. 4-bit adder implementation on generic fabric

differentiation integrated to it can make it possible to design irregular structure too. The generic structure for 4-bit adder and 4-bit counter is proposed. These circuits in earlier work were implemented without switch box for routing.The generic fabric with two cells and two switch boxes is shown in Fig. 1.

Each cell is having serial input, parallel input from outside of fabric. Parallel output is to outside of fabric. Each cell has one associated switch box below to it. The configuration of generic cell is shown in Fig. 2. The cell has genome data loaded by data-in through state machine. The data configures each cell with same LUT data and number of cloned cells are decided by clone count. The clone count is part of genome data. The mux selection is C/S for combinational and sequential logic.

Each switch box is having five routing directions. The architecture in paper [5] is about optimization of routing resources for connections between cells. The cell to switch box connections and the switch box bus width is decided based on it and to our application.

III. Adder Implementation

Fig. 3 shows 4-bit adder implementation on the generic fabric. It needs four cells and four associated switch boxes. Each cell has serial and parallel inputs/outputs. The switch box has five bus directions, out of them south, north, east and west are for communicating with other cells. The fifth bus is between the switch box and its associated cell. The adder LUT is implemented in the cell's Configurable Logic Block(CLB).

The addition is performed on two parallel input bits with any previous carry if there. The previous carry for first cell is from west bus of switch box. The sum output is placed at parallel output while the carry has to propagate to next cell via east bus of switch box. Within the cell the mux selection is set for combinational logic. Each cell has serial outputs as carry (not clocked).

The LUT inputs can be cell's serial input/parallel input or signals coming through switch box. The bus between cell and switch box is called as cell-SB. The carry has to be propagated through this bus. The first cell's previous carry from west bus is also mapped to cell-SB.

The clone module of the fabric loads genome data to all the cells with clock (CLK). The cloning process enables to create multicellular fabric. The growth process as a part of fabric structural configuration mechanism is discussed in [6]. In this fabric the growth is done only in east direction. The genome data contains LUT data and clone count. Once genome data is loaded the cell output is available as per the mux selection (for combinational and sequential) and clk-clb (for sequential). The final sum is available at parallel output of cells and final carry is avavailable at the east bus of last switch box.

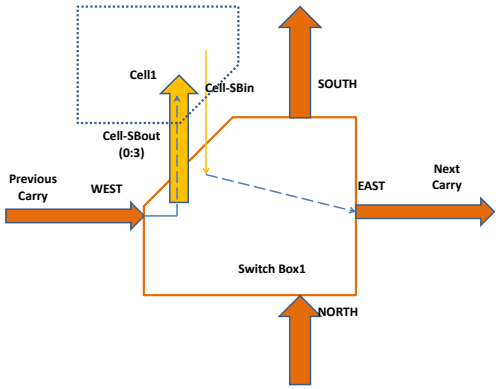

Fig. 4. Configuration of adder switch box

A. Configuration of Adder Switch Box

The switch box has four directional buses. The width of each of data bus is three.The diagonal bus cell-SB has the width of five, out of it one is input (cell-SBin) is to switch

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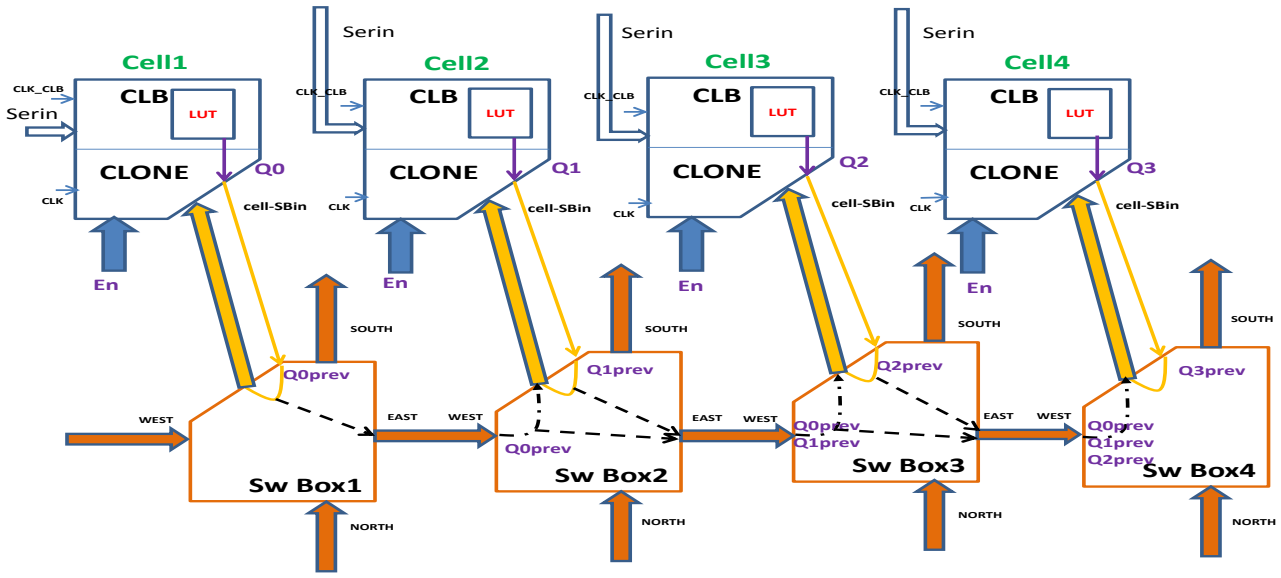

Fig. 6. 4-bit counter implementation on generic fabric; switch box routing depicted

Cell-SBout(0) Previous Carry	Parin(1)	Parin(0)	Parout Sum	Cell-SBin Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig. 5. Adder Look Up Table

box and four are outputs (cell-SBout) from the switch box. The four outputs from switch box can be taken as one of input to cell LUT. This will be additional LUT input other than serial and parallel inputs.

The configuration of switch box is shown in Fig.4. There are two defined operations of adder switch box-

- West bus data transfer to cell-SBout output
- Cell-SBin data transfer to east bus

The east bus of previous switch box is connected to west bus of next switch box in the fabric.

B. Adder Look Up Table

In adder fabric each cell is loaded with same configuration data of 1-bit adder with carry. The LUT has inputs as parin(0), parin(1) and cell-SB(0). The cell-SB(0) is lowest bit of cell-SBout array. The LUT is shown in Fig. 5. The sum is addition of two parallel inputs (parin(0) and parin(1)) and previous carry (through west bus cell-SB(0)). The carry output is assigned to serial output of cell. This serial output is mapped to cell-SBin (input to switch box). The next carry is assigned to east bus.

IV. Counter Implementation

Fig. 6 shows the 4-bit counter implementation in generic fabric. It needs four cells and four associated switch boxes. Counter need one parallel input as enable (En) to start counting. As per counter equations-

$$D_0 = (Q_0)_{prev} \oplus Enable \quad (1)$$

$$D_1 = (Q_1)_{prev} \oplus [(Q_0)_{prev} Enable] \quad (2)$$

$$D_2 = (Q_2)_{prev} \oplus [(Q_1)_{prev}(Q_0)_{prev} Enable] \quad (3)$$

$$D_3 = (Q_3)_{prev} \oplus [(Q_2)_{prev}(Q_1)_{prev}(Q_0)_{prev} Enable] \quad (4)$$

the next output to be fed back to input of cell. This is done via serial input/output of cells. The routing is done through switch box. The mux selection is for sequential logic so all the serial outputs are clocked with clk-clb. Each cell has four serial outputs out of that only one output has to be fed back. Eg. First cell's Q0 has to be fed back, second cell's Q1 has to be fed back and so on. As per the equations the outputs have to be routed to next cells too. The counter outputs are available at cell-SBin (cell to switch box output line).

A. Configuration of Counter Switch Box

The switch boxes of counter shown in Fig. 6 has defined routing. The four switch boxes have different routing for each of them. Each switch box has to acquire the previous cell outputs via west bus and its associated cells output (via cell-SB bus). There are four defined operations of counter switch box-

- Cell-SBin data fed back to cell-SBout (Qprev of same cell)
- Cell-SBin data transfer to east bus (Qnext to next cell)
- West bus data transfer to one output of cell-SBout (Qprev of previous cell)
- West bus data transfer to east bus (transfer of signal between switch box)

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The east bus of one switch box is connected to west bus of next switch box in the fabric.

All the three data lines of east and west buses are utilized for this implementation. This puts the limitation of the approach for bigger circuits. The routing need to be automated for that.

Q0 Cell-SBout(3)	Q1 Cell-SBout(2)	Q2 Cell-SBout(1)	Q3 Cell-SBout(0)	En Parin(0)	Cell1 Cell-SBin Q0next	Cell2 Cell-SBin Q1next	Cell3 Cell-SBin Q2next	Cell4 Cell-SBin Q3next
0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	0	0	1
0	0	0	1	1	1	0	0	1
0	0	1	0	0	0	0	1	0
0	0	1	0	1	1	0	1	0
0	0	1	1	1	1	0	1	1
0	1	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0	0
0	1	0	1	0	0	1	0	1
0	1	0	1	1	1	1	0	1
0	1	1	0	0	0	1	1	0
0	1	1	0	1	1	1	1	0
0	1	1	1	0	0	1	1	1
0	1	1	1	1	1	1	1	1
1	0	0	0	0	1	0	0	0
1	0	0	0	1	0	1	0	0
1	0	0	1	0	1	0	0	1
1	0	0	1	1	0	1	0	1
1	0	1	0	0	1	0	1	0
1	0	1	0	1	0	1	1	0
1	0	1	1	0	1	0	1	1
1	0	1	1	1	0	1	1	1
1	1	0	0	0	1	1	0	0
1	1	0	0	1	0	1	0	0
1	1	0	1	0	1	1	0	1
1	1	0	1	1	0	1	1	1
1	1	1	0	0	1	1	1	0
1	1	1	0	1	0	0	0	1
1	1	1	1	0	1	1	1	0
1	1	1	1	1	0	0	0	0

Fig. 7. Counter Look Up Table

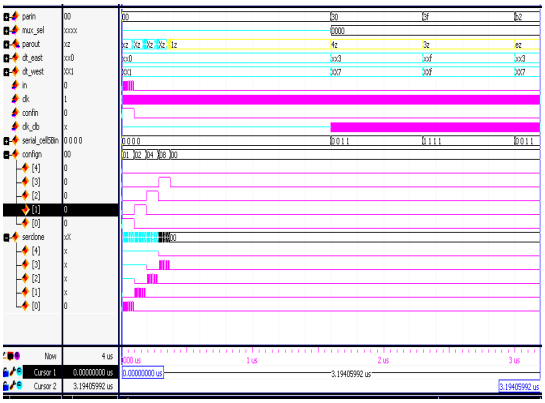

Fig. 8. Adder Simulation results

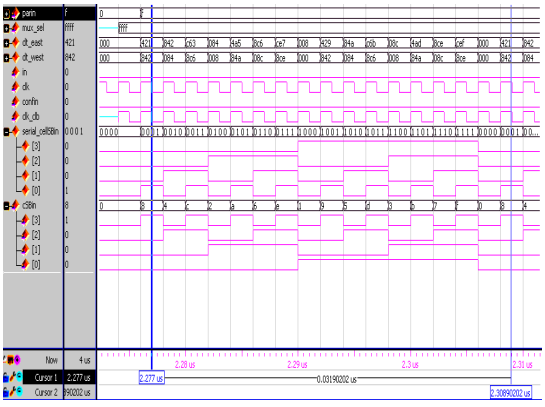

Fig. 9. Counter Simulation results

B. Counter Look Up Table

The counter LUT is shown in Fig. 7. While first cell LUT has inputs Q0 and parin (En), the other Q1,Q2 and Q3 are as dont care. To have same LUT data for all cells, all cell LUTs has inputs as cell-SB(0:3) and parin. The output is sent to next cell through cell-SBin. The previous cell's output is through west bus of one switch box to cell-SBout of next switch box.

V. Simulation Results

The simulation result of adder is shown in Fig. 8 . The serial cloning is done for four cells with the confign signal. Once LUT data is stored, the mux selection is done for '0000' (combinational logic). The parallel inputs are applied at parin and the previous carry for first cell is set through dt-west. Three different 4 bit additions are tested. First set is '1'(previous carry)+ '0011'(parin MSB) + '0'(parin LSB). The sum is stored in parout ('0100')and the carry at each cell is transferred through serial-cellSBin ('0011').

The simulation result of counter is shown in Fig. 9. For counter the mux selection is done for '1111' (sequential logic). Each cell has four serial outputs. The output is selected for transfer through cellSBin eg. Q0 from first cell, Q1 from second cell and so on. This is fed back to same cell and carried forward by east bus to next cell. The counter output is available at serial-cSBin shown in the figure. The input bus of cell3 from switch box is shown as cSBin. The cSBbin data corresponds to counter outputs Q0Q1Q2Q3 in reverse order.

VI. Conclusion

The switch box topology is designed and tested for generic embryonic cell fabric. The routing is based on circuit functionality and need to be automated. The self-repair [7] feature to be introduced in the fabric.

The approach mentioned in [8] integrates the evolutionary algorithm on embryonic fabric for self healing. This will lead to design optimization in the fabric. Recent review paper [9] talks about the scalability issues of embryonic approach for future applications.

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