Topology Optimization of 3D Hybrid Optical-Electronic Networks-on-Chip

Zhicheng Zhou, Ning Wu, and Gaizhen Yan

***Abstract*—Power and latency constraints of the electronic interconnection would greatly limit the scalability of future Multi-Processors System-on-Chip (MPSoC). The emerging silicon optical interconnection and 3D integration are envisioned as the promising technologies to solve the problem. However, due to the necessity of optical-electronic signal conversion, the ultra-fast propagation and low power consumption of the optical links might be under-utilized when the communication distance is short. Therefore, we are motivated to develop a hybrid interconnection architecture, in which, large and long distance packets are delivered in the optical links and the others would propagate in the electronic ones. Anyway, distribution of the optical routers would greatly affect the system performance. An ILP (Integer Linear Programming) based method has been proposed to optimize the proposed hybrid architecture in this paper. Compared to the mesh-based Optical Networks-on-Chip (ONoC) with the same topology size, the proposed Hybrid Optical-Electronic Networks-on-Chip (HOE-NoC) has reduced the energy efficiency by 10.2%.**

***Index Terms*—MPSoC, interconnection architecture, ILP optimization, HOE-NoC**

I. INTRODUCTION

WITH the rapid development of large scale and high density integrated circuits, the scale of the Multi-Processors System-on-Chip (MPSoC) is increasing. There are a large number of challenges in SoC development namely communication and synchronization among on-chip modules or cores. Networks-on-Chip (NoC) have been proved to be a promising interconnection in providing better performance, reducing chip area and power consumption [1]–[2]. However, in deep submicron (DSM) VLSI technologies, copper-based metallic interconnects are becoming increasingly susceptible to parasitic resistance and capacitance [3]. Both chip-to-chip and on-chip global interconnects are facing serious problems of delay, power consumption, and electromagnetic interference (EMI). As feature sizes continue to decrease, metallic interconnects would consume significant amounts of power to deliver the higher communication bandwidth required in the near future, and Electronic NoC (ENoC) may not be able to satisfy future performance requirements under certain power restrictions. As the increasingly required communication bandwidth, power consumption and transmission latency have become the bottleneck of the traditional ENoC [4]–[5].

Recently, Optical NoC (ONoC) are envisioned as a disruptive technology to overcome the problems in the traditional ENoC [6]–[7]. With the heterogeneous integration capability offered by 3D technology, one chip can integrate optical die together with CMOS processor dies [8]. Although ONoC promise low power and high-throughput communication, they also present design challenges. For the first, communication locality is poorly supported in traditional mesh and torus based ONoC. In nonhierarchical networks, such as generic mesh and torus, short and long distance traffic interfere with each other and cause low network utilization and large communication latency. Secondly, optical circuit switching mechanisms are only effective for long-distance traffic, but for short-distance traffic, the overhead of circuit switching limits the communication efficiency [9]. Thirdly, due to the necessity of optical-electronic signal conversion, the power consumption and latency caused by the optical-electronic conversion unit, might not be compensated by the low cost waveguide, when the communication distance is short. To fully utilize the bandwidth and power advantage of the optical signal, while retain high flexibility and low cost of the electric link, HOE-NoC architectures have been proposed, in which long distance packets are delivered in the optical links and the others would propagate in the electronic ones.

There is already a number of work covering HOE-NoC. Ye et al. [10] presented a torus-based hierarchical hybrid optical-electronic NoC, which takes advantage of both electrical and optical routers and interconnects in a hierarchical manner. Each four processors are grouped into a cluster and all the clusters are interconnected through optical switching and waveguides. The drawback of this scheme is that nodes in different cluster would communicate through optical links, even when they are neighbors. This might limit the programing flexibility. Tan et al. [11] explored a butterfly fat tree-based hybrid optoelectronic NoC architecture, in which the generic wavelength-routed optical router is utilized at the top level for

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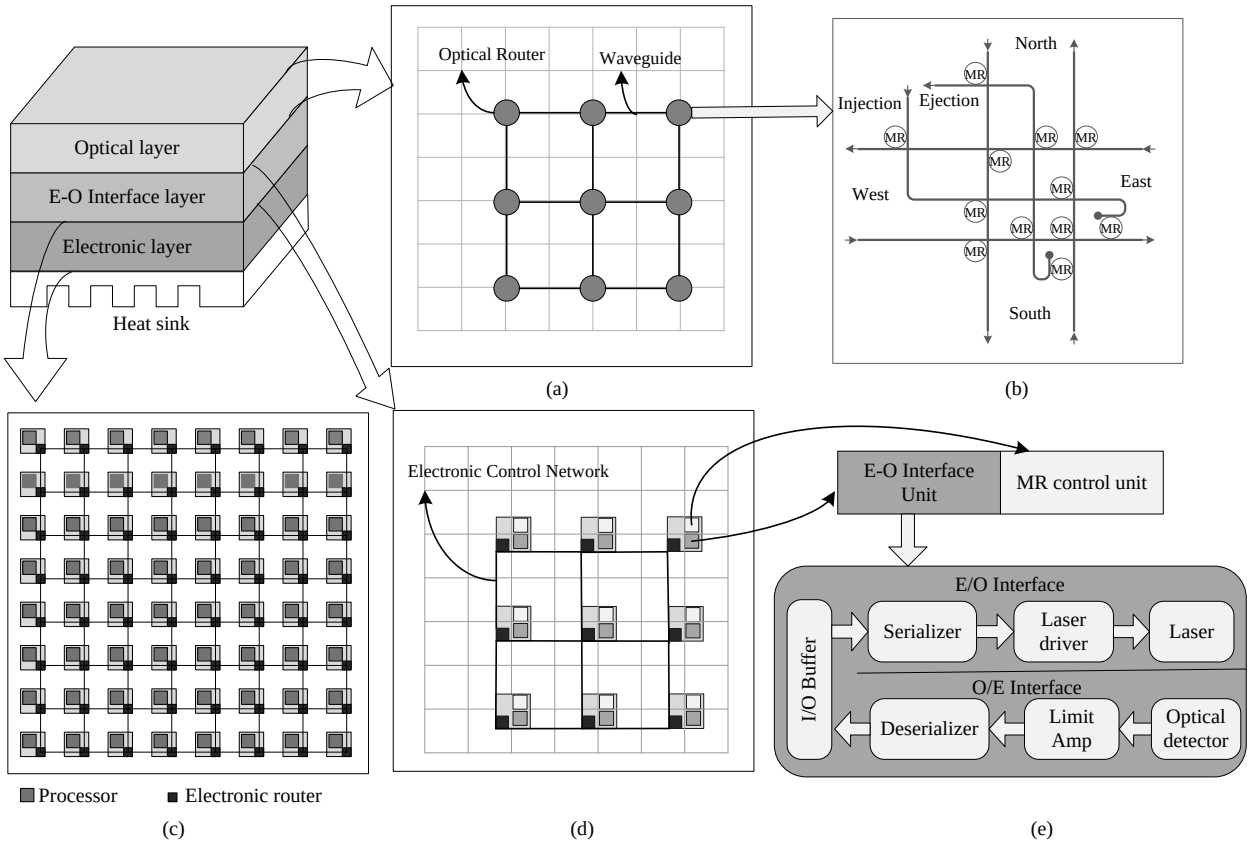

Fig. 1 Architecture of 3D HOE-NoC. (a) Optical layer consists of optical router and waveguide. (b) Architecture of Crux router. (c) Electrical layer consists processor and electronic router. (d) E-O interface layer consists of electronic control network, MR control unit and E-O interface. (e) E-O Interface Unit include E/O interface and O/E interface.

global communication and electronic sub-tree networks are applied for local communication. With the increasing of the tree level, bandwidth bottleneck might be formed at the top level. There are also HOE-NoC employ large size optical crossbars between clusters, such as Corona [12] and Firefly [13]. Large size crossbars also suffer from significant power loss on the waveguide and micro-ring scattering loss [11].

Based on the above observation, we propose a mesh based HOE-NoC for MPSoC. It is composed of an electrical interconnection layer and an optical layer. Each layer was connected by TSV (through-silicon via). the electrical interconnection layer is a normal 2D mesh architecture, in order to provde locality for any two nighboured nodes. Number and distribution of the Optical routers would greatly affect the system performance. We propose an ILP based method to optimize the number and position of optical router.

The rest paper arranged as follows: Section 2 describe the architecture of the 3D HONoC and introduce the optimal placement scheme of optical router. Section 3 introduce the routing mechanism. Optimal placement results of the optical router and performance comparison will be given in section 4. Section 5 is the conclusion of this paper.

II. THE PROPOSED HOE-NOC AND OPTIMIZATION

A. Architecture of HOE-NoC

A proposed mesh based architecture of HOE-NoC is shown in Fig. 1. The top layer is optical layer which consists of optical router which connected by waveguides, as shown in Fig. 1(a). The bottom layer is electrical layer close to the heat dissipation, as shown in Fig. 1(c). Electrical layer contains processor and electronic router in each tile. E-O Interface layer of the system contains all the optoelectronic components (modulators, detectors) required for the optical routing, as shown in Fig. 1(d). Each layer was connected by TSV.

We choose Crux router as the optical router [14], as shown in Fig. 1(b). The five bidirectional ports include injection/ejection, east, south, west, and north ports. They are aligned to their intended directions so no extra crossings will be incurred in the floorplan. Input and output of each port are also properly aligned. Crux is constructed based on two basic switching elements, both of which consist of two optical waveguides and one MR. As shown in Fig. 2.

When packet was transmitted through the optical layer, a path-setup packet would be routed in the electronic control network for path reservation. MR will be powered on according to path-setup packet. A reservation table is used in each router control unit to identify the state of the local router ports. In case the target optical link has been reserved by another transmission, the path-setup packet will be stalled at the current router and wait for the release of the link.

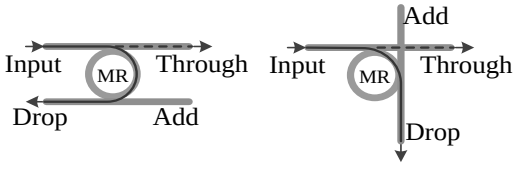

Fig. 2 Two basic switching elements of optical router

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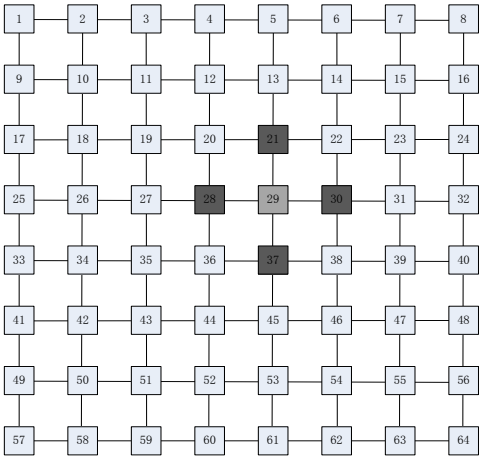

Fig. 3 The points collection within 1 MD to node 29

B. *The optimization of proposed HOE-NoC*

In an 80 nm design, while the O-E interfaces consume about 2.5 pJ/bit, the laser sources consume about 1.68 pJ/bit, which accounts for a large proportion of the total optical layer power consumption [15]–[16]. In context of ensuring the system performance, we need to minimize the number of optical router, thus decreasing the power consumption of the photoelectric interface. In this paper, we have figured out an ILP based optimization method to determine the number and distribution of the optical router.

The optimal placement should satisfy the following requirements:

(1) Each node shall reach at least one optical router node within a determined distance.

(2) The number of optical router node shall be as small as possible.

The issue of finding an optimal placement of optical router in a network topology can be expressed as an optimization problem. In the next, we will present an Integer Linear Programming (ILP) method that considers the above requirements to find an optimal placement.

In a n×n scale optical network, we define the set of optical routers in a layer to X. The adjacency matrix is defined as follows:

$$A=\begin{pmatrix} a_{11} & a_{12} & \cdots & a_{1n} \\ a_{21} & a_{22} & \cdots & a_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ a_{n1} & a_{n2} & \cdots & a_{nn} \end{pmatrix}$$

If a direct connection between node n_i and n_j exists, the corresponding element a_{ij} of adjacency matrix A is one. Otherwise, a_{ij} is zero. Based on the matrix A, the distance matrix D can be derived. The elements d_{ij} of D indicate the Manhattan Distance between two nodes n_i and n_j. The collection of all points within 1 MD (Manhattan Distance) to a certain point which id is i is represented by the set O(i):

$$O(i)=\left\{ n_j \middle| 0 \le d_{ij} \le 1 \right\} \tag{1}$$

As shown in the Fig. 3, we take point 29 as the optical router, then O(29) = {21, 37, 28, 30, 29}. In this way, nodes within one hop to the optical router can be calculated.

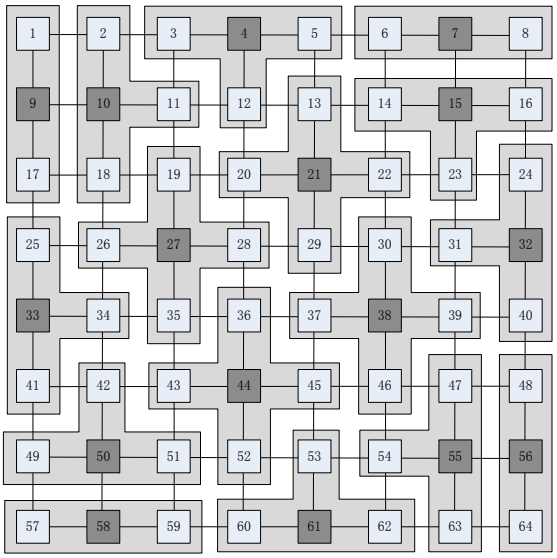

Fig. 4 The distribution of the optical router in 8×8 scale network

To represent the type of a node, a vector V is used. An element v_i is 1 if the corresponding node n_i is an optical router node, $v_i = 0$ represents a normal node. The minimal number f is obtained by the (2) that is the optimization objective function.

$$f=\min\sum v_i, v_i=\begin{cases} 1, & n_i \in X \\ 0, & n_i \notin X \end{cases} \tag{2}$$

The optimal placement of the optical routers is converted into a 0-1 ILP problem. The goal of optimization is to minimize the number of optical router. This will not only reduce the cost of the construction of optical network, but also can reduce the transmission distance of the network state information. The distribution of the optical router in 8×8 scale network is shown as Fig. 4.

An optimal architecture of 8×8 scale HOE-NoC as shown in Fig. 5. Electrical layer is divided into regions. Every region chose one node to connect with optical router in optical layer by TSVs.

III. ROUTING MECHANISM

Each processor is assigned a unique ID of (x_i, y_i, z_i) for addressing, and the local router has the same address. For a packet from the source processor $S(x_s, y_s, z_s)$ to the destination $D(x_d, y_d, z_d)$, as shown in Fig. 5. Firstly, we can calculate the Manhattan Distance L between node S and node D.

$$L=|x_s-x_d|+|y_s-y_d| \tag{3}$$

The power dissipation of each electronic router is η (J/bit). $L_{payload}$ is the payload packet size. Then if the packet routed in electronic layer, the total power consumption from S to D is:

$$P_E=\eta\times L\times L_{payload} \tag{4}$$

If the packet was transmitted though optical layer, the power dissipation can be calculated as (5), where P_{payload} is the energy consumed by a payload packet directly, and P_{ctr}

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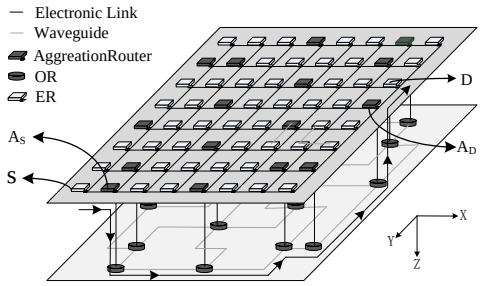

Fig. 5 The optimal architecture of HOE-NoC

is control overhead.

$$P_O = P_{\text{payload}} + P_{\text{ctr}} \tag{5}$$

P_{payload} can be calculated by (6), where m is the number of microresonators in the on-state while transferring the payload packet, P_{mr} is the average power consumed by a microresonator when it is in the on-state, $L_{payload}$ is the payload packet size, R is the data rate of EO-OE interfaces, P_{OE} is the energy consumed for 1-bit OE and EO conversions.

$$P_{\text{payload}} = (mP_{mr} \cdot \frac{1}{R} + P_{OE}) \cdot L_{payload} \tag{6}$$

P_{ctr} can be calculated by (7). L_{ctr} is the total size of the control packets used, h is the number of hops to transfer the payload

$$P_{ctr} = P_{OE} \cdot L_{ctr} \cdot h \tag{7}$$

When $P_E < P_O$, we choose XY routing algorithm to transmit packet only though electronic layer. Otherwise, $P_E > P_O$, the packet would be firstly transmitted from S to As. Then, propagated in optical layer. After finishing the optical transition, it will be back to electronic layer and arriving at point A_D. Finally, to the destination point D.

IV. EXPERIMENT AND RESULT

A. ILP results

The problem described in section 2 is a 0/1 ILP (Integer Linear Programming) problem. Lingo (Linear Interactive and General Optimizer), ILP software solver, can solve this problem conveniently. The experiment is conducted on 32 bits Win7 computer system equipped with 3.3Ghz core i3 CPU and 4G memory.

As Shown in the Fig. 6, bigger scale will result in longer time. In a small scale, the ILP problem is solved successfully in very short time. After the scale reaches 12×12, solution time increases sharply. Under different network scale, the distribution of sink node is shown in the following Table 1.

Table 1 Distribution of aggregation nodes in different scale

Scale	Num	Aggregation node id
3×3	3	2 5 8
4×4	4	3 5 12 14
5×5	7	3 6 10 12 19 21 24
6×6	10	2 4 7 12 15 19 23 28 32 36
7×7	12	3 5 8 14 18 23 27 32 36 42 45 47
8×8	16	4 7 9 10 15 21 27 32 33 38 44 50 55 56 58 61
9×9	20	4 7 10 11 18 23 24 30 35 37 42 49 54 56 61 64 68 72 75 79
10×10	24	2 6 8 14 20 21 27 33 35 39 41 47 54 60 62 66 68 74 80 81 87 93 95 99
11×11	29	2 6 9 15 20 22 23 29 36 38 43 47 52 56 61 66 70 75 79 84 86 92 93 99 100 107 113 116 120
12×12	35	2 5 10 14 19 20 24 28 33 37 42 47 51 56 63 65 71 72 73 79 81 88 95 98 102 104 112 118 120 121 187 135 137 141 143
13×13	40	3 7 11 14 18 22 26 29 34 36 40 45 51 56 61 67 72 76 78 83 87 92 94 98 103 109 114 119 125 130 134 136 141 144 148 152 156 159 163 167
14×14	47	3 5 9 12 15 21 28 30 32 37 38 39 48 55 57 59 64 68 75 81 84 86 91 95 102 107 111 113 118 123 129 134 140 143 145 150 152 155 161 168 172 177 179 184 188 191 195
15×15	53	3 7 10 12 14 16 20 25 34 38 43 45 47 51 56 64 69 74 76 82 87 93 95 100 105 108 113 118 121 126 131 139 144 149 150 152 157 162 170 175 180 181 183 188 193 201 206 210 212 214 217 219 223
16×16	60	1 5 8 11 15 19 24 9 33 37 42 47 48 52 55 61 66 68 733 78 86 91 96 97 99 104 109 117 122 127 130 135 140 148 153 158 160 161 166 171 179 184 189 191 195 197 202 205 209 215 219 224 228 233 238 242 246 249 252 256

B. Simulation experiments

The motivation of this paper is to enhance the performance and energy efficiency by taking advantage of ENoC and

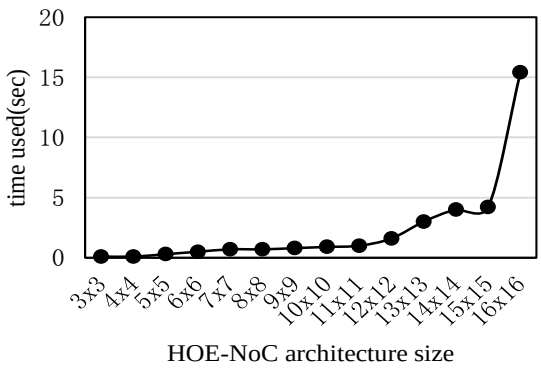

Fig. 6 Time required by ILP to find an optimal placement of optical router

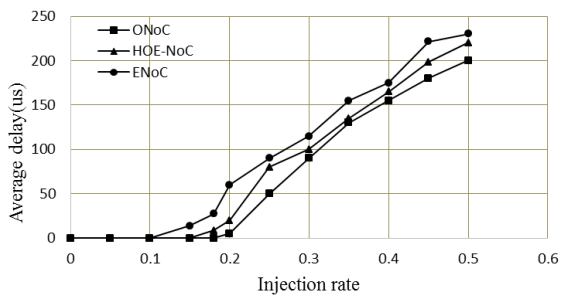

Fig. 7 Average latency comparison at different injection rate

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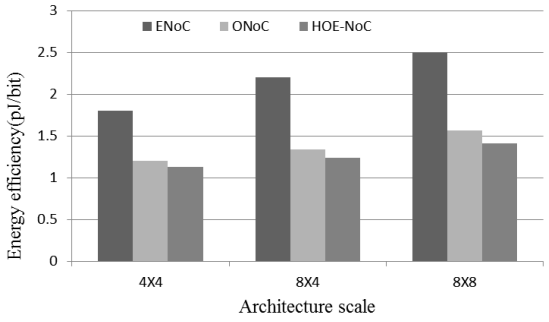

Fig. 8 Energy efficiency under different architecture

ONoC. All the comparisons between different NoCs are on equal footing for the 8×8 cores. We evaluated the lantency and energy efficiency of the proposed HOE-NoC for MPSoC in 45 nm, and compared it with the matched ONoC and the ENoC. SystemC-based cycle-accurate simulators are developed for network simulations of the proposed HOE-NoC and the referenced NoCs.

In the experiment, the length of the ordinary data packet is 1024B. The average latency of three kinds of NoCs under different packet injection rate is shown in Figure 7. It is shown that the network latency increases with the injection rate, and after a saturation point, the packet delay of all the three NoCs increase dramatically. At the injection rate of 0.45, the average packet delay of the ONoC increases to 180μs and the one of the HOE-NoC and ENoC are 198.6μs and 221.43μs, respectively. It seems that the mesh-based ONoC has the best performance in packet latency.

The energy efficiency comparison under the three NoCs is shown in Fig. 8. It is found that, under the 4×4, 8×4 and 8×8 topology size, the proposed HOE-NoC has reduced the energy efficiency by 5.8%, 7.4%, and 10.2%, respectively. The performance improvement in energy efficiency is better when the topology size is larger.

V. CONCLUSION

In this paper, we proposed a 3D mesh-based HOE-NoC for MPSoC, together with an ILP based method to optimize distribution of the optical routers. Packet latency and power efficiency have been compared to the ONoC and ENoC with the same topology size. It is found that, under 8×8 topology size, the proposed HOE-NoC has reduced 10.4% average latency compared with the ENoC at most. And the optimized HOE-NoC consumes 10.2% less energy compared to the ONoC.

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