Asynchronous Sequential Symbol Synchronizers based on Pulse Comparison by Hybrid Transitions at Quarter Bit Rate

Antonio D. Reis, Jose F. Rocha, Atilio S. Gameiro and Jose P. Carvalho

Abstract— **This work studies the asynchronous sequential symbol synchronizers based on pulse comparison by hybrid (both and positive) transitions at quarter bit rate. Their performance will be compared with the standard reference asynchronous symbol synchronizers based on pulse comparison by both transitions at bit rate.**

For the reference and proposed variants, we consider two versions which are the manual (m) and the automatic (a).

The objective is to study the four synchronizers and evaluate their output jitter UIRMS (Unit Interval Root Mean Square) versus input SNR (Signal Noise Ratio).

Index Terms—**Synchronism, Digital Communications**

I. INTRODUCTION

This work studies the asynchronous sequential symbol synchronizer based on pulse comparison operating by hybrid transitions at quarter bit rate (ah/4). Their jitter is compared with the standard reference asynchronous synchronizers operating by both transitions at bit rate (ab) [1, 2].

For both, reference and proposed variant, we consider the versions manual (m) and automatic (a) [3, 4, 5, 6, 7].

The difference between the reference and proposed synchronizer is in the symbol phase comparator since the other blocks are similar. The phase comparator compares the input variable pulse duration Pv with the intern reference fixed pulse duration Pf and the error pulse Pe synchronizes the VCO (Voltage Controlled Oscillator) [8, 9, 10].

The synchronizer regenerates the data, recovering a clock (VCO) that samples and retimes the data [11, 12, 13, 14].

Fig.1 shows the blocks of the general symbol synchronizer.

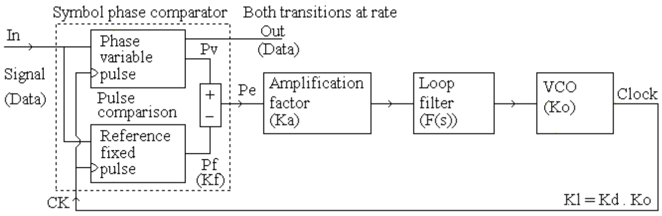

Fig.1 Synchronizer based on pulse comparison

Kf is the phase comparator gain, F(s) is the loop filter, Ko is the VCO gain and Ka is the loop amplification factor that controls the root locus and then the loop characteristics.

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In priori and actual-art state was developed various synchronizers, now is necessary to know their performance.

The motivation of this work is to create new synchronizers and to evaluate their performance with noise. This contribution increases the knowledge about synchronizers.

Following, we present the reference variant, asynchronous sequential symbol synchronizers based on pulse comparison by both transitions at bit rate, with versions manual (ab-m) and automatic (ab-a). Next, we present the proposed variant, asynchronous sequential symbol synchronizer based on pulse comparison by hybrid transitions at quarter bit rate, with versions manual (ab-m/4) and automatic (ah-a/4).

After, we present the design and tests. Then, we present the results. Finally, we present the conclusions.

II. REFERENCE BY BOTH AT BIT RATE

The standard reference, asynchronous sequential symbol synchronizers based on pulse comparison operating by both transitions at bit rate has two versions which are the manual (ab-m) and the automatic (ab-a) [1, 2]. The versions difference is in the phase comparator, the variable pulse Pv is common but the fixed Pf is different. Their jitter- SNR curves are the general quality reference.

A. Reference by both at rate manual (ab-m)

The block Pv, shown below, produces a variable pulse Pv between the input bits and VCO. The manual adjustment delay with Exor produces a manual fixed pulse Pf (Fig.2).

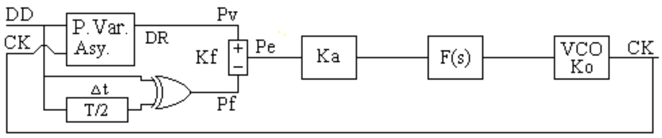

Fig.2 Asynchronous by both at rate and manual (ab-m)

The comparison between the pulses Pv and Pf provides the error pulse Pe that forces the VCO to synchronize the input. The block Pv is an asynchronous circuit (Fig.3).

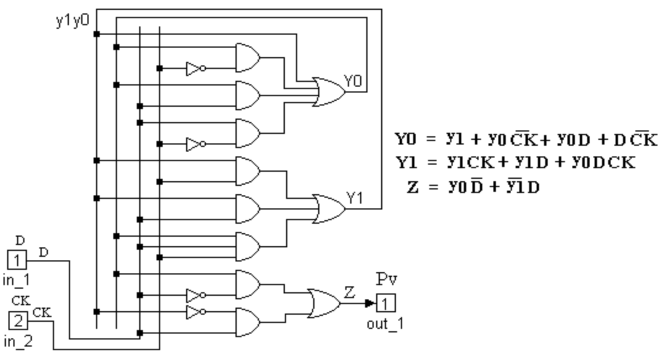

Fig.3 Intern aspect of the block Pv

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Fig.4 shows the waveforms of the reference manual (equal to the corresponding synchronous version) [3].

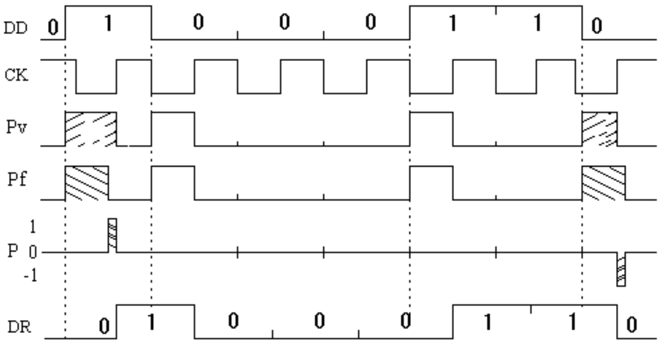

Fig.4 Waveforms of the asynchronous by both at rate manual

The error pulse Pe diminishes during the synchronization time and disappear at the equilibrium point.

B. Reference by both at rate automatic (ab-a)

The block Pv, common with anterior, produces the variable pulse Pv between input and VCO. The block Pf, shown below, produces the comparison fixed pulse Pf (Fig.5).

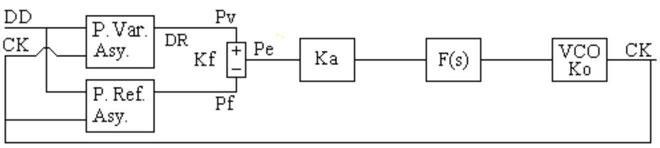

Fig.5 Asynchronous by both at rate and automatic (ab-a)

The comparison between the pulses Pv and Pf provides the error pulse Pe that forces the VCO to follow the input. The block Pf is an asynchronous circuit (Fig.6).

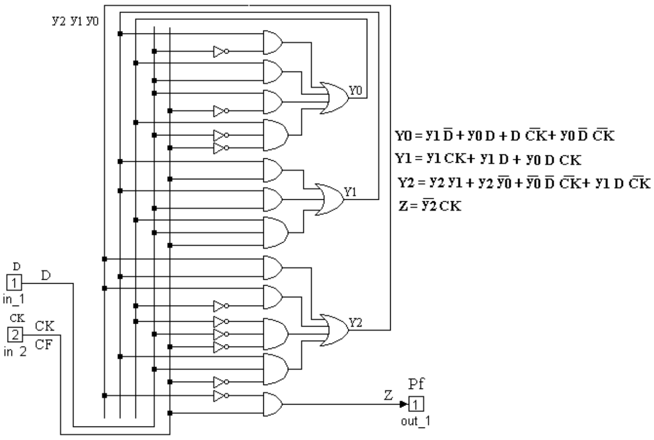

Fig.6 Intern aspect of the block Pf

Fig.7 shows the waveforms of the reference automatic (equal to the corresponding synchronous version) [3].

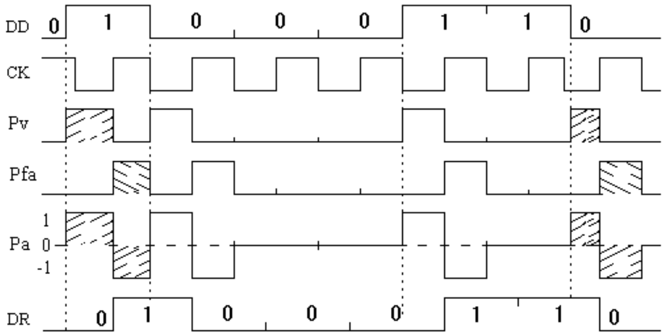

Fig.7 Waveforms of the asynchronous by both at rate automatic

The error pulse Pe don't disappear, but the variable area Pv is equal to the fixed Pf at the equilibrium point.

III. PROPOSAL BY HYBRID AT QUARTER BIT RATE

The new proposal, asynchronous sequential symbol synchronizers based on pulse comparison operating by hybrid transitions at quarter bit rate has also two versions namely the manual (ab-m/4) and the automatic (ah-a/4) [3]. The versions difference is in the phase comparator, the variable pulse Pv is common but the fixed Pf is different [4]. Their jitter- SNR curves will be compared with the previous.

A. Proposal by both at quarter manual (ab-m/4)

The block Pv produces the variable pulse Pv between input transitions and VCO. The manual adjustment delay T/2 with Exor produces a fixed pulse Pf (Fig.8).

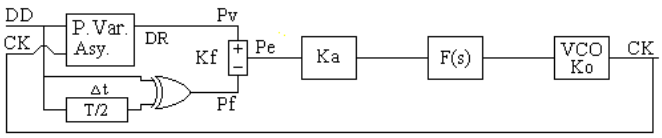

Fig.8 Asynchronous by both at quarter rate and manual (ab-m/4)

The comparison between pulses Pv and Pf provides the error pulse Pe that forces the VCO to synchronize the input.
The block Pv is an asynchronous circuit (Fig.9).

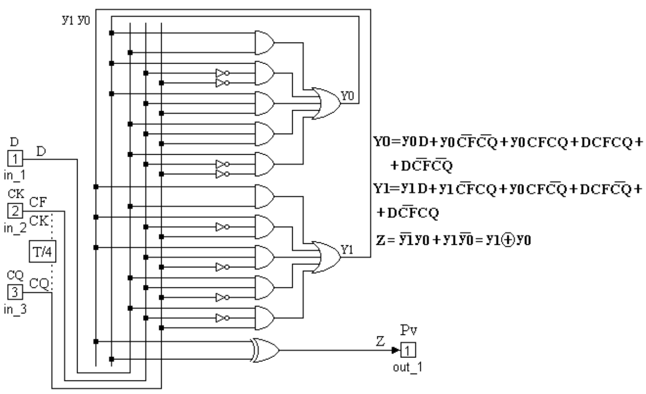

Fig.9 Intern aspect of the block Pv

Fig.10 shows the waveforms of the proposed manual (equal to the corresponding synchronous version) [3].

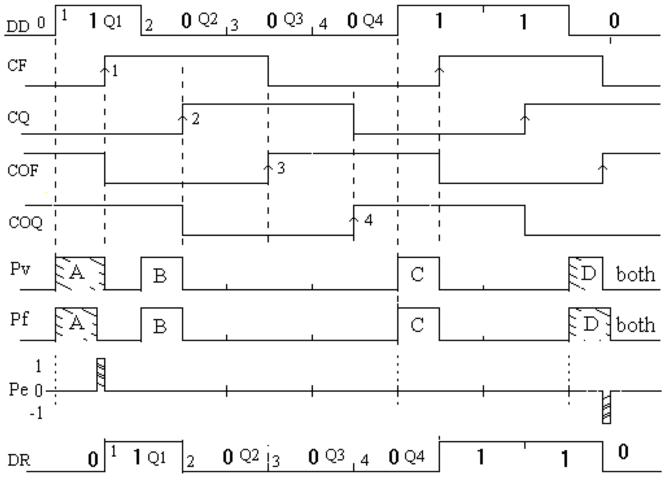

Fig.10 Waveforms of the asynchronous both at quarter rate manual

The error pulse Pe diminishes during the synchronization time and disappear at the equilibrium point.

B. Proposal by hybrid at quarter automatic (ah-a/4)

The block Pv, that is common, produces the variable pulse Pv between input and VCO. The block Pf, shown below, produces the comparison fixed pulse Pf (Fig.11).

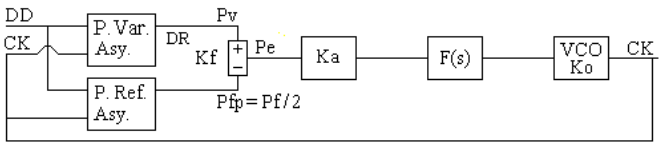

Fig.11 Asynchronous by hybrid at quarter rate automatic (ah-a/4)

The comparison between the pulses Pv and Pf provides the error pulse Pe that forces the VCO to follow the input. The block Pf, that uses hybrid transitions, is an asynchronous circuit (Fig.12). This block uses only positive transitions to generate pulses of a period T, instead T in both transitions. So, the multiplication by 0.5 is dispensed.

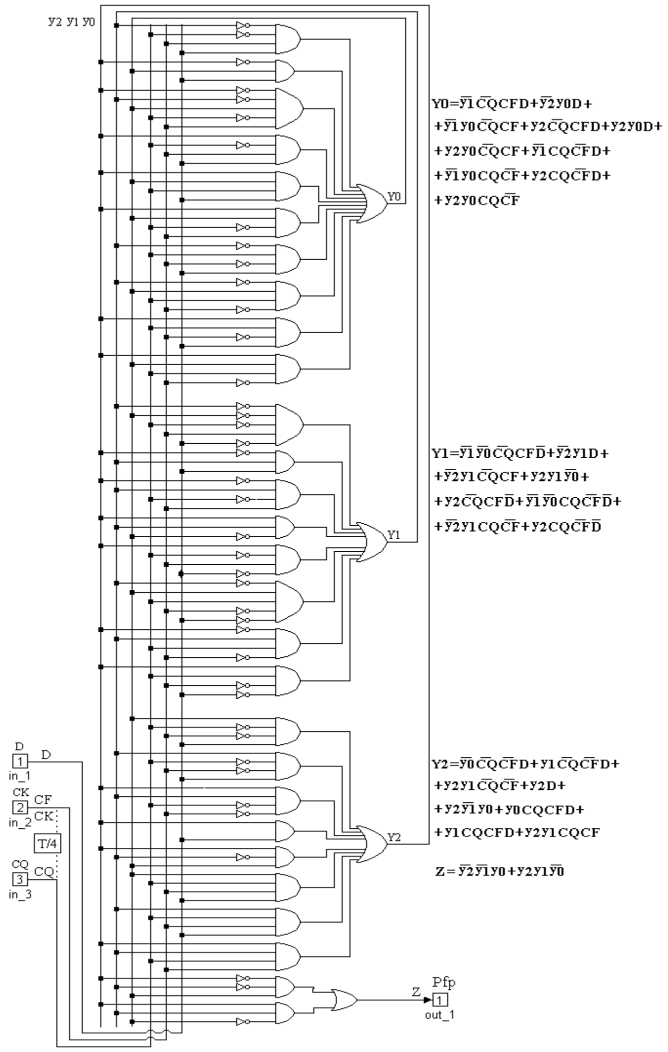

Fig.12 Intern aspect of the block Pfp (without the 0.5)

Fig.13 shows the waveforms of the proposed automatic (equal to the corresponding synchronous version) [3].

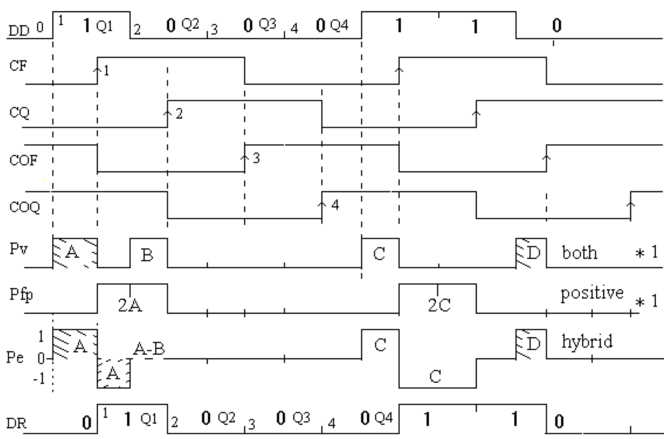

Fig.13 Waveforms of the asynchronous hybrid at quarter automatic

The error pulse Pe don't disappear, but the variable area Pv is equal to the fixed Pf at the equilibrium point.

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IV. DESIGN, TESTS AND RESULTS

We present the design, tests and results of the various synchronizers [5].

A. Design

We design all the synchronizers with the same loop gain conditions to have guaranteed results. The loop gain is Kl = Ka.Kf.Ko, where Kf and Ko are fixed. The Ka is the variable parameter that controls the loop characteristics.

To facilitate the analysis, we use normalized values for the bit rate tx= 1baud, clock frequency fCK=1Hz, extern noise bandwidth Bn=5Hz and loop noise bandwidth Bl=0.02Hz.

We apply a power signal Ps= A^2_{ef} with power noise Pn= No.Bn= $2\sigma n^2.\Delta\tau$.Bn, where σn is the noise standard deviation and $\Delta\tau$ =1/fSamp is the sampling period.

Then, the relation between SNR and noise variance σn^2 is

SNR= Ps/Pn= A^2_{ef}/(No.Bn)= $0.5^2/(2\sigma n^2 * 10^{-3} * 5) = 25/\sigma n^2$ (1)

Now, for each synchronizer, we must measure the output jitter UIRMS versus the input SNR

- 1st order loop:

The used cutoff loop filter F(s)= 0.5Hz, which is 25 times greater than Bl= 0.02Hz, eliminates the high frequency but maintains the loop characteristics. The transfer function is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKoF(s)}{s+KdKoF(s)}=\frac{KdKo}{s+KdKo} \quad (2)$$

the loop noise bandwidth is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (3)$$

So, with (Km=1, A=1/2, B=1/2, Ko=2π) and loop bandwidth Bl=0.02, we obtain respectively the Ka, for analog, hybrid, combinational and sequential synchronizers, then

$$Bl=(Ka.Kf.Ko)/4=(Ka.Km.A.B.Ko)/4 \rightarrow Ka=0.08*2/\pi \quad (4)$$

$$Bl=(Ka.Kf.Ko)/4=(Ka.Km.A.B.Ko)/4 \rightarrow Ka=0.08*2.2/\pi \quad (5)$$

$$Bl=(Ka.Kf.Ko)/4=(Ka*1/\pi*2\pi)/4 \rightarrow Ka=0.04 \quad (6)$$

$$Bl=(Ka.Kf.Ko)/4=(Ka*1/2\pi*2\pi)/4 \rightarrow Ka=0.08 \quad (7)$$

For the analog PLL, the jitter is

$$\sigma_\phi^2=Bl.No/Aef^2=0.02*10^{-3}*2\sigma n^2/0.5^2=16*10^{-5}.\sigma n^2 \quad (8)$$

For the others PLLs, the jitter formula is more complicated.

- 2nd order loop:

It is not used here, but provides similar results.

B. Tests

We used the following setup to test synchronizers (Fig.14)

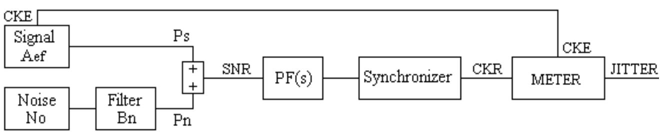

Fig.14 Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock, the difference is the jitter.

C. Results

We present the results in terms of output jitter UIRMS versus input SNR. Fig.15 shows the jitter- SNR curves of the four synchronizers which are the both rate manual(ab-m), the both rate automatic (ab-a), the both quarter rate manual (ap-m/4) and the hybrid quarter rate automatic (ah-a/4).

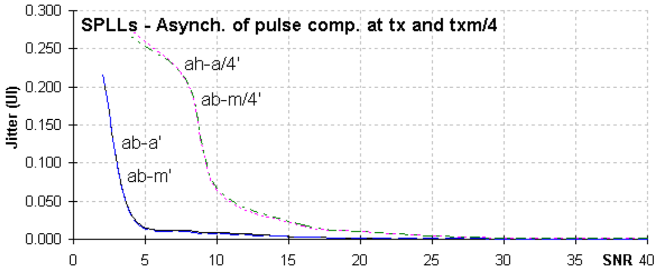

Fig.15 Jitter-SNR curves of the 4 synchro. (ab-m,ab-a,ab-m/4,ah-a/4)

We observe that, in general, the output jitter UIRMS decreases gradually with the input SNR increasing.

We verify that, for high SNR, the four jitter curves tend to be similar. However, for low SNR, the variant asynchronous both at rate manual (ab-m) and automatic (ab-a) are better than the variant asynchronous hybrid at quarter rate manual (ab-m/4) and automatic (ah-a/4).

V. CONCLUSIONS

We studied four synchronizers involving the reference variant asynchronous by both transitions at rate with versions manual (ab-m) and automatic (ab-a) and the proposed variant asynchronous by hybrid transitions at quarter rate with versions manual (ab-m/4) and automatic (ah-a/4). Then, we tested and compared their jitter - SNR curves.

We observed that, in general, the output UIRMS jitter curves decrease gradually with the input SNR increasing.

We verified that, for high SNR, the four synchronizers jitter curves tend to be similar, this is comprehensible since all the synchronizers are digital, with equal noise margin. However, for low SNR, the variant asynchronous by both at rate with their versions manual (ab-m) and automatic (ab-a) are better than the variant asynchronous by hybrid at quarter rate with their versions manual (ab-m/4) and automatic (ah-a/4), this is comprehensible because the variant by both transitions at rate has minus states than the variant by hybrid transitions at quarter rate and then, the time to pass from the error state to the correct state is lesser in 1st case.

In the future, we are planning to extend the present study to other types of synchronizers.

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