

Propagation Delay Analysis of Multi-layered GNR and Multi-walled CNT Through-Silicon Via at Different Technology Nodes

Pankaj Kumar Das, Anjali Yadav, Kamal Kumar

Abstract— In current era of Nanotechnology Through-silicon vias (TSVs) have potentially provided an attractive solution for the development of reliable 3D integrated system. The 3D integrated system is potentially dependent on the filler materials used in TSVs. This research paper introduces multi-walled carbon nanotubes (MWCNT) bundle and Multi-layered graphene nanoribbons (MLGNRs) as filler materials for TSVs. Equivalent single conductor (ESC) model for different bundle configuration is employed to analyze the propagation delays. It is observed that at lower technology node, the overall delays are reduced by 6.311% and 10.86% respectively for MWCT bundle and MLGNR compared to higher technology node.

Index Terms— Multi-walled Carbon Nanotubes (MWCNTs), Multi-layered Graphene Nanoribbons (MLGNRs), Through-Silicon Vias (TSVs), Propagation Delay.

I. INTRODUCTION

THE constant reduction of VLSI design has led to the rapid growth of VLSI technology. In the era of high speed technology, it is of utmost importance that device speed should be increased in order to provide high speed applications. High speed of VLSI circuits or IC's not only depends on the main circuit but also on interconnect used to connect various VLSI circuits. Although the continuous scaling is cost effective with less power dissipation and gate delays, it has enhance the challenges faced by interconnect delay in very large-scale integration (VLSI) circuits. So In 1965, according to the observation made by co-founder of Intel, Gordon-Moore it was predicted that the number of transistors increased per square inch on integrated circuit as the technology grew [1,2]. So according to him, this trend should continue into the fore seeable future i.e. number of transistors should increase with decrease in size of integrated circuits.

Earlier 2-D technology was being used in which two IC's are connected placing them in a common plane through interconnect devices. But due to which it led to an increased

area as transistor size could not further be reduced. It also had some other disadvantages such as short circuiting etc. in the traditional interconnect material being used is copper. Due to its high conductance property, it uses less energy to pass electricity through them. But one of the major disadvantages of copper is electro migration. It has been defined as the process of shape deformity of metal conductor under the high influence of electric current flowing through it. It may also cause breaking of conductor wire or interconnect thereby affecting the whole circuit. Major limitations of 2-D technology and electro migration in the past few years, has put a red brick end to the copper materials being used. To overcome above limitations 3-D technology was being introduced [1, 3]. It has some incomparable properties such as heterogeneous integration, improved latency and lower foot print. The latest development in this area is the 3D stacked IC using TSVs that employs a single package containing vertical stack of naked dies and allows the die to be vertically interconnect with another die.

To run-over copper's limitations, graphene has been introduced as one of the conceivable candidate material for both interconnect and transistors. It is a flat single layer of carbon atoms that are tightly packed into a 2-D honey comb lattice [4,5]. It is also the basic building block of CNTs, GNRs, graphite etc. but GNRs have one major advantage over CNTs that is its easy and straight forward fabrication process [6]. According to theory of tight bonding model, graphene is a semi-metal or a zero-gap semiconductor [7]. Graphene being ambi-polar that is can conductance takes place due to both holes and electrons and Boltzmann equation has been used to find conductivity. It has been found that the parasitic parameters depend on the number of conducting channels which in turn depends on the width and Fermi energy level [6].

This research paper introduces three different bundle arrangements of MWCNT and MLGNRs at the technology node 28, 32 and 90. Interconnect performance in terms of propagation delays has been analyzed.

The organization of paper is as follows: Section I introduces the unique properties of CNT and GNR and the use of TSVs in 3D vertical interconnect. Section II describes the geometrical arrangement of MWCNT bundle and MLGNR at various technologies. Section III introduces the ESC model of MWCNT bundle and MLGNR Simulation setup using DIL system is presented in section IV. Section V compares the results of MWCNT bundle and MLGNR at different technology node. Finally section VI

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draws a brief summary of the paper.

II. BUNDLE GEOMETRY AND ARRANGEMENT

Geometry of MLGNR above ground plane is shown in figure. 1. The distance between the ground plane and GNR layer is denoted by 'd' where $d= 50\text{nm}$ [8]. The distance between two layers of graphene is taken as 0.34nm [9,10]. Figure. 1 describes the arrangement of MLGNR for various technology nodes having an aspect ratio $AR= 2.5$.

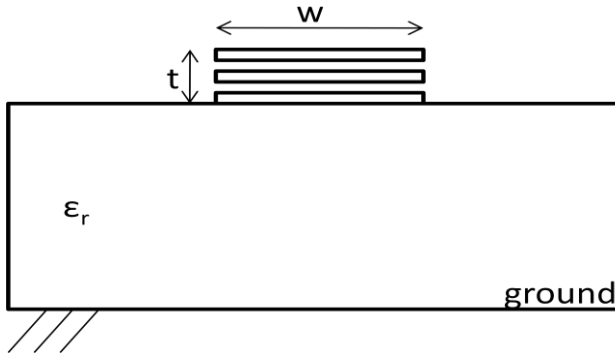


Figure 1. Geometry of MLGNR

Figure 1 shows the geometry of MLGNR, considering the geometry of MLGNR interconnects parasitic has been calculated. These parasitic depend upon the number of conducting channel of GNR, which is depends on the Fermi energy level and width of GNR [11].

Number of conducting channels is given by,

$$N_{CH}(w, E_F) = \begin{cases} a_0 + a_1w + a_2w^2 + a_3E_F + a_4wE_F + a_5E_F^2 & \text{for } E_F > 0 \\ b_0 + b_1w + b_2w^2 & \text{for } E_F < 0 \end{cases} \quad (1)$$

where a and b are constants defined in [11]. Total number of conducting channels for complete bundle of GNR is calculated by,

$$N_{TOTAL} = N_{CH} \times N_{LAYER} \quad (2)$$

where N_{LAYER} is the number of layers present in GNR at various technology nodes. It is given by [8],

$$N_{LAYER} = 1 + \frac{t}{\delta} \quad (3)$$

Where t and δ are the interconnect width and inter layer spacing respectively.

Let us consider that nano materials are made up of carbon nanotubes [12]. Different bundle configuration of MWCNT has been deployed and by using the bundle configuration various electrical parameters has been calculated for the analysis of interconnect performance [13, 14].

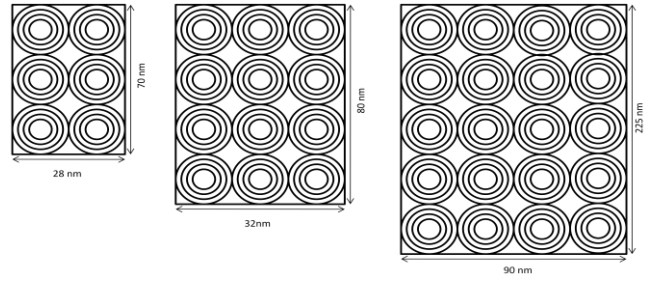


Figure 2. Geometry of 4-shell MWCNT bundle at different technology node

The aspect ratio (AR) of different bundle has been taken $AR= 2.5$ [13]. The bundle arrangements presents the 4- shell MWCNTs placed inside the bundle and bundle height and width varies with the technology node [20].

$$D_n = D_1 + 2 \times (n - 1) \times \delta \quad (4)$$

Where δ is the inter layer spacing equal to $.34\text{nm}$ [8] and n stands for number of shells.

The total number of 4-shell MWCNT placed in a bundle can be calculated as

$$N_{MWCNT} = N_W N_H - \text{integer} \left[\frac{N_H}{2} \right] \quad (5)$$

Where

$$N_W = \frac{W - D_n}{D_n + \delta} \quad N_H = \frac{H - D_n}{(D + \delta)\sqrt{3}/2} + 1 \quad (6)$$

N_W and N_H represent the number of CNT in horizontal and vertical direction.

III. ESC MODEL

Equivalent single conductor (ESC) model of MLGNR is build up using the concept of multi-conductor transmission line theory [8]

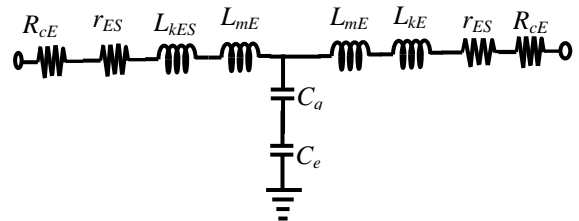


Figure 3. ESC model of MWCNT bundle

A. Metal contact resistance

It appears due to the imperfect metal- interconnect contact. It can be reduced with improved fabrication processes as it is totally fabrication dependent. It's value is approximately taken as [21]

$$R_{MC} = 3.2k\Omega \quad (7)$$

B. Scattering and quantum resistance (R_{ESC})

Scattering and quantum resistance arises due to higher nanotube length that exceeds mean free path of electrons and quantum confinement of electrons in a nano wire respectively [18]. The two resistance can be calculated from[1]

$$R_S = \frac{h}{2e^2 \times N_{LAYER}} \sum_n \left(\left(\frac{1}{\lambda_{eff}} \right)^{-1} \right)^{-1} \quad (8)$$

$$R_Q = \frac{h}{2 \times e^2 \times N_{TOTAL}} \quad (9)$$

C. Kinetic and magnetic inductance

Kinetic inductance arises from the kinetic energy of electrons. It depends upon the length of GNR and increases with it [18]. It is given by [1]

$$L_K = \frac{h}{4e^2 N_{CH} v_f} \quad (10)$$

where v_f is Fermi velocity. Magnetic inductance arises due to magnetic field induced by current flowing through a nanotube [1]

$$L_M = \frac{\mu_0 d}{w} \quad (11)$$

where μ_0 is the permittivity of free space, $\mu_0 = 1.25 \times 10^{-6}$ F/m

D. Quantum and electrostatic capacitance

Quantum capacitance represents finite density of states at Fermi energy whereas electrostatic capacitance arises due to the potential difference between the GNR bundle and ground plane [18]. They are given by

$$C_q = \frac{4e^2}{h v_f} \times N_{TOTAL} \quad (12)$$

E. Proposed TSV model for GNR

During the recent past years, several researchers have designed a way to stack ICs more compactly in order to achieve 'More than Moore' [22, 23]. In such organization, IC layers were stacked on top of each other in order to integrate more number of devices on a single chip which gave improved performance. This implemented technique is known as 3-D die stacking [24, 25]. Various advantages of this 3-D technology include higher transistor density, improved speed, lower power dissipation and area [26]. To achieve this type of arrangement a TSV model has been proposed in order to simplify the ESC model.

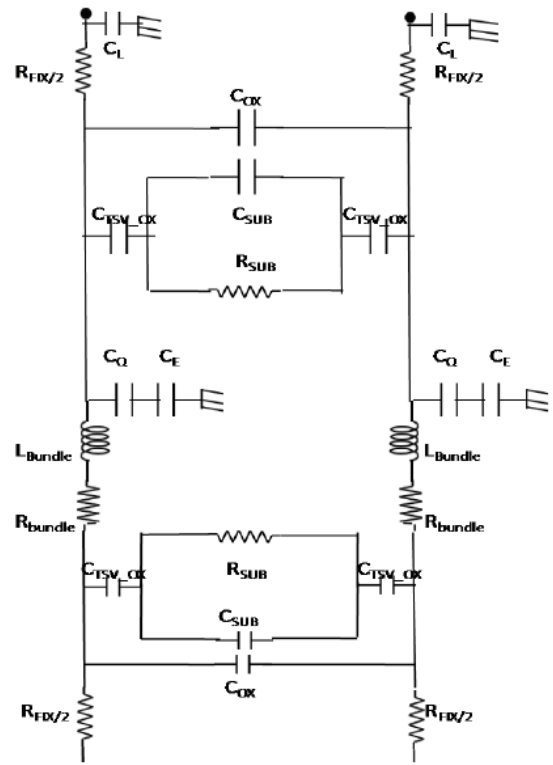


Figure 4. TSV model for GNR

C_{TSV-ox} is the oxide capacitance around the via [18]. C_{ox} is the oxide capacitance around two TSV [25, 27]. These two capacitances depend upon the thickness of SiO_2 layer (t_{ox}) and are given by

$$C_{TSV-ox} = \frac{4\epsilon_0 \epsilon_r t_{si} (w_{TSV} - t_{ox})}{t_{ox}} \quad (13)$$

$$C_{ox} = \left[\frac{2}{C_{TSV-ox}} + \left(\frac{\epsilon_0 \epsilon_r A}{d_{pitch} h} \right)^{-1} \right]^{-1} \quad (14)$$

where $A = H_{TSV} \times w_{TSV}$, $d_{pitch} = w + s$,

w is the width of TSV, s is the spacing between two TSVs, H_{TSV} = height of TSV, ϵ_0 is the permittivity of vacuum and ϵ_r is permittivity of SiO_2 .

The conductance and capacitance of silicon substrate are given by [18],

$$G_{SUB} = \frac{\sigma \pi}{\ln \left[\frac{d_{pitch} h}{w_{TSV}} + \sqrt{\left(\frac{d_{pitch} h}{w_{TSV}} \right)^2 - 1} \right]} \quad (15)$$

$$C_{SUB} = \frac{\epsilon_0 \epsilon_r A}{d_{pitch} h} \quad (16)$$

Where $\sigma = 0.1 (\Omega.cm)^{-1}$ is the conductivity of silicon substrate [18].

F. Quantum and intrinsic resistance (R'_q)

It appears due to the quantum confinement of electrons in a nano wire. It does not depend on length of GNR. It shows dependency on number of conducting channels and number of layers of GNR [18].

$$R_q' = \frac{h}{2e^2 N_{TOTAL}} \quad (17)$$

Scattering resistance exists due to higher nanotube length that exceeds mean free path of electrons. Due to this electrons suffer scattering and thus are scattered in a different directions [18].

$$R_s = \frac{h}{2e^2 \times N_{LAYER}} \times \sum_n \left(\frac{1}{\lambda_{eff_n}} \right)^{-1} \quad (18)$$

G. Quantum (C_Q') and Electrostatic capacitance (C_e)

Quantum capacitance in GNR represents the finite density of states at Fermi energy. It depends on the number of conducting channel and number of layers of GNR [12].

$$C_Q' = C_Q \times N_{TOTAL} \quad (19)$$

Electrostatic capacitances exists due to the potential difference between the GNR bundle and ground plane. It depends on the width of GNR and distance between GNR bundle and the ground [12].

$$C_e = \frac{\epsilon w}{d} \quad (20)$$

H. Kinetic and magnetic inductances

Kinetic inductance originates from kinetic energy of electrons. It depends upon the length of GNR and increases with increase in its length. Magnetic inductance arises due to magnetic field induced by current flowing through a nanotube [8].

$$L_K' = \frac{h}{4e^2 N_{CH} \theta_f} \quad (21)$$

IV. SIMULATION SETUP

This research paper analyzes the propagation delay for MLGNRs, and MWCNT bundle at various technology nodes at varying interconnect lengths ranging from 400µm to 2000 µm. DIL system with CMOS driver is used at 32nm technology node. The interconnect line of DIL system is terminated with a load capacitance $C_L = 10$ af with supply voltage $V_{dd} = 1V$ for accurate estimation of delay and crosstalk. The ESC models of MLGNR and MWCNT bundle are replace with the interconnect line [28].

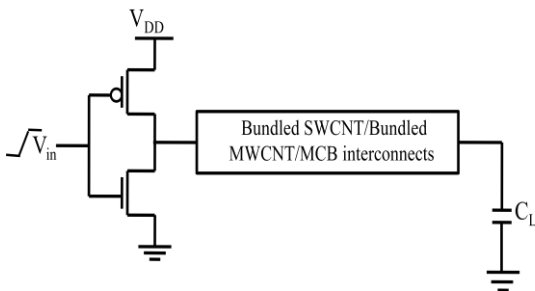


Fig.5. Driver Interconnect Load (DIL) System.

V. RESULTS AND DISCUSSION

HSPICE simulations are performed for MLGNRs and MWCNTs bundle structures to address the propagation

delay of different structures. The propagation delay increases with interconnect lengths but reduces at lower technology node. The reason behind that the propagation delay primarily depends on interconnect parasitic such as resistance, capacitance and inductance. The increasing number of shells in MWCNT increases the number of conducting channel due to that reduces the interconnect parasitics resistance and inductance results decreases the propagation delay.

Finally, the propagation delay for different bundle arrangements is summarized in Table 1. It has been observed that propagation delay significantly reduces for lower technology node.

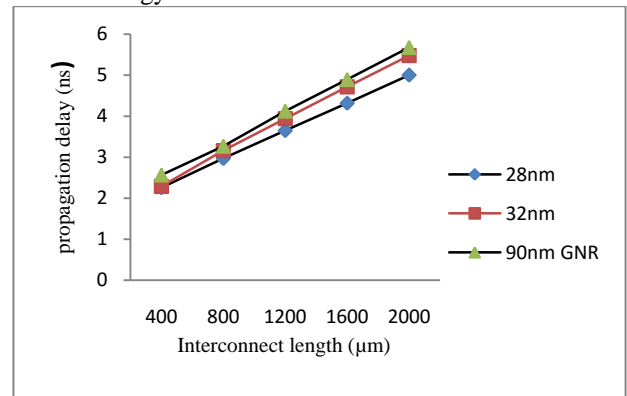


Figure 6. Propagation delays for MLGNRs structure at different technology node.

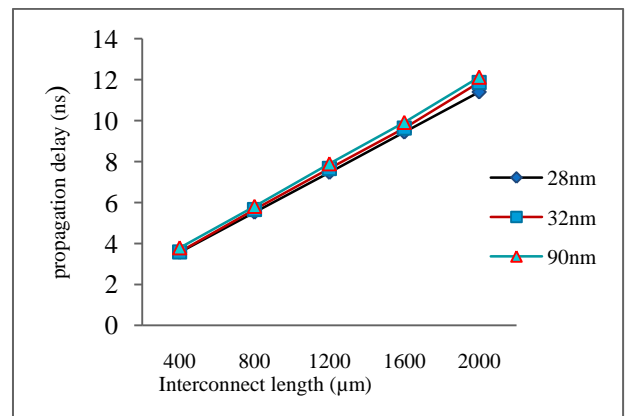


Figure 7. Propagation delays for MWCNT bundle structure at different technology node.

Table 1. Propagation Delay For MLGNR and MWCNT bundle at different technology node.

| Interconnect length (in µm) | 28nm | | 32nm | | 90nm | |
|-----------------------------|------|----------|------|----------|------|----------|
| | GNR | MWC - NT | GNR | MW-- CNT | GNR | MW-- CNT |
| 400 | 2.25 | 3.56 | 2.28 | 3.58 | 2.56 | 3.78 |
| 800 | 2.97 | 5.52 | 3.16 | 5.65 | 3.26 | 5.81 |
| 1200 | 3.65 | 7.46 | 3.94 | 7.66 | 4.12 | 7.89 |
| 1600 | 4.31 | 9.43 | 4.71 | 9.63 | 4.89 | 9.91 |
| 2000 | 5.00 | 11.40 | 5.48 | 11.86 | 5.54 | 12.12 |

VI. CONCLUSION

This paper introduces a MLGNRs and MWCNT bundle structure at different technology node and presented the ESC model for MLGNR and MWCNT bundle structure. Propagation delay has been analyzed for bundle structures at different global interconnect lengths. It has been observed that the propagation delay primarily depends on interconnect parasitic that is basically depends on the number of CNT presents in the bundle or on total number of conducting channel. On an average, the propagation delay are improved at lower technology node, the overall delays are reduced by 6.311% and 10.86% respectively for MWCT bundle and MLGNR compared to higher technology node.

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